Table of Contents

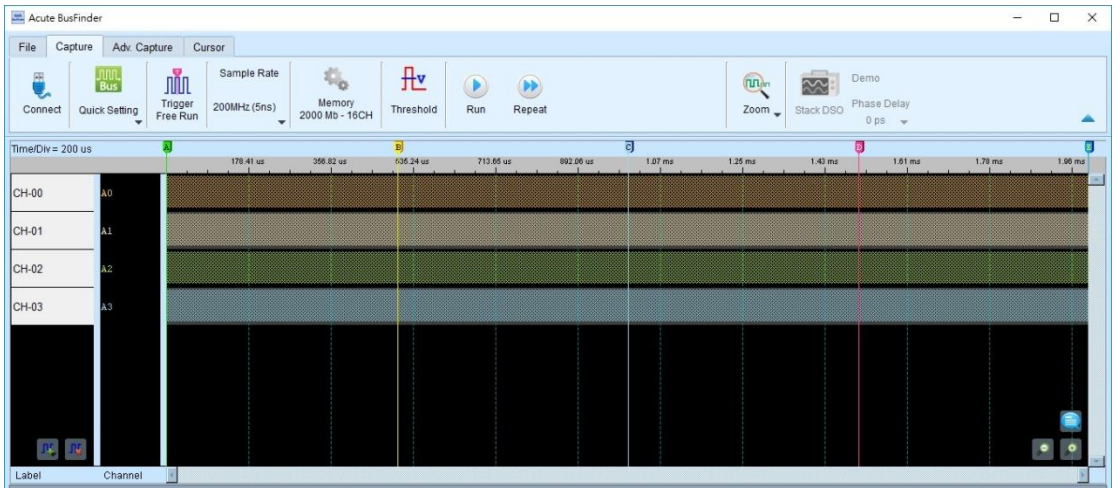
Chapter 1 Bus Decode

Basic operation

Add a Bus Decode

Method 1:

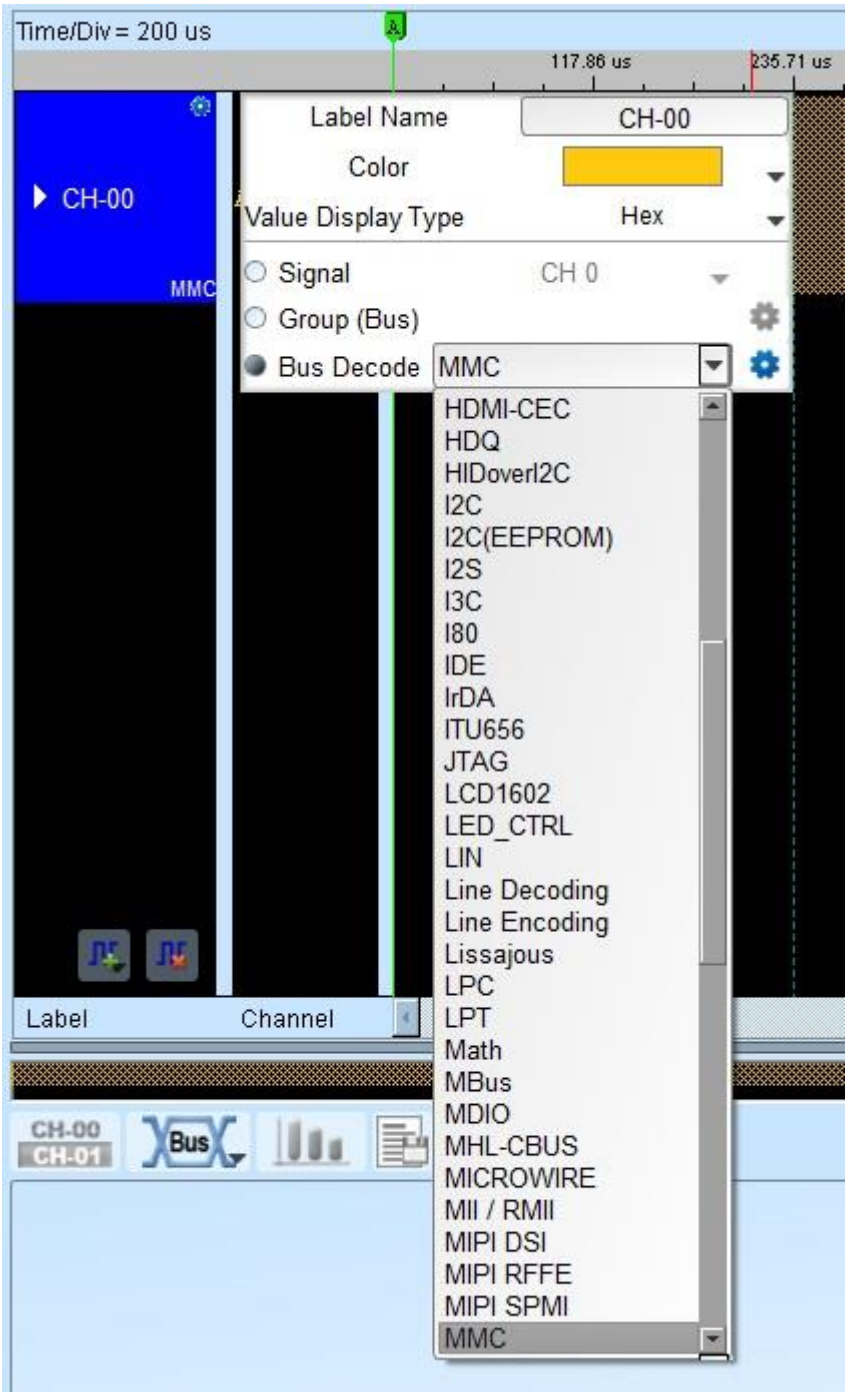
Click the Quick Setting  in the menu, and select the bus decode.



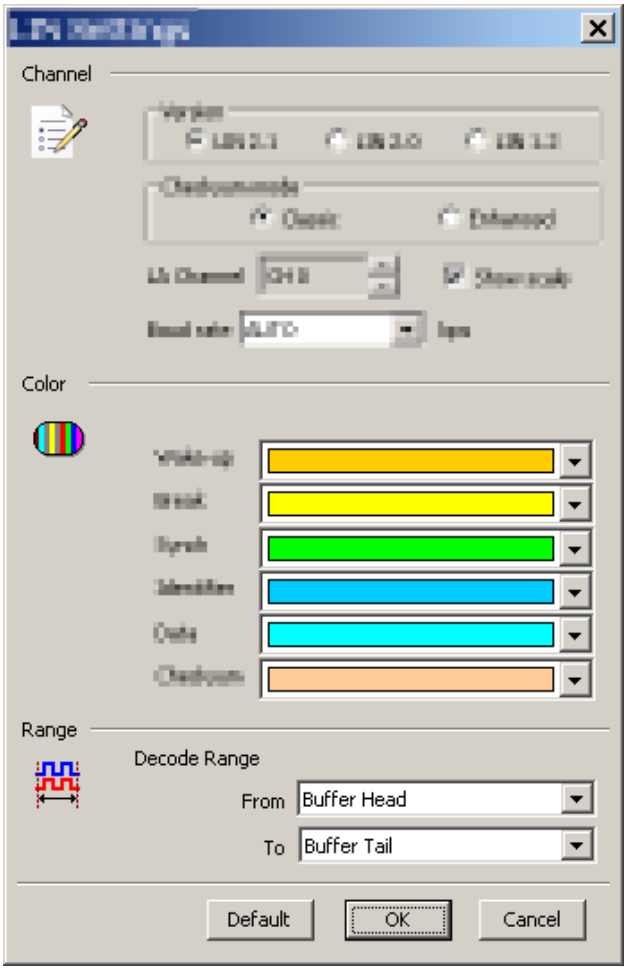
Method 2:

Click Add Bus Decode in the Label menu or right-click the label field to show the dialog box.

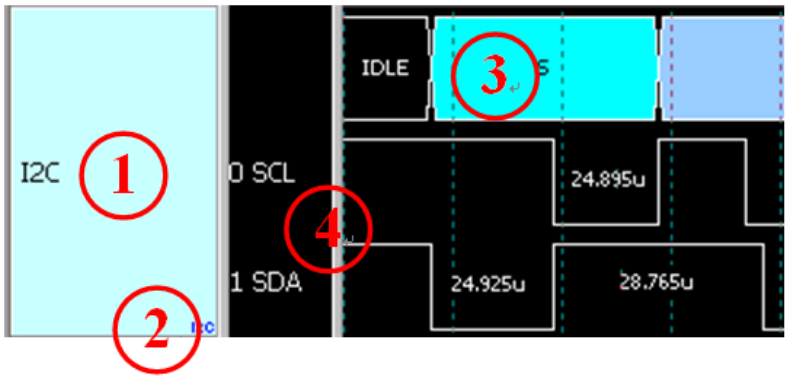
Advance channel setting



1. **Bus Name:** Enter the label name with 31 characters or less. (Chinese word expresses two characters.)
2. **Color:** Set the waveform color.
3. **Display the waveforms with decode**
4. **Display the waveforms with its decode together.**
5. **Advance:**



Set the decode parameters or press **OK** to use default settings. There are "Channel", "Color", "Range" settings



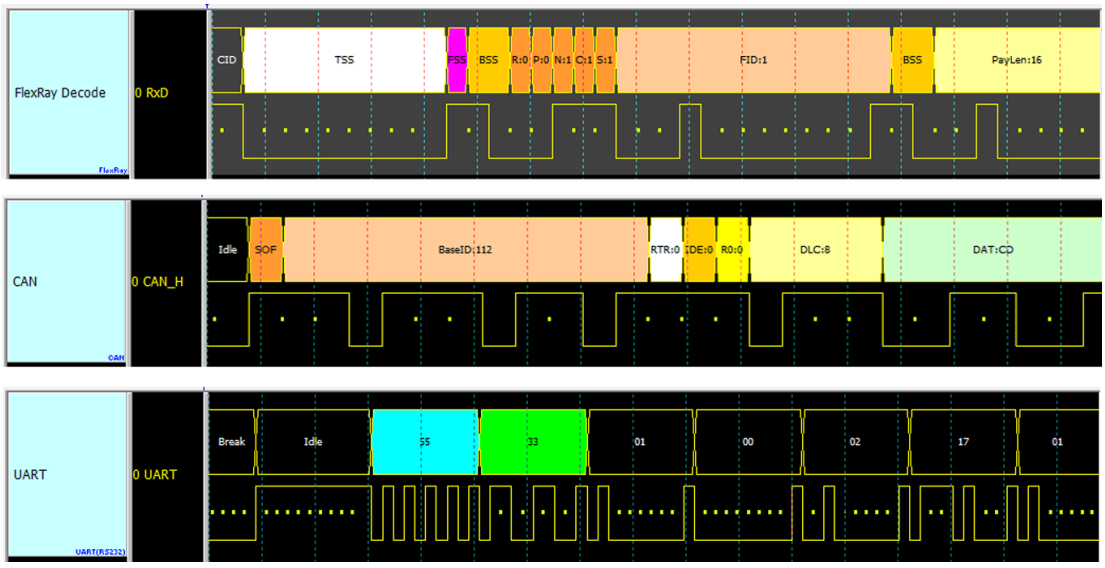
1. Bus name
2. Decode type
3. Result
4. Channel name & signal

Specially Bus Decode:

The bus decodes display the data in text format, but some decodes are able to show the original form for the data such as voice (I2S decode…), image, analog waveform (ADC decode) etc.

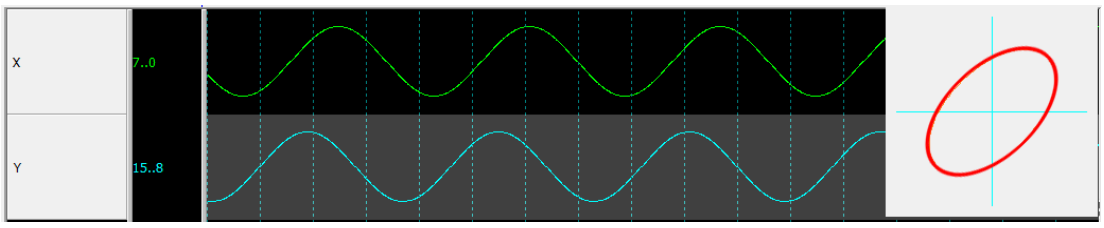
UART/CAN/FlexRay..bus decodes:

The data is displayed according to bit points in order to calculate the bit number。



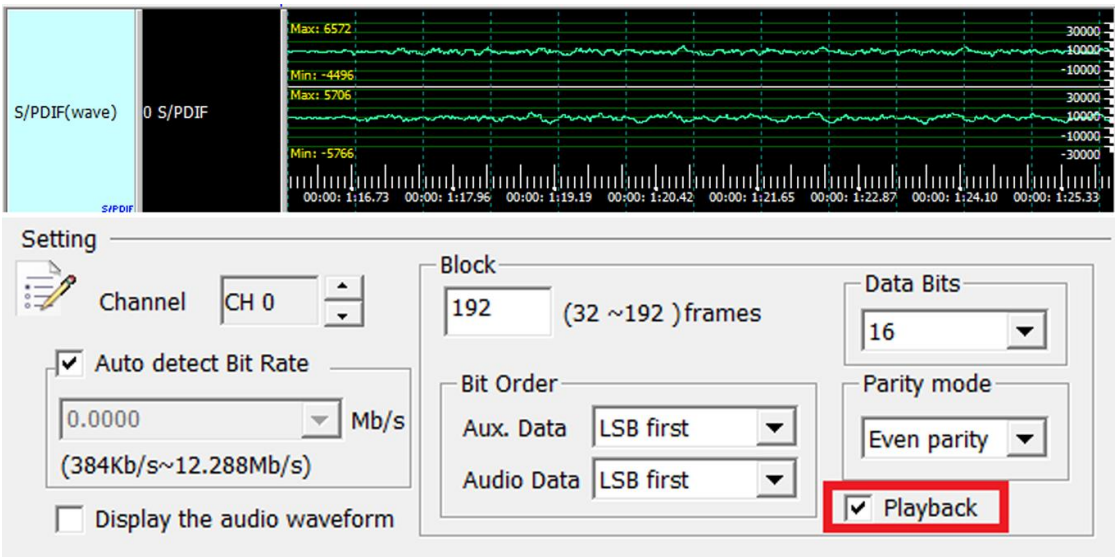
Lissajous analysis (released in 2009/09, LA Viewer Ver.2.0):

Display the signal in graph by X-Y or I-Q data。



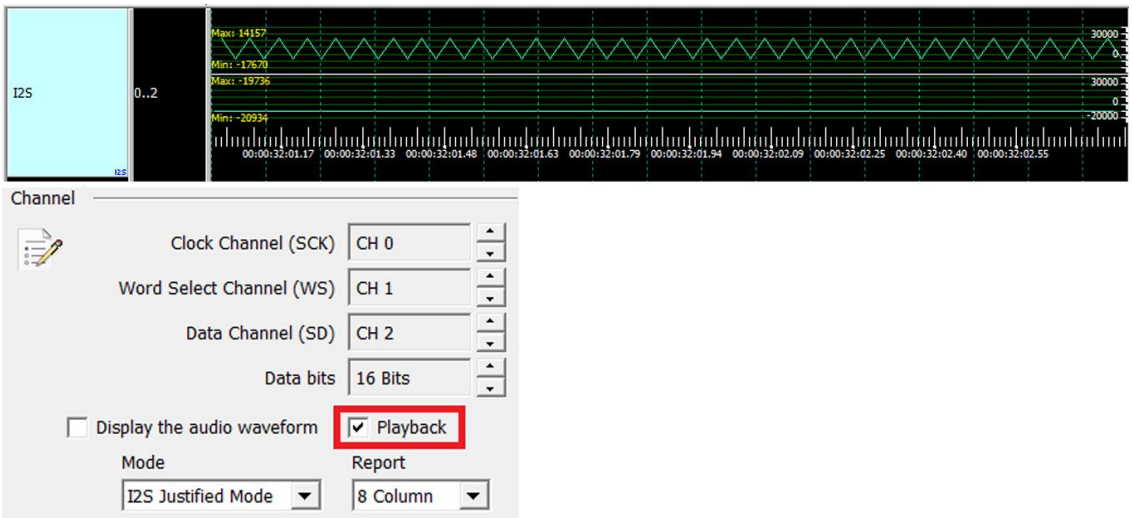
S/PDIF analysis:

Display the data in sound waveform。



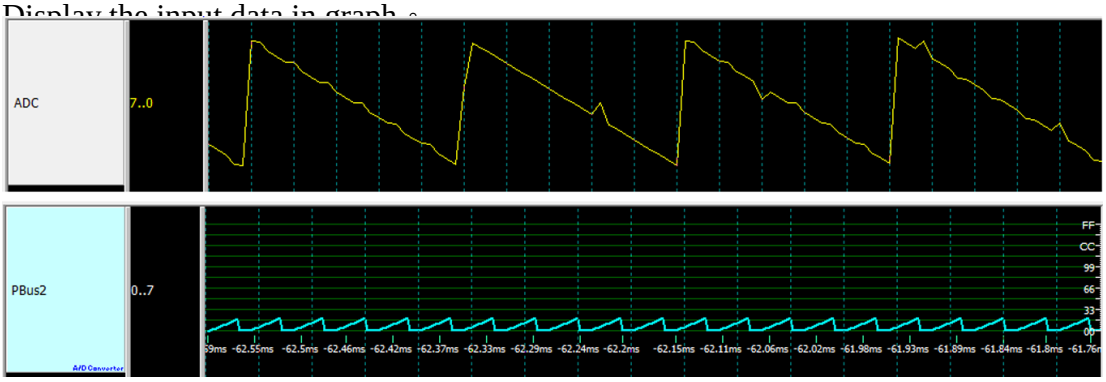
I2S analysis:

Display the data in sound waveform。



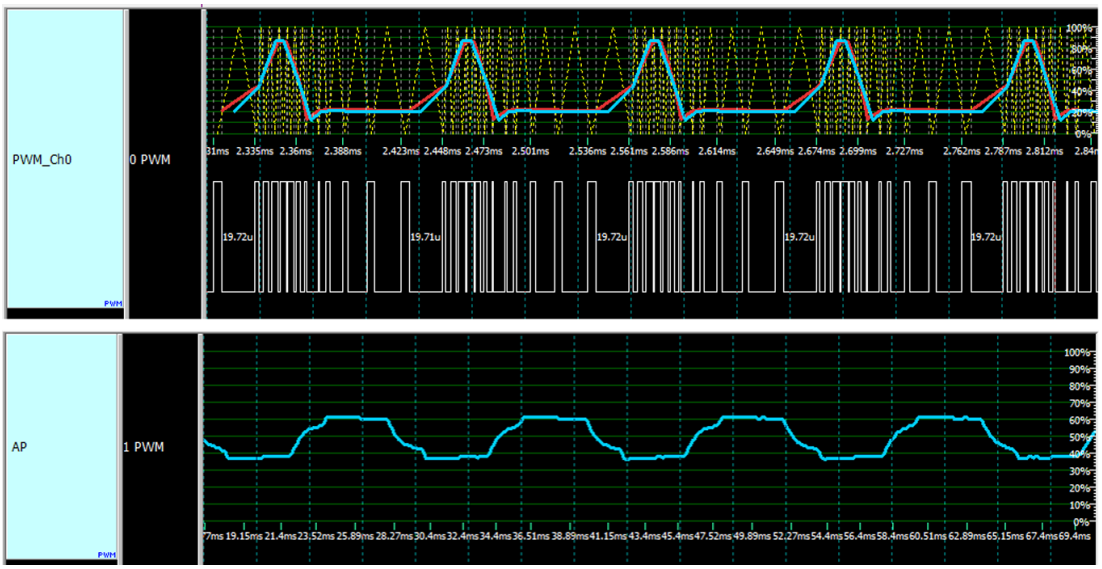
ADC bus decode:

Display the input data in graph。



PWM analysis:

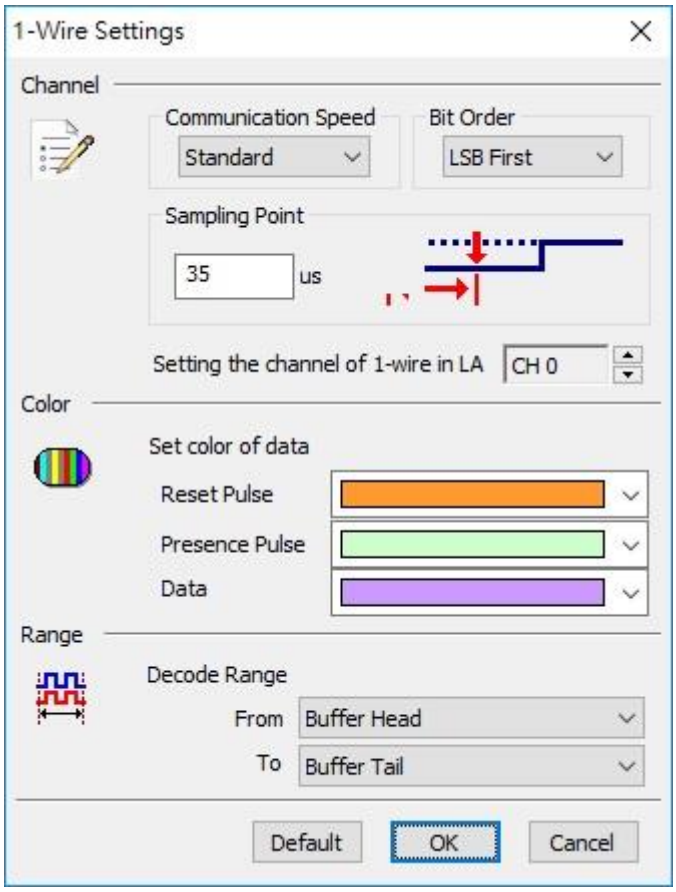
Restore and display the data in the waveform window as percentile or frequency。



1-Wire

The 1-Wire bus has data bits (Reset Pulse, Presence Pulse, Write 1, Write 0, Read 1, Read 0) in standard or overdrive speed as the diagram below.

Settings



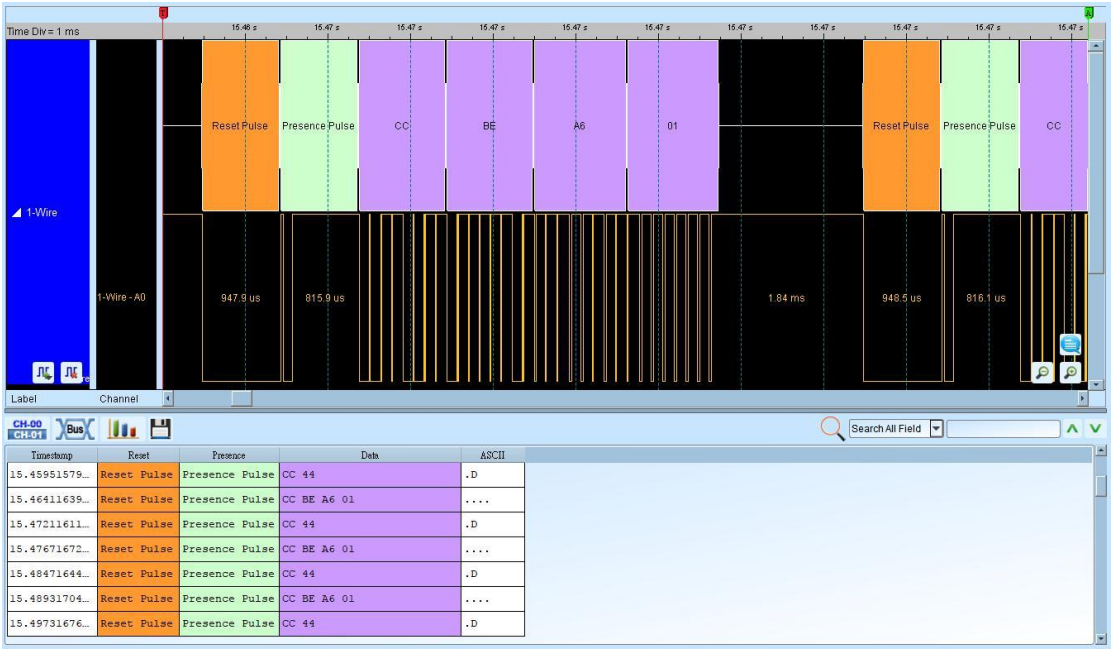
Communication Speed: Standard or overdrive.

Bit Order: LSB first or MSB first.

Sampling point: Set the sampling point N microseconds (us) after the beginning of each data bit.

Result

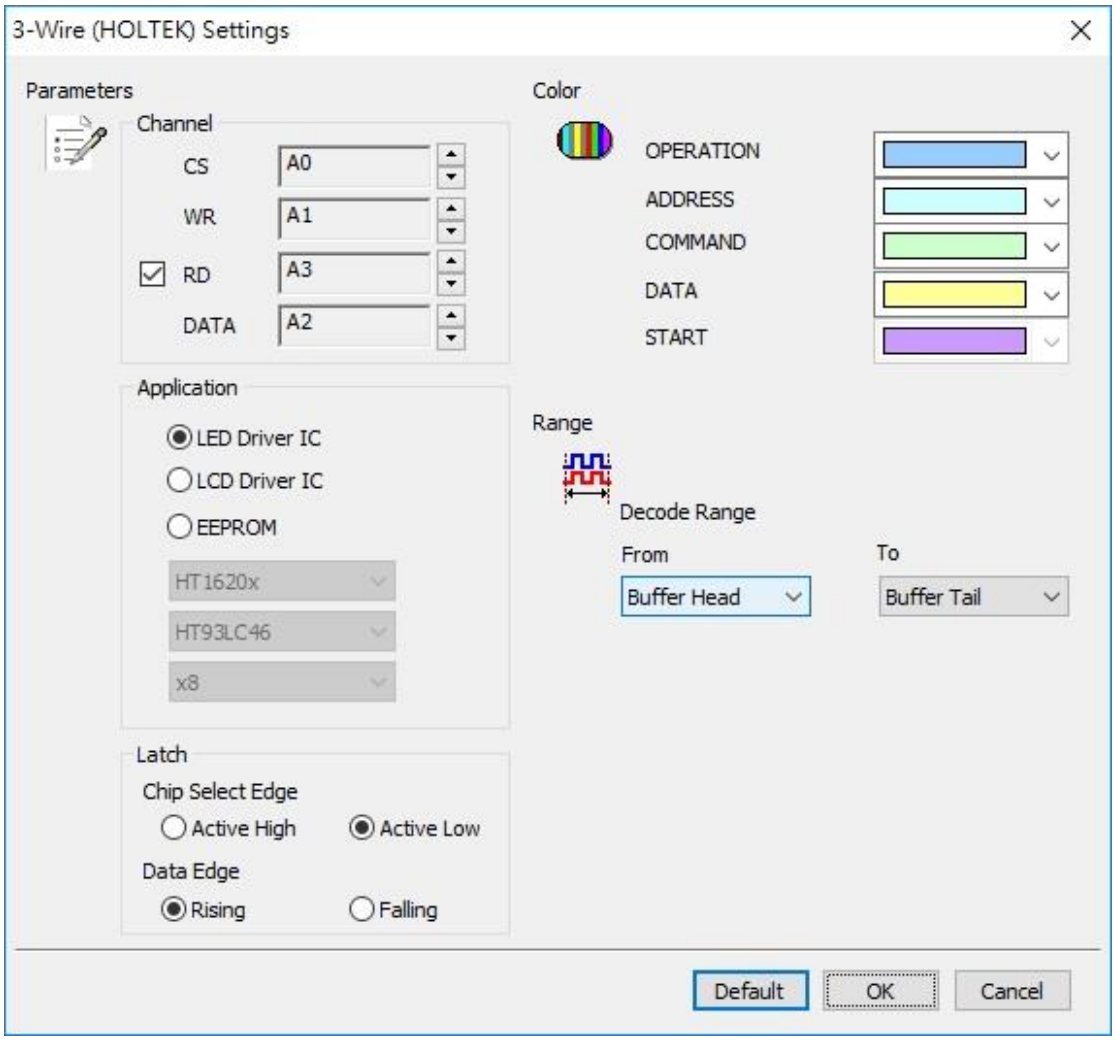
Click OK to run the 1-Wire decode and see the result on the Waveform Window below.



3-Wire

3-Wire protocol is established by HOLTEK SEMICONDUCTOR INC. It's Applied to control LED/LCD driver IC or EEPROM.

Settings



Channel: Show the selected channels (CS:CH0, WR:CH1, DATA:CH2, RD:CH3)

LED Driver IC: Select LED driver IC application.

LCD Driver ID: Select LCD driver IC application.

EEPROM: Select EEPROM application.

Active High: Select Active High.

Active Low: Select low chip select (CS).

Rising: Select Rising Data Edge.

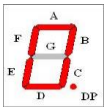
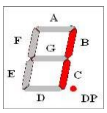
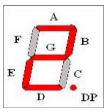
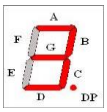
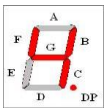
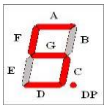
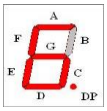
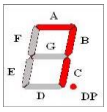
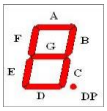
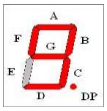
Falling: Select Falling Data Edge.

Result

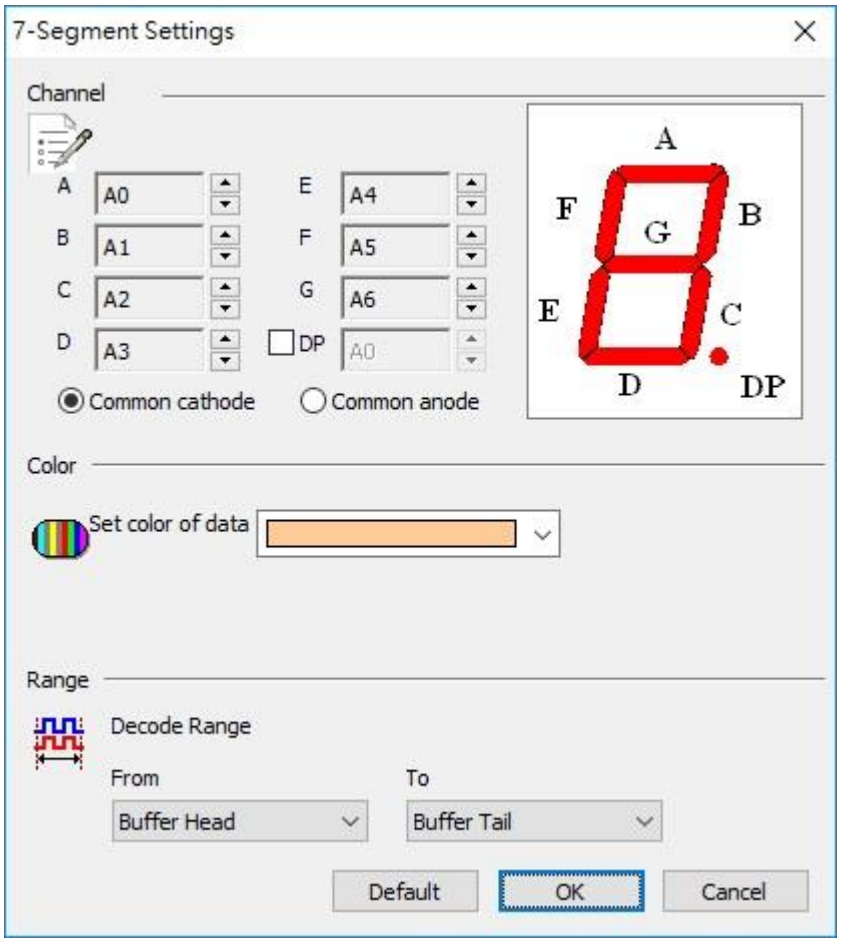
Timestamp	Operation	Command	Address	Data
1.335000000...	5 (WRITE)		00	0
36.11500000...			01	0
46.81500000...			02	0
57.52000000...			03	0
68.22500000...			04	3
78.92500000...			05	7
89.63000000...			06	0

7-Segment

A seven-segment display, is a form of electronic display device for displaying decimal numerals that is an alternative to the more complex dot-matrix displays.

Digit	LED	A	B	C	D	E	F	G
0		**ON**	**ON**	**ON**	**ON**	**ON**	**ON**	OFF
1		OFF	**ON**	**ON**	OFF	OFF	OFF	OFF
2		**ON**	**ON**	OFF	**ON**	**ON**	OFF	**ON**
3		**ON**	**ON**	**ON**	**ON**	OFF	OFF	**ON**
4		OFF	**ON**	**ON**	OFF	OFF	**ON**	**ON**
5		**ON**	OFF	**ON**	**ON**	OFF	**ON**	**ON**
6		**ON**	OFF	**ON**	**ON**	**ON**	**ON**	**ON**
7		**ON**	**ON**	**ON**	OFF	OFF	OFF	OFF
8		**ON**	**ON**	**ON**	**ON**	**ON**	**ON**	**ON**
9		**ON**	**ON**	**ON**	**ON**	OFF	**ON**	**ON**

Settings



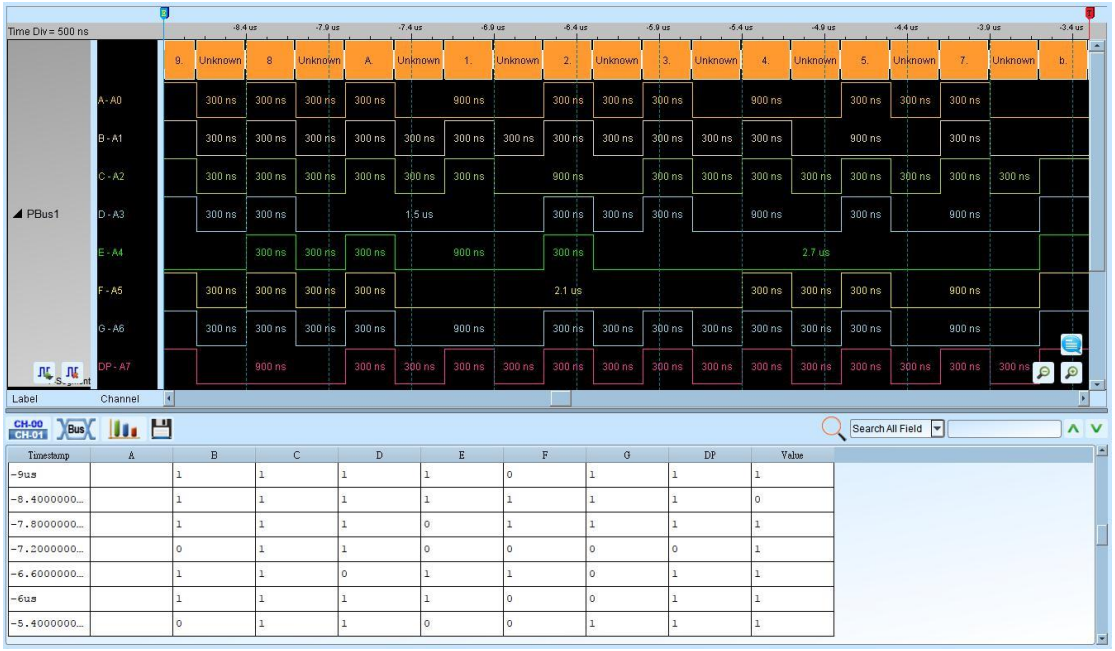
Channel: Show the selected channel (CH 0).

DP: to analysis decimal point.

Common cathode/anode: Show the same cathode or anode.

Result

Click **OK** to run the 7 Segment decode and see the result on the Waveform Window below.

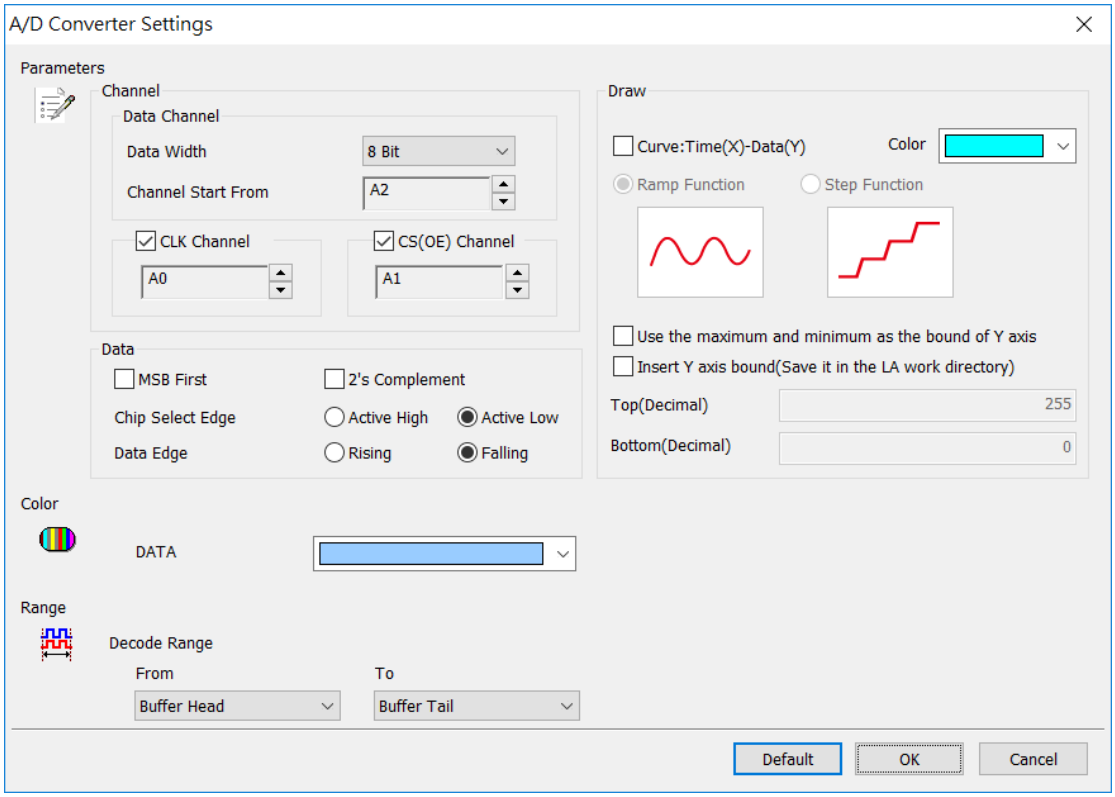


Timestamp	A	B	C	D	E	F	G	DP	Value
-9us		1	1	1	1	0	1	1	1
-8.4000000...		1	1	1	1	1	1	1	0
-7.8000000...		1	1	1	0	1	1	1	1
-7.2000000...		0	1	1	0	0	0	0	1
-6.6000000...		1	1	0	1	1	0	1	1
-6us		1	1	1	1	0	0	1	1
-5.4000000...		0	1	1	0	0	1	1	1

A/D Converter

A/D Converter (Analog-To-Digital Converter), is a device that uses sampling to convert a continuous quantity to a discrete time representation in digital form.

Settings



Data Channel Start From: ADC data channel start from

CLK Channel: ADC clock in channel

CS(OE) Channel: ADC chip select (output enable) channel

Data Width: ADC data width, range: 4Bit ~ 32Bit

MSB First: Data bit starts form MSB; LSB defaulted

2's Complement: Show the 2's complement result.

Chip Select Edge: Set the chip select edge; Active Low defaulted

Data Edge: Set the Data Edge; Falling Edge defaulted

Curve: Time(X)-Data(Y) Show the diagram in form of time as X axis; data as Y axis.

Ramp/Step Function: Select Ramp/Step curve, Ramp Function defaulted

Color: Select the curve color

Use the maximum and minimum as the bound of Y axis: Use the maximum data as the top bound of Y axis and minimum data as the bottom bound of Y axis.

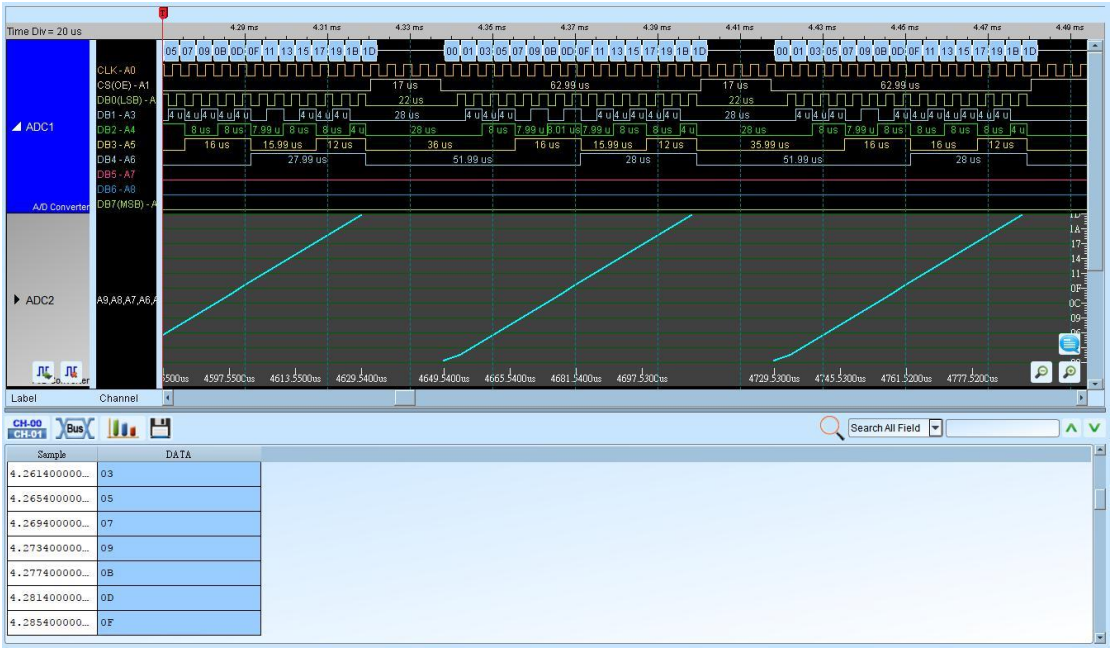
Insert Y axis bound: Set the maximum and minimum bounds of Y axis.

Note: When Insert Y axis boundaries is actived (Save it in the LA file directory), the Top and Bottom values will always be saved as an independent text file named as ADC.txt, different from the waveform file, at file work directory unless a different name is assigned. If you need the specific boundary settings, please save it, so you can reload the settings next time.

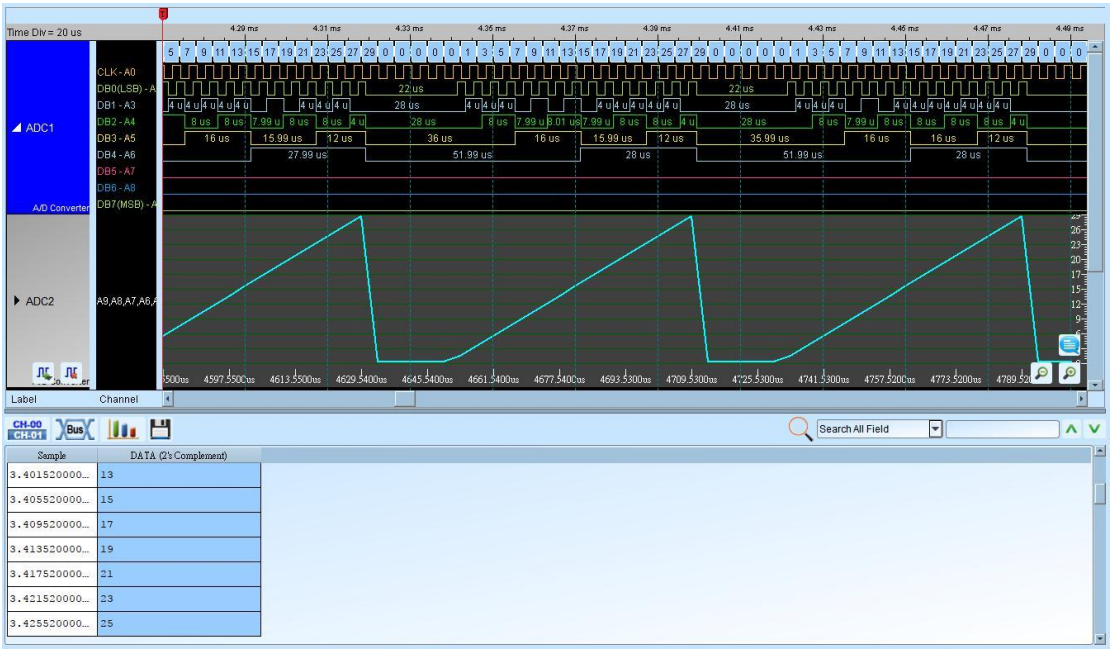
Result

Click **OK** to run the A/D Converter decode and see the result on the Waveform Window below.

Select 8-bit data, CLK/CS channels:



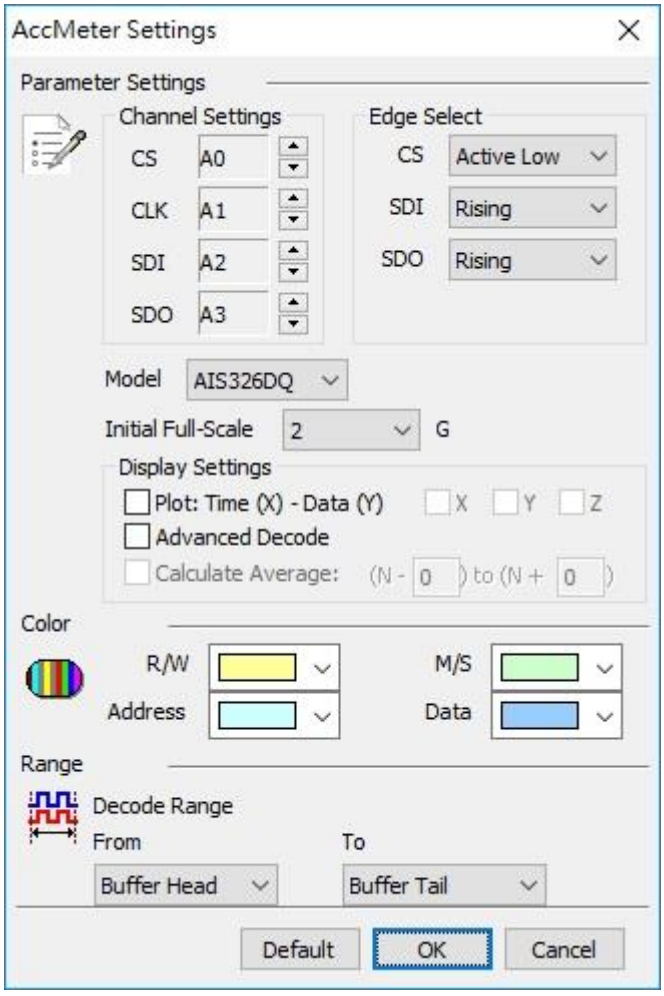
Select 8-bit data:



AcceleroMeter

AcceleroMeter (AccMeter) decoder is the SPI interfaced accelerometer data decoder, which provides bus value to acceleration value conversion and curve drawing function.

Settings



CS: Chip Select, must specified the active state of the CS pin.

CLK: Clock

SDI: Data Input Pin, must specified the data sampling edge.

SDO: Data Output Pin, must specified the data sampling edge.

Model: The IC model of the target accelerometer.

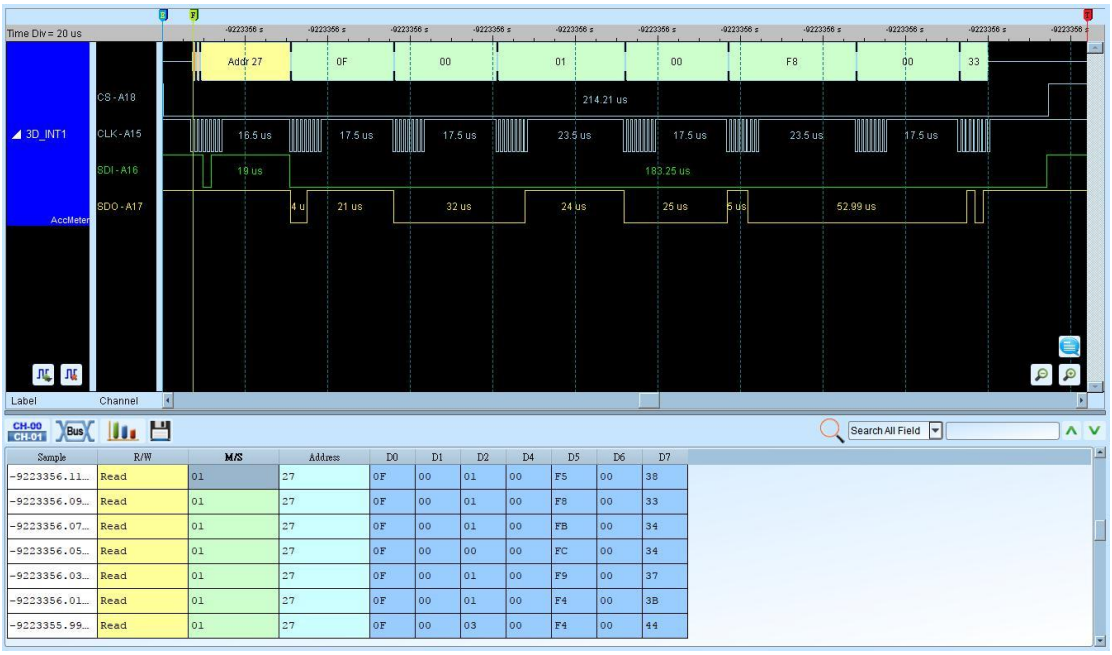
Initial Full-Scale: The default Full-Scale setting.

Plot: Enable/Disable to display the waveform in Time-Value curve.

Advanced Decode: Enable/Disable the address, value convert function.

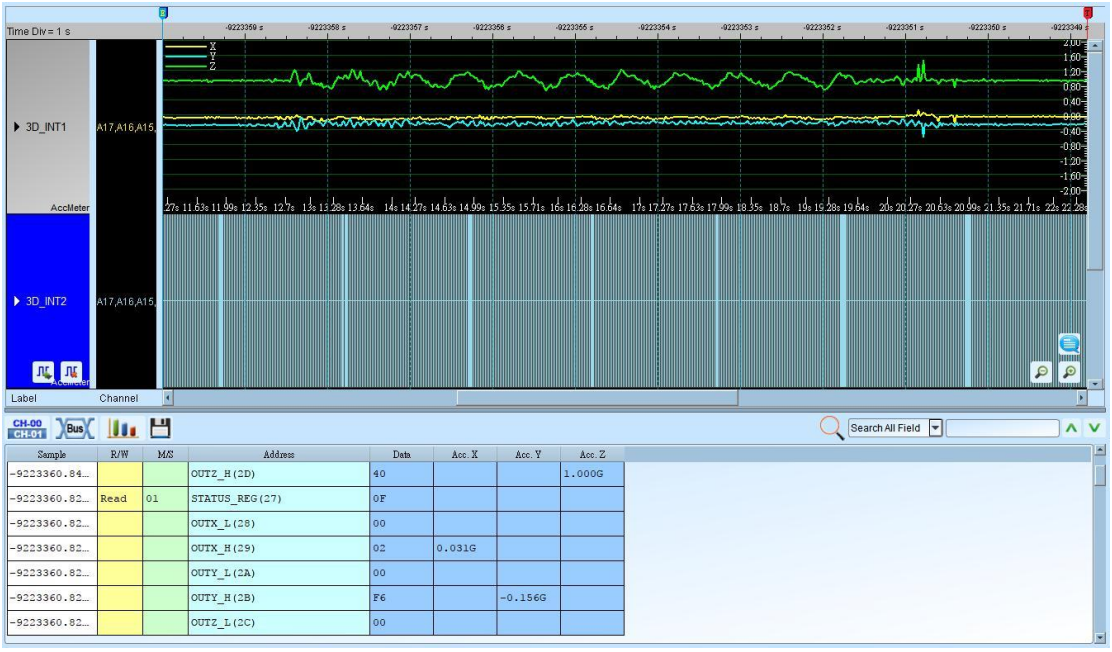
Result

Standard decoder result



Sample	R/W	M/S	Address	D0	D1	D2	D4	D5	D6	D7
-9223356.11...	Read	01	27	0F	00	01	00	F5	00	38
-9223356.09...	Read	01	27	0F	00	01	00	F8	00	33
-9223356.07...	Read	01	27	0F	00	01	00	FB	00	34
-9223356.05...	Read	01	27	0F	00	00	00	FC	00	34
-9223356.03...	Read	01	27	0F	00	01	00	F9	00	37
-9223356.01...	Read	01	27	0F	00	01	00	F4	00	3B
-9223355.99...	Read	01	27	0F	00	03	00	F4	00	44

Advanced decode result + Time-Value curve display

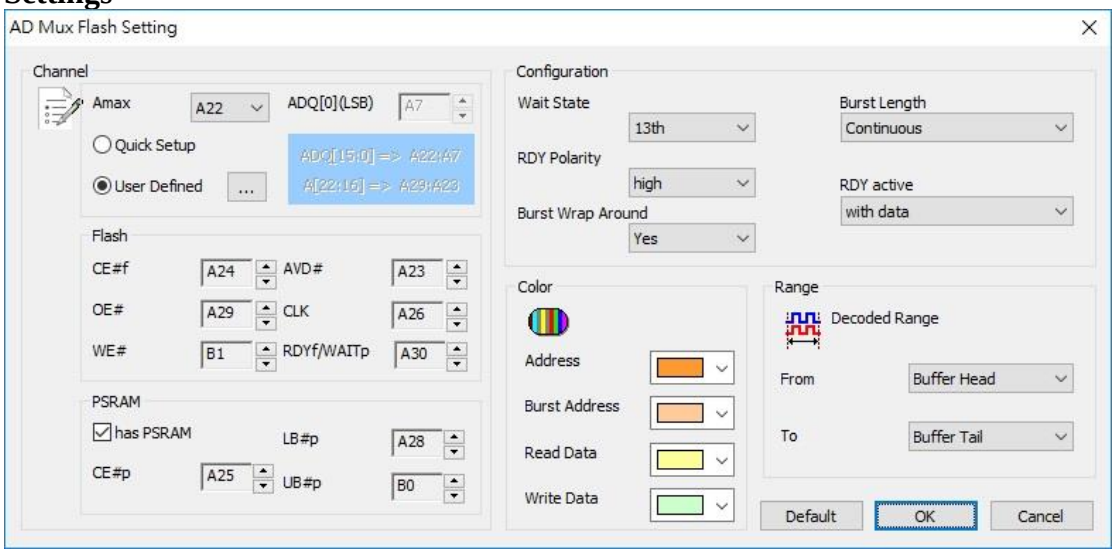


Sample	R/W	M/S	Address	Data	Acc. X	Acc. Y	Acc. Z
-9223360.84...			OUTZ_H(2D)	40			1.000G
-9223360.82...	Read	01	STATUS_REG(27)	0F			
-9223360.82...			OUTX_L(28)	00			
-9223360.82...			OUTX_H(29)	02	0.031G		
-9223360.82...			OUTY_L(2A)	00			
-9223360.82...			OUTY_H(2B)	F6		-0.156G	
-9223360.82...			OUTZ_L(2C)	00			

AD-Mux Flash

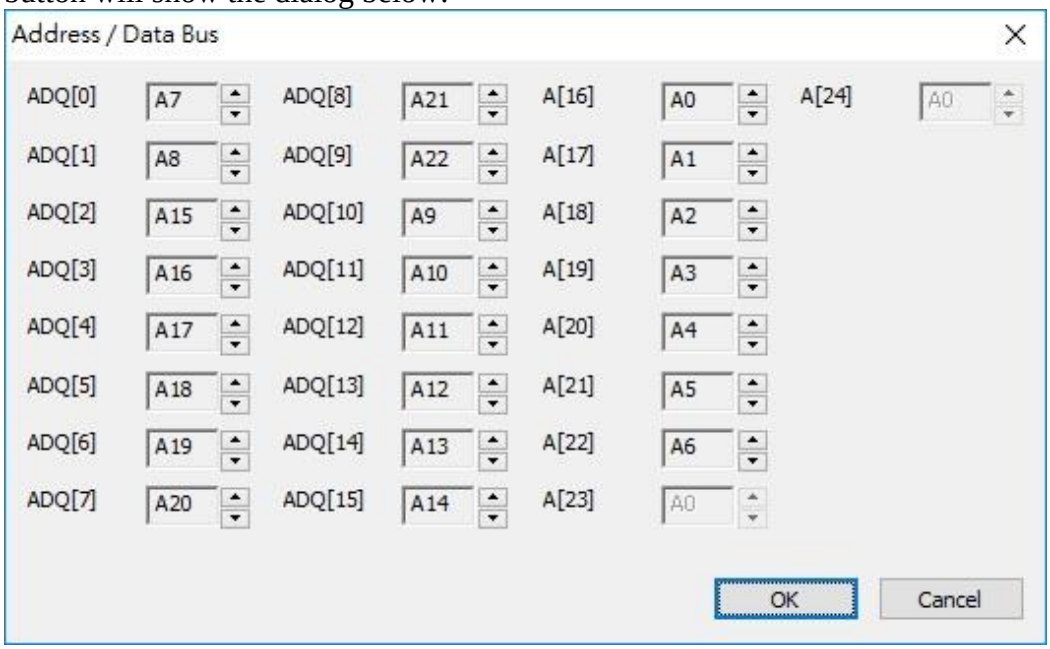
AD-Mux Flash is one kind of parallel flash that utilize an Address and Data multiplexed interface.

Settings



Amax: Setting the number of address pin.

Quick Setup/User Defined: Only set ADQ[0](LSB) when select the Quick Setup, other channels will be set automatically. When check User Defined and press the button will show the dialog below:



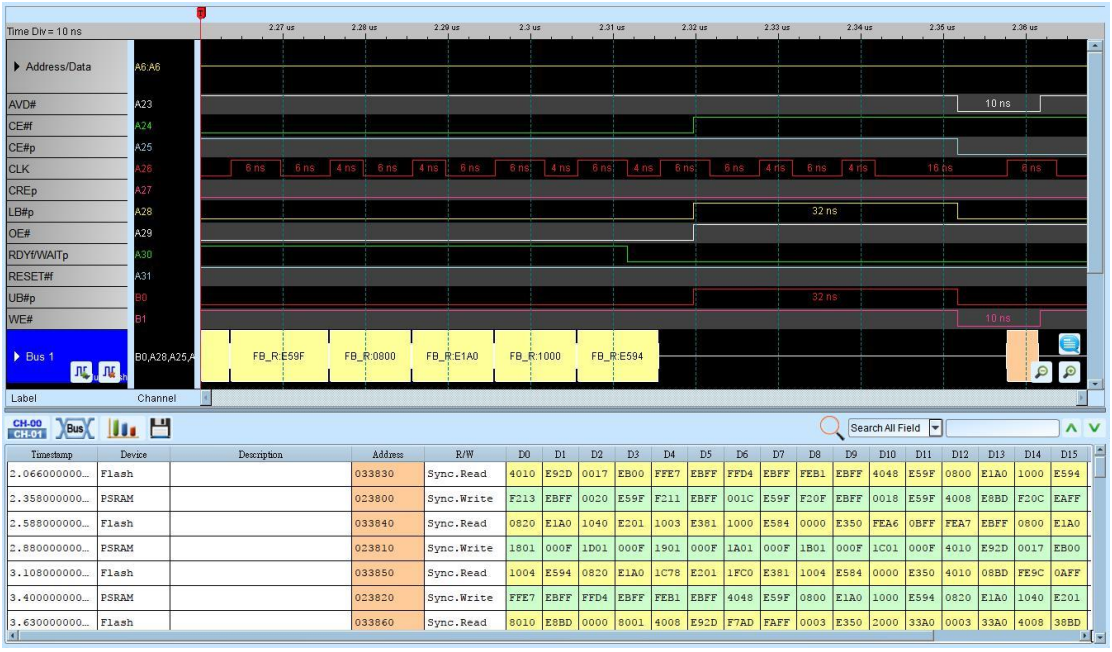
Flash: Control pins of flash.

PSRAM: Control pins of PSRAM. Some MCP include Flash and PSRAM in one package. It will decode PSRAM at the same time when “has PSRAM” is checked.

Configuration: The default setting of configuration register. User must set here to make a correct analysis.

Result

Click OK to run the AD-Mux Flash Decode and see result on the Waveform Windows below.

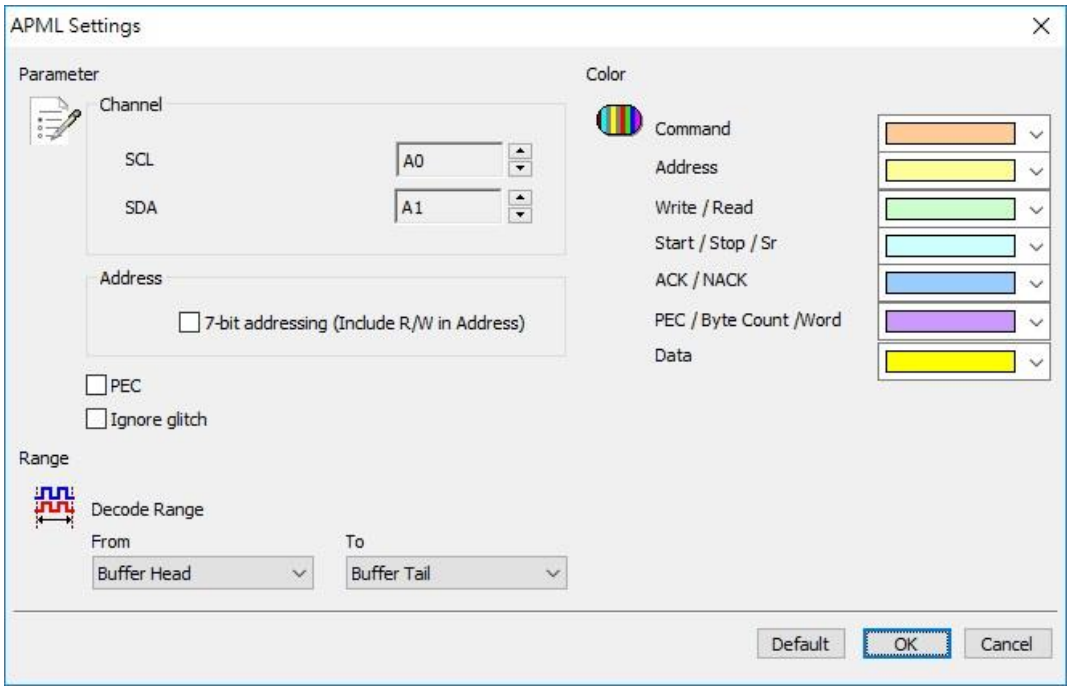


Timestamp	Device	Description	Address	R/W	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
2.066000000...	Flash		033830	Sync.Read	4010	E92D	0017	EB00	FFE7	EBFF	FFD4	EBFF	FEB1	EBFF	4048	E59F	0800	E1A0	1000	E594
2.358000000...	PSRAM		023800	Sync.Write	F213	EBFF	0020	E59F	F211	EBFF	001C	E59F	F20F	EBFF	0018	E59F	4008	E8BD	F20C	EAFF
2.588000000...	Flash		033840	Sync.Read	0820	E1A0	1040	E201	1003	E381	1000	E584	0000	E350	FEA6	0BFF	FEA7	EBFF	0800	E1A0
2.880000000...	PSRAM		023810	Sync.Write	1801	000F	1D01	000F	1901	000F	1A01	000F	1B01	000F	1C01	000F	4010	E92D	0017	EB00
3.108000000...	Flash		033850	Sync.Read	1004	E594	0820	E1A0	1C78	E201	1FC0	E381	1004	E584	0000	E350	4010	08BD	FE9C	0AFF
3.400000000...	PSRAM		023820	Sync.Write	FFE7	EBFF	FFD4	EBFF	FEB1	EBFF	4048	E59F	0800	E1A0	1000	E594	0820	E1A0	1040	E201
3.630000000...	Flash		033860	Sync.Read	8010	E8BD	0000	8001	4008	E92D	F7AD	FAFF	0003	E350	2000	33A0	0003	33A0	4008	38BD

Advanced Platform Management Link (APML)

APML protocol is established by AMD for it's Opteron CPU platform.

Settings



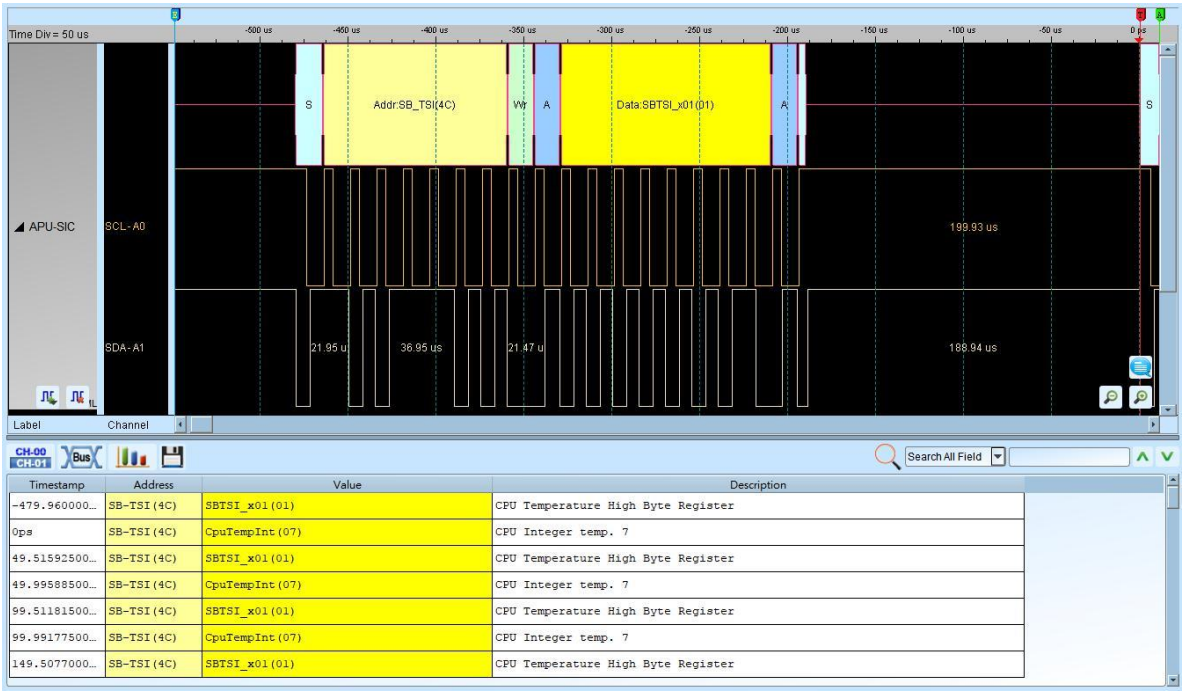
Channel: Show the selected channels (CS:CH0, WR:CH1, DATA:CH2, RD:CH3)

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit R/W).

PEC: Packet Error Check.

Ignore glitch: Ignore the glitch when the slow transitions.

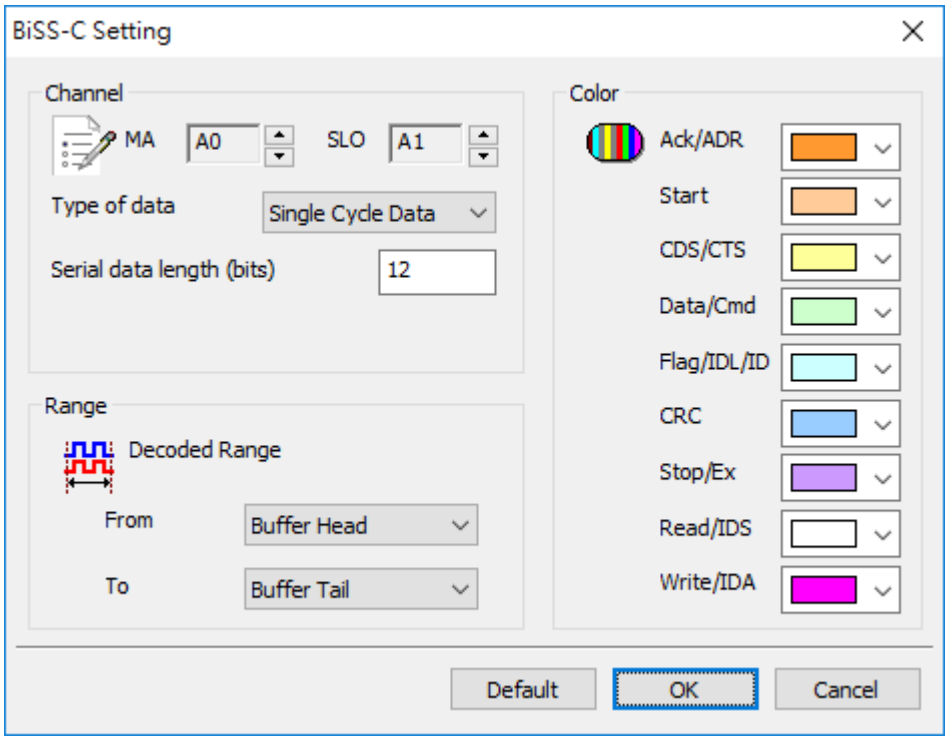
Result



BiSS-C

BiSS-C (Bidirectional Synchronous Serial C-mode) designed by Ic-Haus. The BiSS Interface is based on a protocol which implements a real time interface. It enables a digital, serial and secure communication between controller, sensor and actuator. It is used in industrial applications which require transfer rates, safety, flexibility and a minimized implementation effort.

Settings



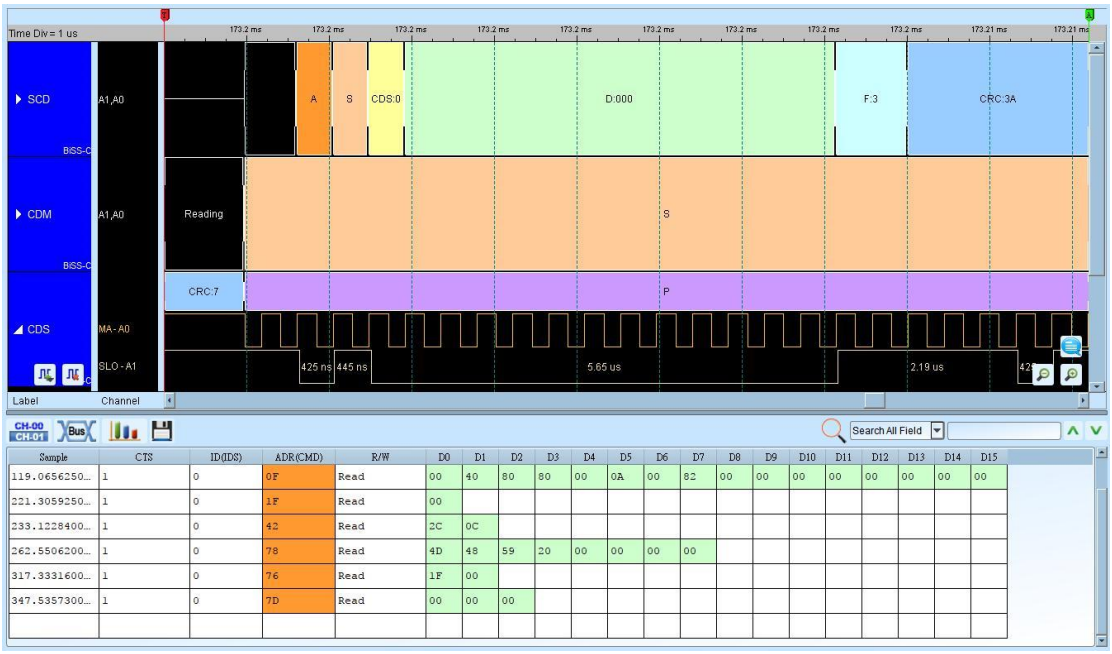
MA/SLO: Setting the channel of MA and SLO.

Type of data: Setting the type you want to decode. It include “Register Data-CDM”, “Register Data-CDS”, “Single Cycle Data”.

Serial data length(bits): Setting the data length when Single Cycle Data mode.

Result

Click OK to run the BiSS-C Decode and see result on the Waveform Windows below.

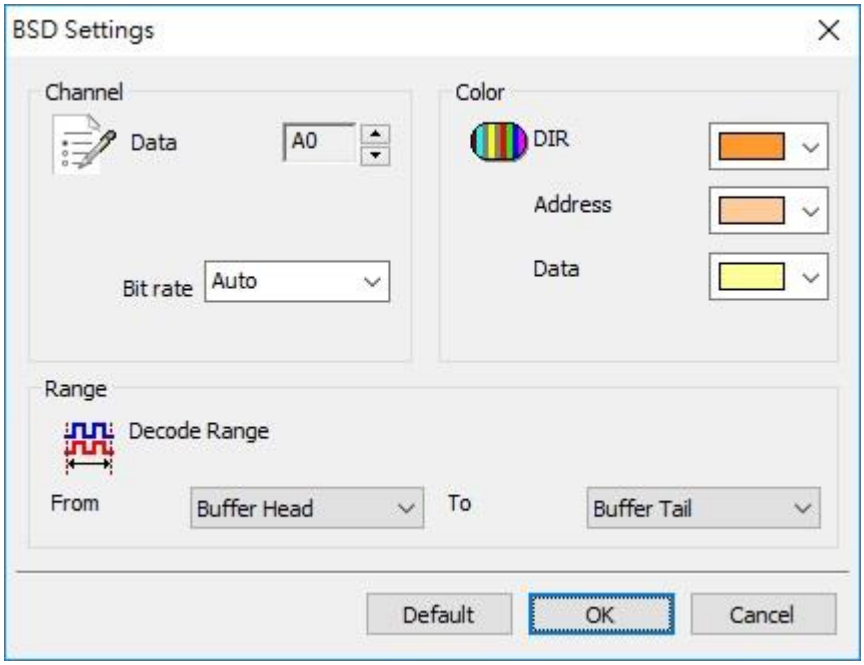


Sample	CTS	ID(IDS)	ADR(CMD)	R/W	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
119.0656250...	1	0	0F	Read	00	40	80	80	00	0A	00	82	00	00	00	00	00	00	00	00
221.3059250...	1	0	1F	Read	00															
233.1228400...	1	0	42	Read	2C	0C														
262.5506200...	1	0	78	Read	4D	48	59	20	00	00	00	00								
317.3331600...	1	0	76	Read	1F	00														
347.5357300...	1	0	7D	Read	00	00	00													

BSD

BSD(Bit Serial Device) is a serial communications protocol for battery monitoring in automotive application.

Settings

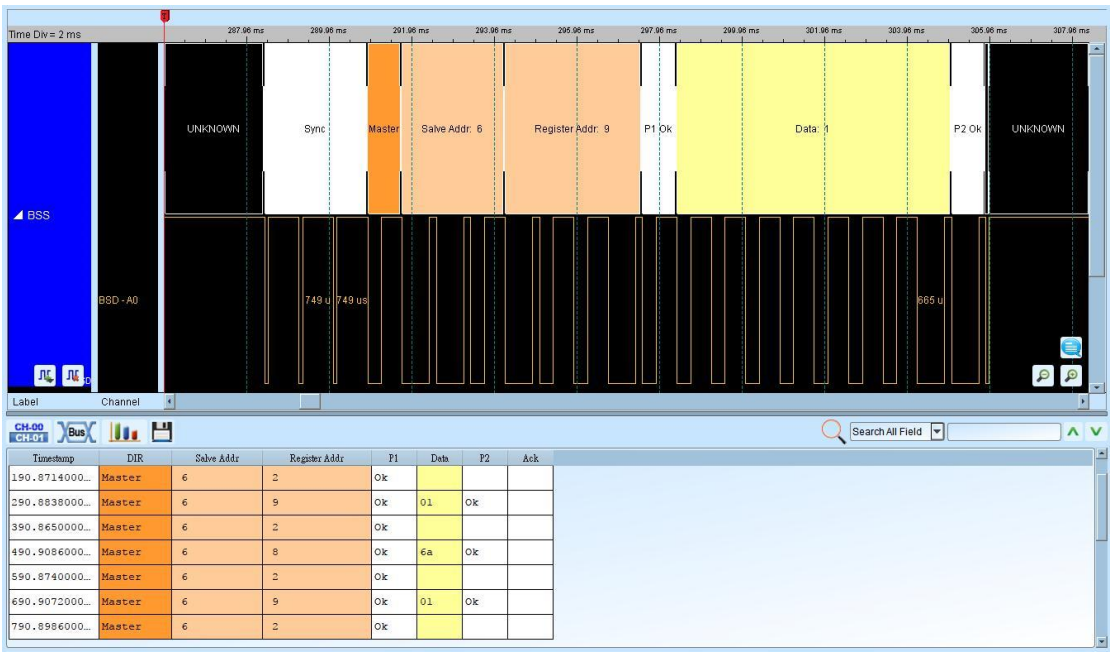


Data: The BSD data.

Bit rate: **T**he bit rate of the BSD data

Result

Click OK to run the BSD Decode and see result on the Waveform Windows below.



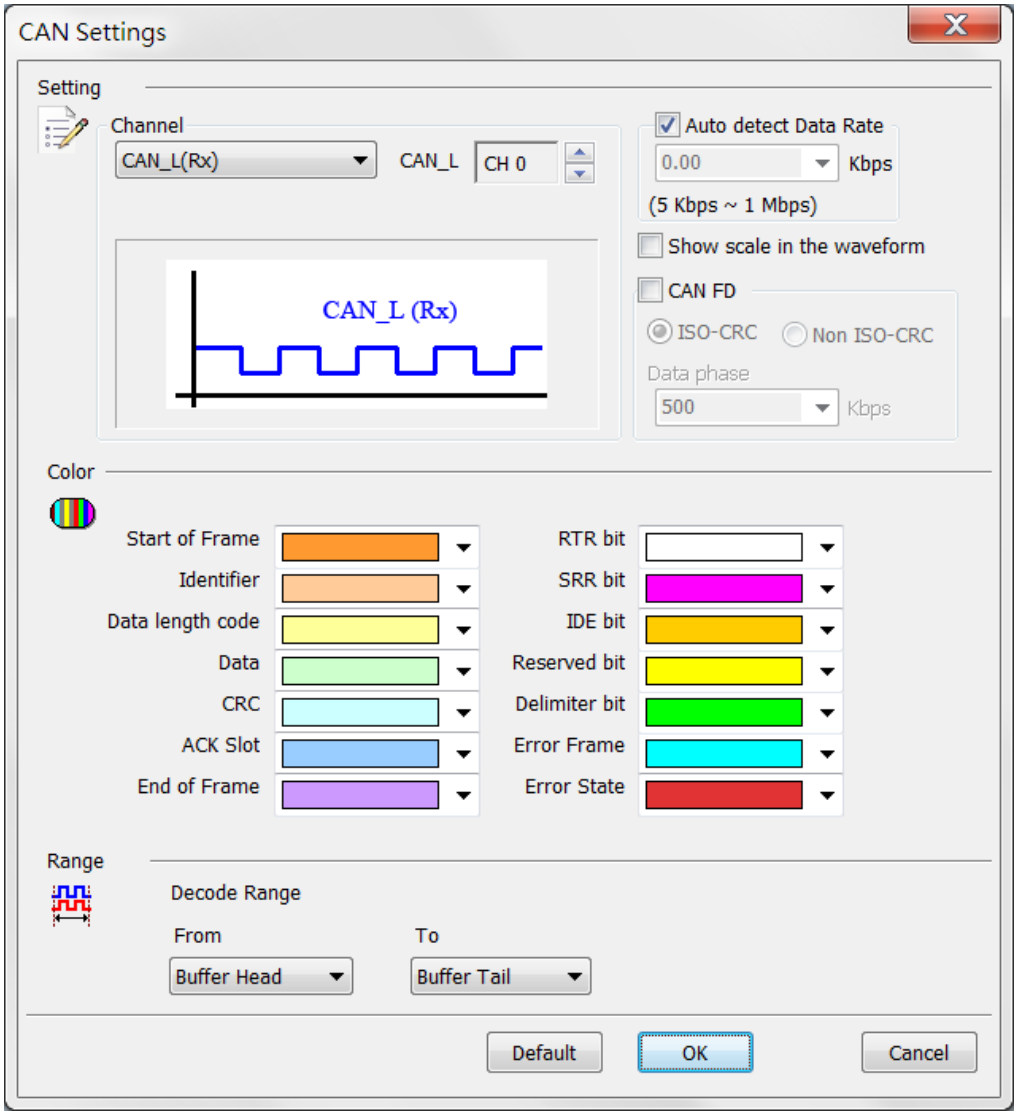
Timestamp	DIR	Salve Addr	Register Addr	P1	Data	P2	Ack
190.8714000...	Master	6	2	Ok			
290.8838000...	Master	6	9	Ok	01	Ok	
390.8650000...	Master	6	2	Ok			
490.9086000...	Master	6	8	Ok	6a	Ok	
590.8740000...	Master	6	2	Ok			
690.9072000...	Master	6	9	Ok	01	Ok	
790.8986000...	Master	6	2	Ok			

CAN 2.0B/ CAN FD

The Controller Area Network (CAN) protocol has version 2.0A (Basic CAN, 11 bits) and version 2.0B (Extended CAN or Peli CAN, 29 bits); both versions have four message types: Data Frame, Remote Frame, Error Frame and Overload Frame as the diagrams below. The CAN Bus has two kinds of data output: CAN High (CAN_H) and CAN Low (CAN_L).

The data rate is flexible in CAN FD (CAN with Flexible Data-Rate). When CAN FD is transferring, it is 64 (bytes/per data) and including CRC17/CRC21.

Settings



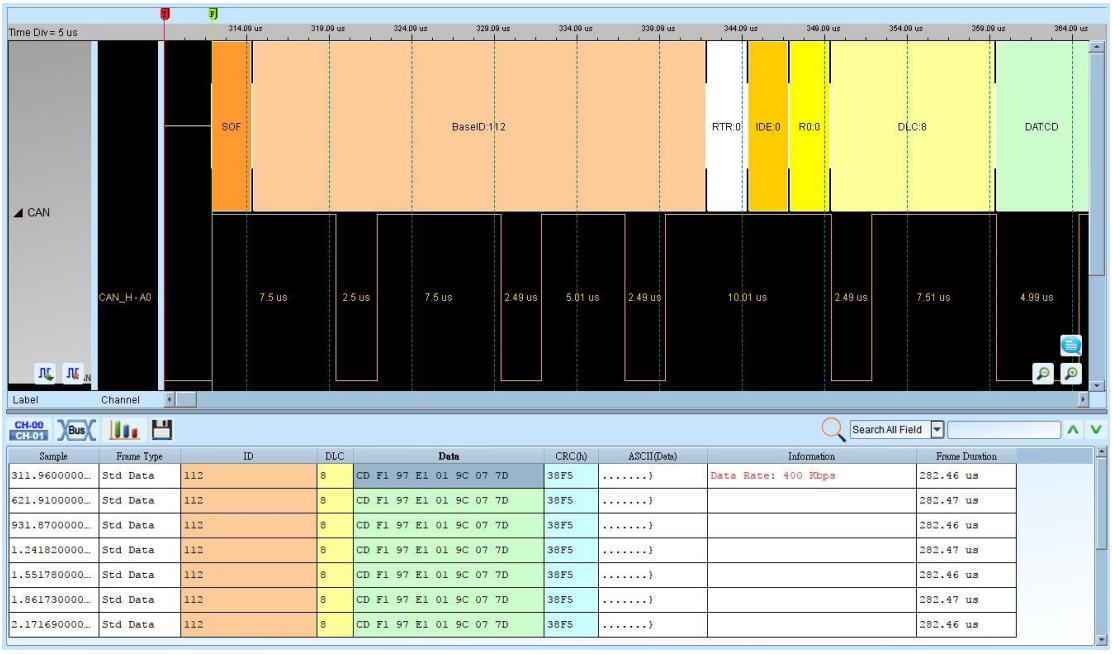
Channel: The differential data from the DSO channel (CAN_H or CAN_L) is shown by default.

Auto detect Data Rate: Check this option for auto-detecting the CAN bit rate by the LA Viewer; this option will be disabled when enabling CAN FD decode, the maximum input range of the Data rate is from 5Kbps-1Mbps.

Show scale in the waveform: Display the scale in the Waveform Window, this option will be disabled when enabling CAN FD decode.

Result

Click **OK** to run the CAN decode and see the result on the Waveform Window below.

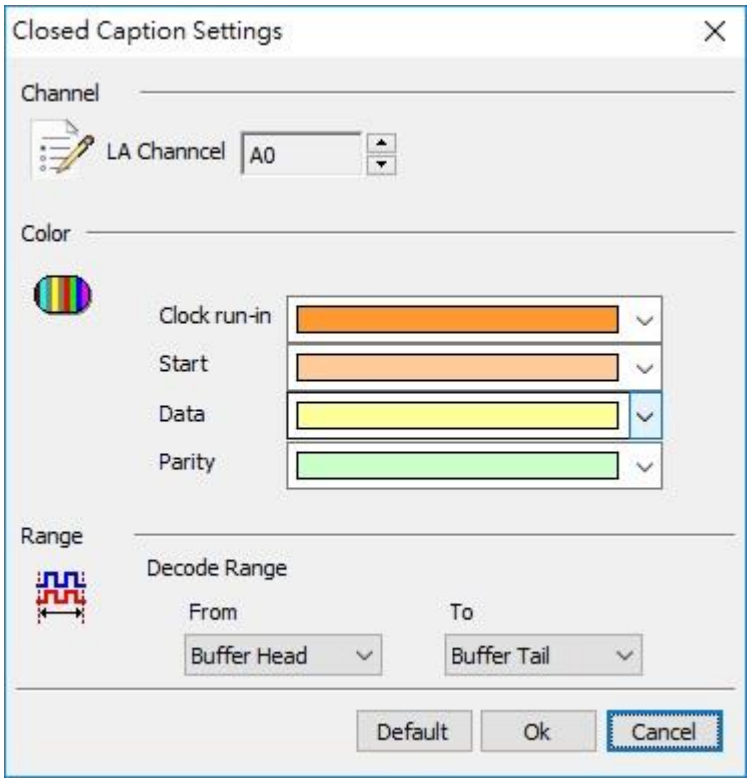


Sample	Frame Type	ID	DLC	Data	CRC(h)	ASCII(Data)	Information	Frame Duration
311.9600000…	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}	Data Rate: 400 Kbps	282.46 us
621.9100000…	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.47 us
931.8700000…	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.46 us
1.241820000…	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.47 us
1.551780000…	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.46 us
1.861730000…	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.47 us
2.171690000…	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.46 us

Closed Caption

Closed captioning is the process of displaying text on a TV or video screen. The text is encoded in the video data stream.

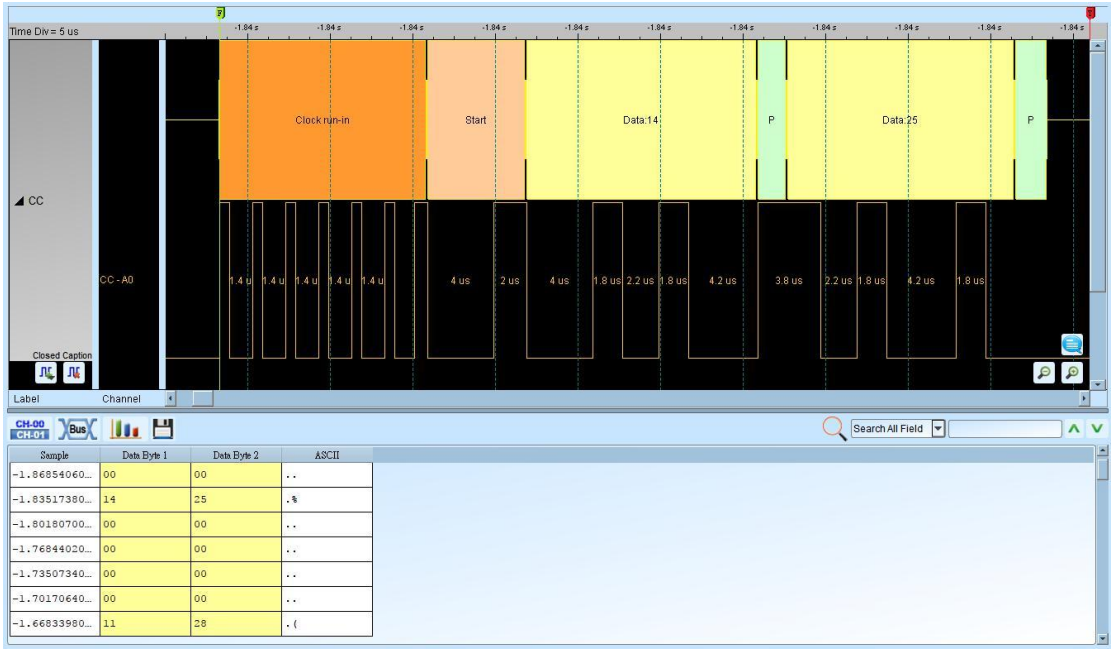
Settings



LA Channel: Show the selected channel (CH0).

Result

Click OK to run the Closed Caption Decode and see result on the Waveform Window below.

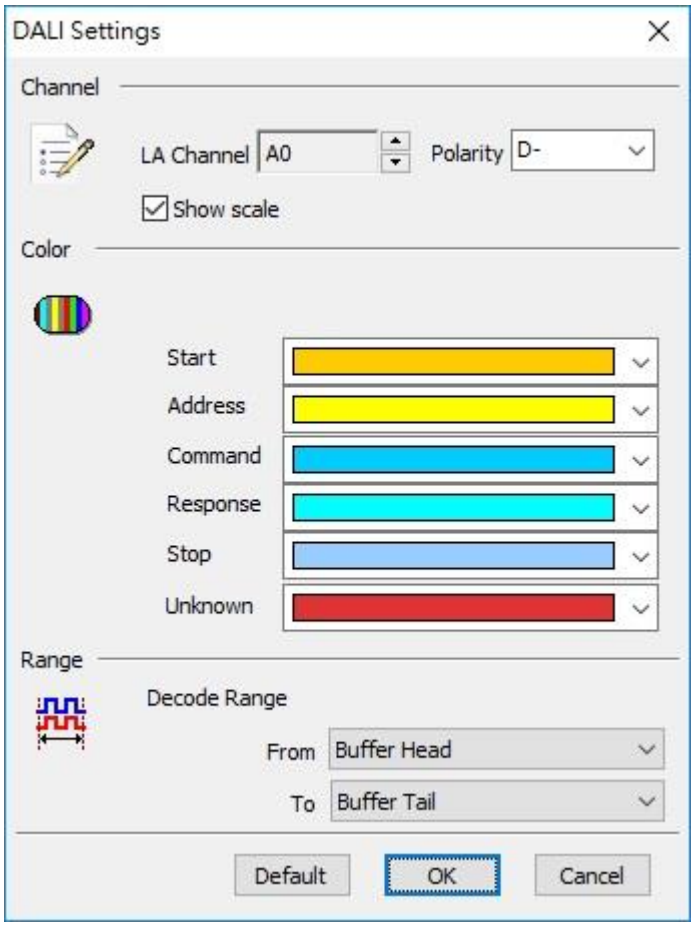


Sample	Data Byte 1	Data Byte 2	ASCII
-1.86854060...	00	00	..
-1.83517380...	14	25	.%
-1.80180700...	00	00	..
-1.76844020...	00	00	..
-1.73507340...	00	00	..
-1.70170640...	00	00	..
-1.66833980...	11	28	.(

DALI

Digital Addressable Lighting Interface (DALI) is a technical standard for network-based systems that control lighting in buildings. The DALI standard, which is specified in the IEC 60929 standard for fluorescent lamp ballasts, encompasses the communications protocol and electrical interface for lighting control networks.

Settings



LA Channel: Show the selected channel (CH0).

Polarity:

D-: Access side of the signal polarity is D-.

D+: Access side of the signal polarity is D+.

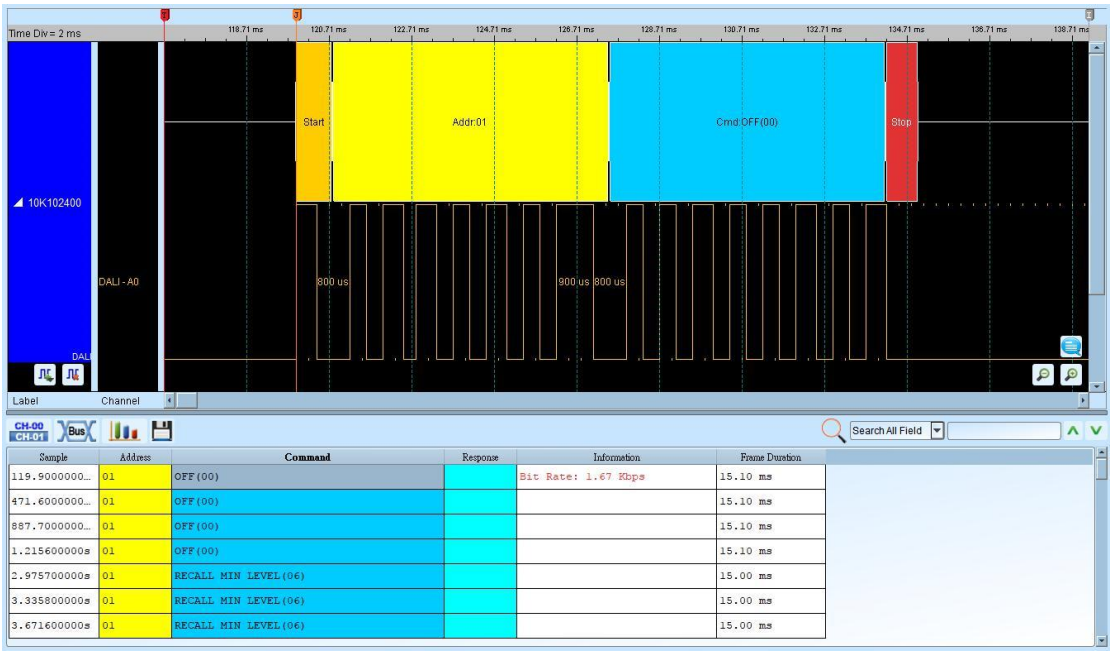
Auto: Automatically detect the polarity of the access end signal.

Show scale: Show Scale on the waveform.

Result

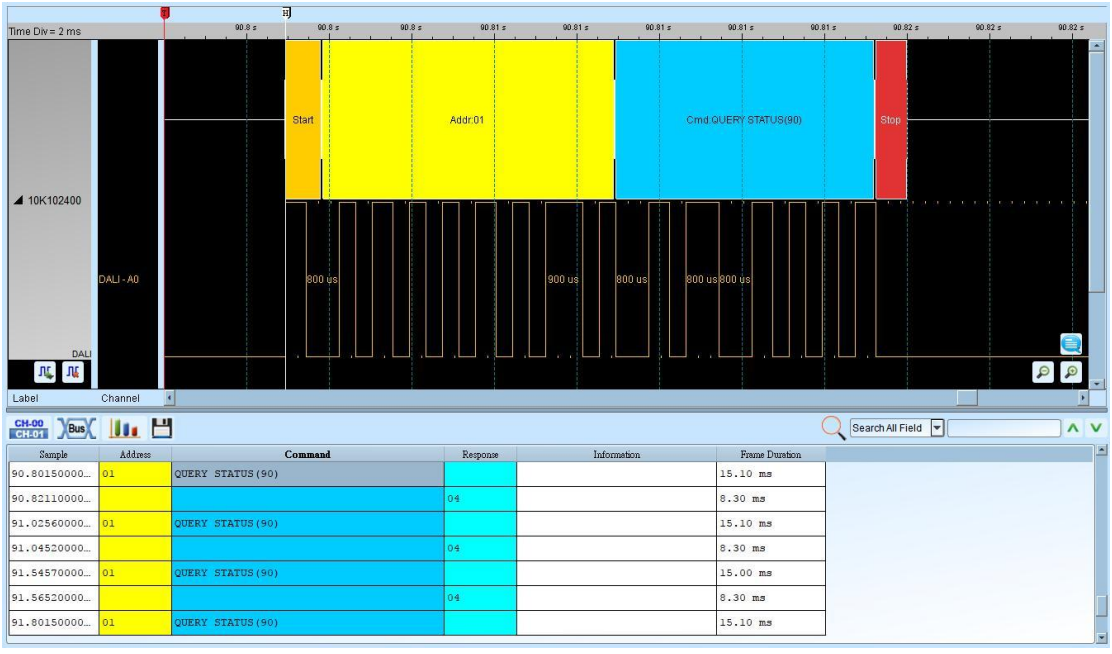
Click OK to run DALI Decode and see result on the Waveform Window below.

Send data



Sample	Address	Command	Response	Information	Frame Duration
119.9000000...	01	OFF(00)		Bit Rate: 1.67 Kbps	15.10 ms
471.6000000...	01	OFF(00)			15.10 ms
887.7000000...	01	OFF(00)			15.10 ms
1.215600000s	01	OFF(00)			15.10 ms
2.975700000s	01	RECALL MIN LEVEL(06)			15.00 ms
3.335800000s	01	RECALL MIN LEVEL(06)			15.00 ms
3.671600000s	01	RECALL MIN LEVEL(06)			15.00 ms

Response data

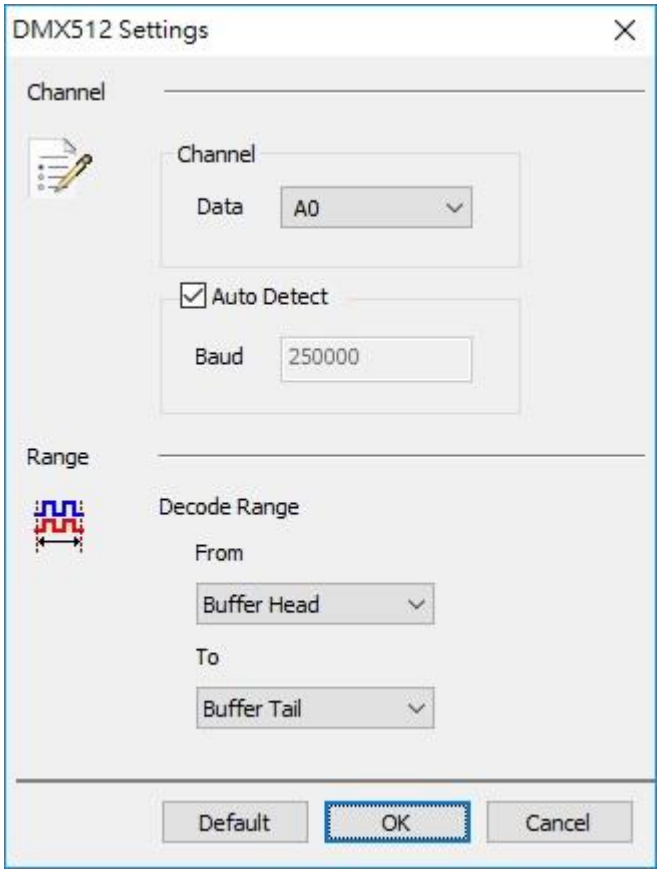


Sample	Address	Command	Response	Information	Frame Duration
90.80150000...	01	QUERY STATUS(90)			15.10 ms
90.82110000...			04		8.30 ms
91.02560000...	01	QUERY STATUS(90)			15.10 ms
91.04520000...			04		8.30 ms
91.54570000...	01	QUERY STATUS(90)			15.00 ms
91.56520000...			04		8.30 ms
91.80150000...	01	QUERY STATUS(90)			15.10 ms

DMX512

DMX512 is a standard for digital communication networks that are commonly used to control stage lighting and effects..

Settings

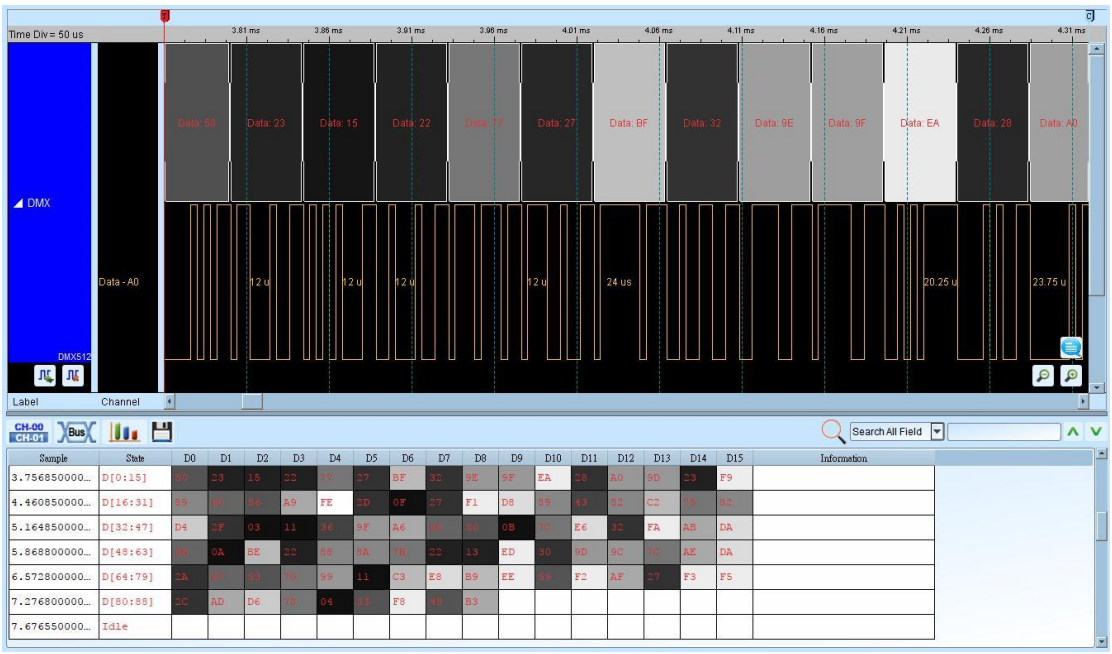


Data: Show the selected channel (CH0).

Auto Detect: Set the Baud Rate manually if not selected.

Result

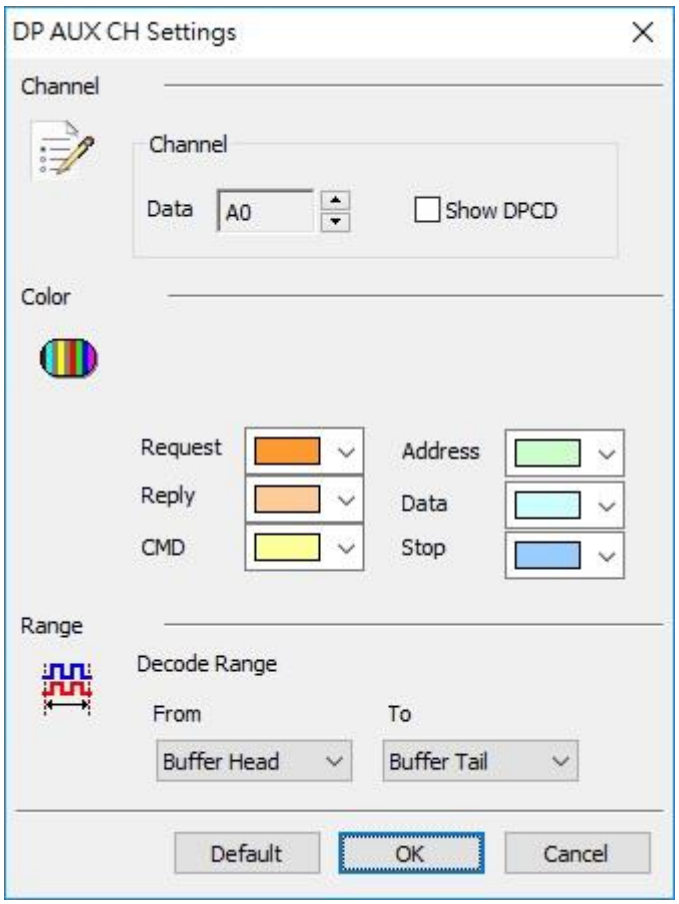
Use grayscale to display the decode results.



Display Port Auxiliary Channel (DP Aux Ch)

The DP Aux Ch is to detect the link, configuration and status of the Display Port source. The Display Port is the digital display interface that is specified in the VESA standard.

Settings

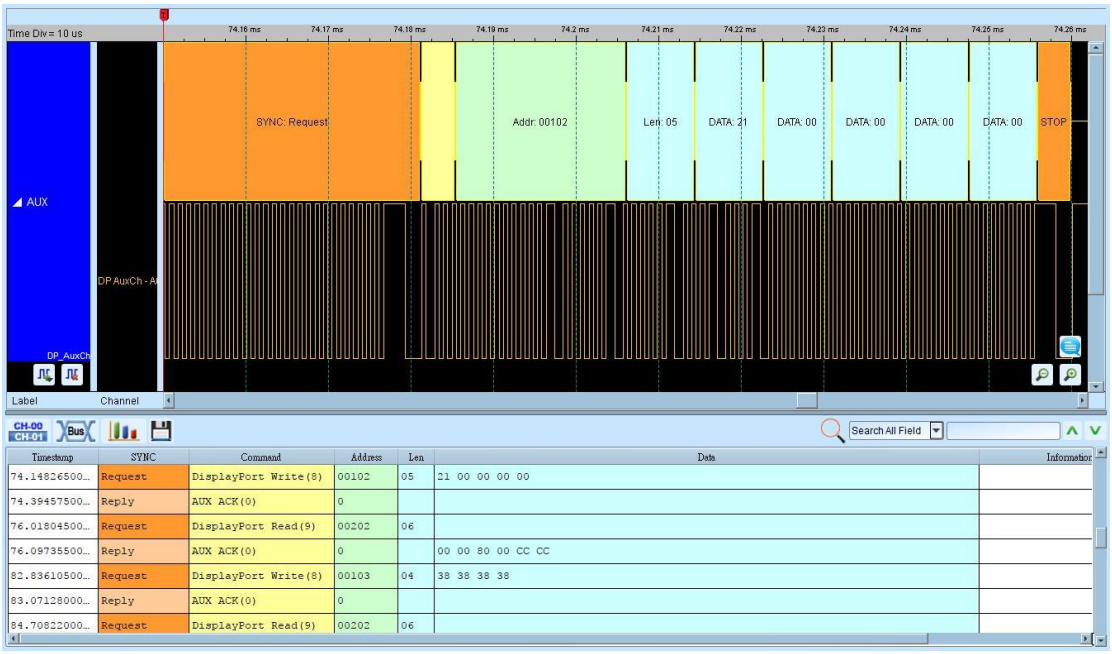


Data: Show the selected channel (CH0).

Show DPCD: Show the Display Port Configuration data.

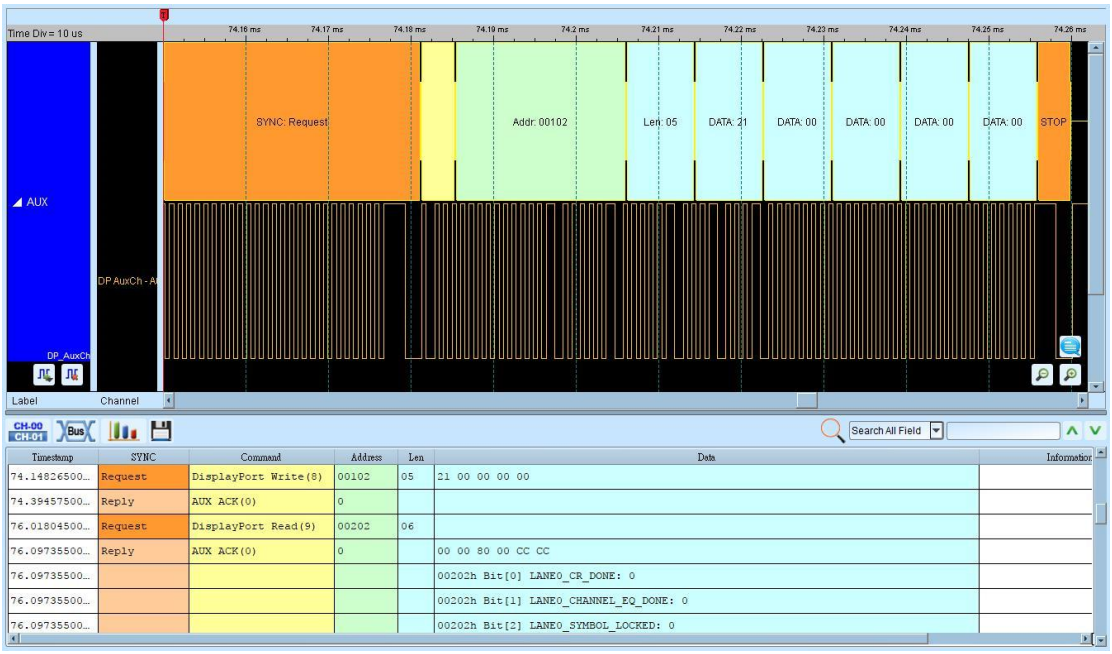
Result

Without the DPCD information



Timestamp	SYNC	Command	Address	Len	Data	Information
74.14826500...	Request	DisplayPort Write(8)	00102	05	21 00 00 00 00	
74.39457500...	Reply	AUX ACK(0)	0			
76.01804500...	Request	DisplayPort Read(9)	00202	06		
76.09735500...	Reply	AUX ACK(0)	0		00 00 80 00 CC CC	
82.83610500...	Request	DisplayPort Write(8)	00103	04	38 38 38 38	
83.07128000...	Reply	AUX ACK(0)	0			
84.70822000...	Request	DisplayPort Read(9)	00202	06		

Show the DPCD information

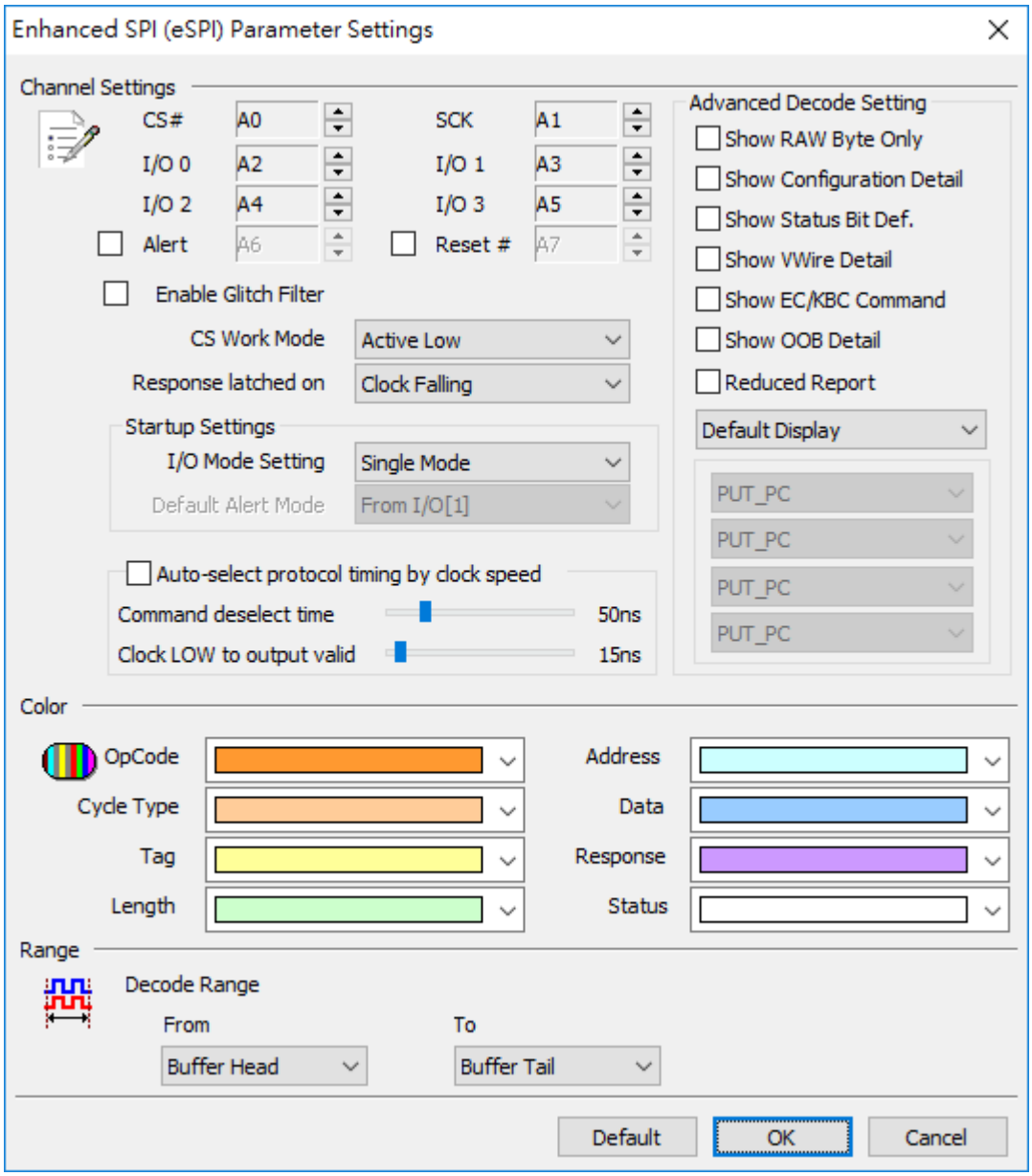


Timestamp	SYNC	Command	Address	Len	Data	Information
74.14826500...	Request	DisplayPort Write(8)	00102	05	21 00 00 00 00	
74.39457500...	Reply	AUX ACK(0)	0			
76.01804500...	Request	DisplayPort Read(9)	00202	06		
76.09735500...	Reply	AUX ACK(0)	0		00 00 80 00 CC CC	
76.09735500...					00202h Bit[0] LANE0_CR_DONE: 0	
76.09735500...					00202h Bit[1] LANE0_CHANNEL_EQ_DONE: 0	
76.09735500...					00202h Bit[2] LANE0_SYMBOL_LOCKED: 0	

Enhanced Serial Peripheral Interface (eSPI)

eSPI is the transmission protocol used in new generation baseboard of Intel, and its specification is to integrate SMBus / LPC / SPI Flash interface to simplify bus and increase transmission efficiency. Source of specification is based on Enhanced Serial Peripheral Interface (eSPI) Interface Base Specification (for Client and Server Platforms) June 2013, Revision 0.75.

Settings



Channel:

CS#:	Chip Select (Active Low)
SCK:	Clock
I/O0 – I/O3:	Data input / output
Alert:	Alert signal (Optional)
Reset:	Reset signal (Optional)

Startup Settings:

I/O Mode Setting: Set the initial I / O state to be Single / Dual / Quad, and I / O state would be switched automatically by the content of the waveform.

Default Alert Mode: Set the channel of Alert signal.

Command deselect time: Set tSHSL, Chip Select# Deassertion Time.

Clock LOW to output valid: Set tCLQV, Output Data Valid Time.

Advanced Decode Setting:

Show Configuration Detail: Show details of SET_CONFIG / GET_CONFIG.

Show Status Bit Def.: Show details of Status.

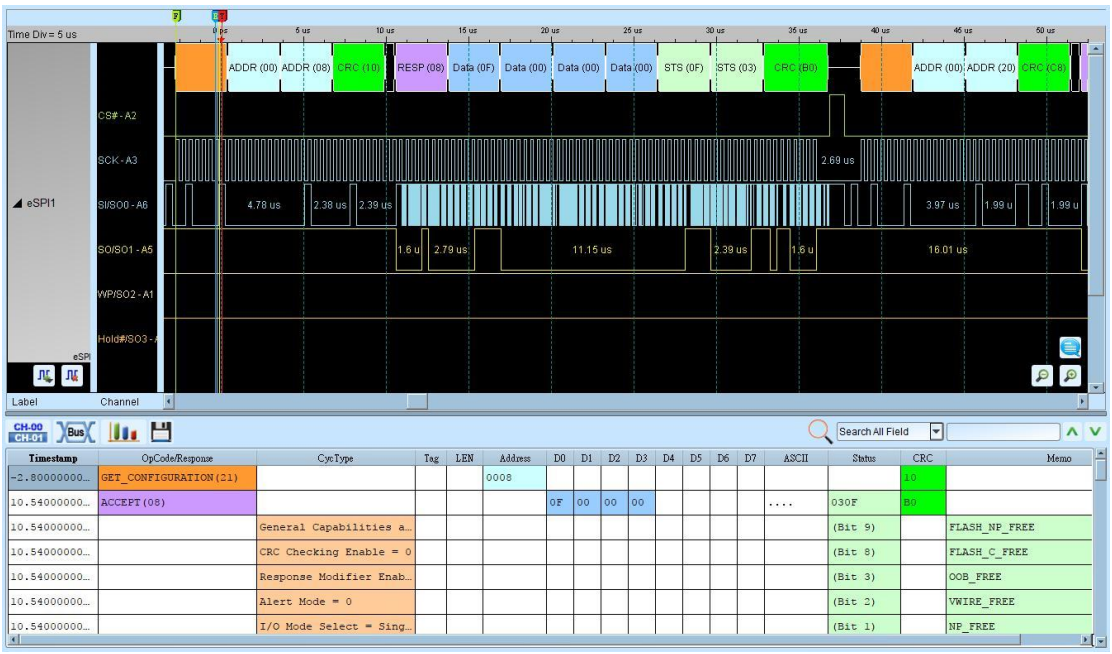
Reduced Report: Reducing the report is easy to check the Command Flow.

Filter Setting: To show or hide the specific OP Code / Cycle Type or Address range in the report.

Note: The setting of Address Filter would be saved as LA\eSPI\eSPIFilterX.bin in the work directory.

Result

Click **OK** to run the eSPI decode and see the result on the Waveform Window below.



Timestamp	OpCode/Response	CycType	Tag	LEN	Address	D0	D1	D2	D3	D4	D5	D6	D7	ASCII	Status	CRC	Memo
-2.80000000...	GET_CONFIGURATION(21)				0008											10	
10.54000000...	ACCEPT(08)					0F	00	00	00					....	030F	B0	
10.54000000...		General Capabilities a...													(Bit 9)		FLASH_NP_FREE
10.54000000...		CRC Checking Enable = 0													(Bit 8)		FLASH_C_FREE
10.54000000...		Response Modifier Enab...													(Bit 3)		OOB_FREE
10.54000000...		Alert Mode = 0													(Bit 2)		VWIRE_FREE
10.54000000...		I/O Mode Select = Sing...													(Bit 1)		NP_FREE

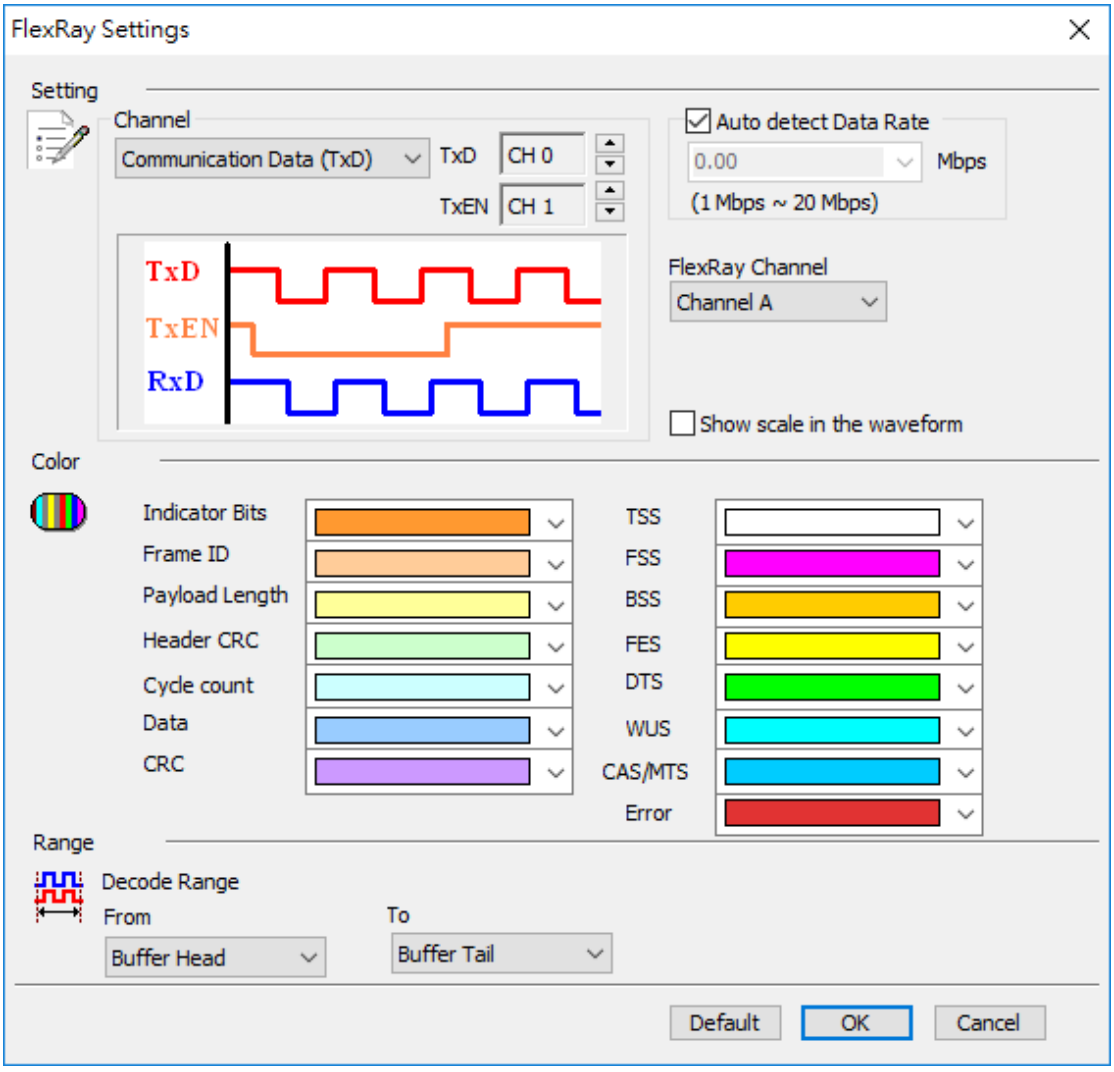
FlexRay

The FlexRay protocol has 2 bits with timing at 10Mbps.

FlexRay signal

Communication Data Layer: The FlexRay communication data is either at transmitter (Txd) or receiver (Rxd) of the FlexRay transceiver. You may set the threshold according to the FlexRay transceiver voltage.

Settings



Channel: Display the channel, Physical Layer is the default.

Communication Data (TxD): The TxD data is from the TxD and TxEN of the FlexRay transceiver.

Communication Data (RxD): The RxD data is from the RxD and RxEN of the FlexRay transceiver.

Auto detect Data Rate: Default is Auto Bit Rate. If disabled, you may use built-in Bit Rate 10/5/2.5 Mbps or input manually, ranges from 1Mbps-20Mbps.

FlexRay Channel: Channel A or B, for Frame CRC checking.

Errors are:

Error	Description
TSS Error	Unable to detect TSS
FSS Error	Unable to detect FSS
BSS Error	Unable to detect BSS
FES Error	Unable to detect FES
Header CRC Error	The header CRC value is incorrect
Frame CRC Error	The frame CRC value is incorrect

Abbreviations are:

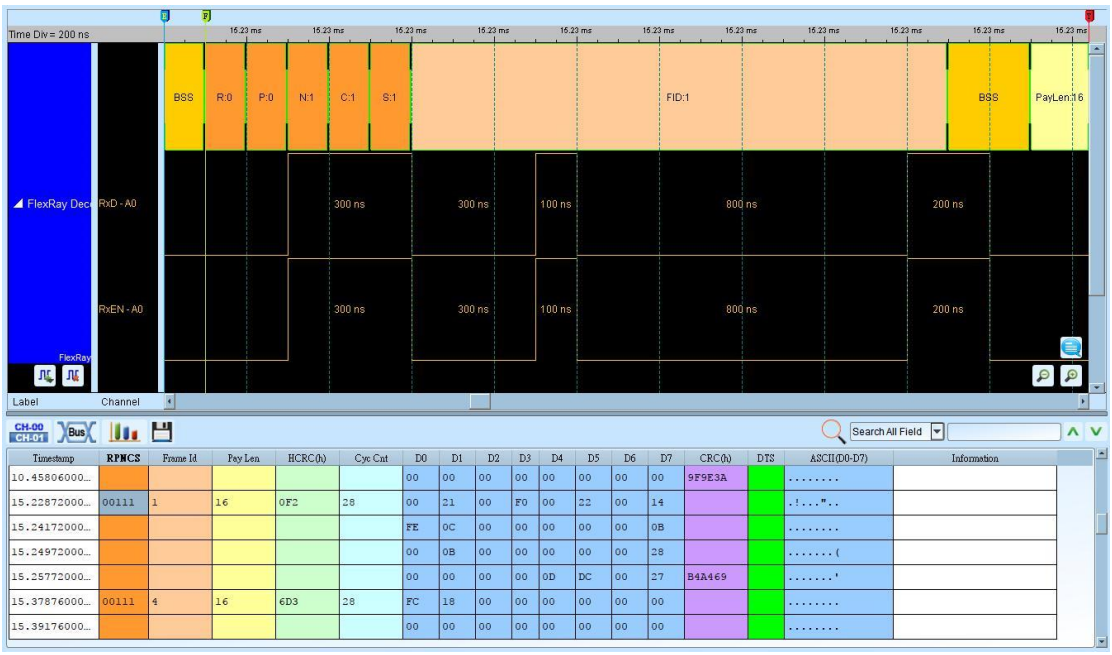
Abbreviation	Description
TSS	Transmission start sequence
FSS	Frame start sequence
BSS	Byte start sequence
FES	Frame end sequence
DTS	Dynamic trailing sequence
CAS	Collision Avoidance Symbol
MTS	Media Access Test Symbol

WUP	Wakeup Pattern
CID	Channel Idle Delimiter

Result

Click **OK** to run the FlexRay decode and see the result on the Waveform Window below.

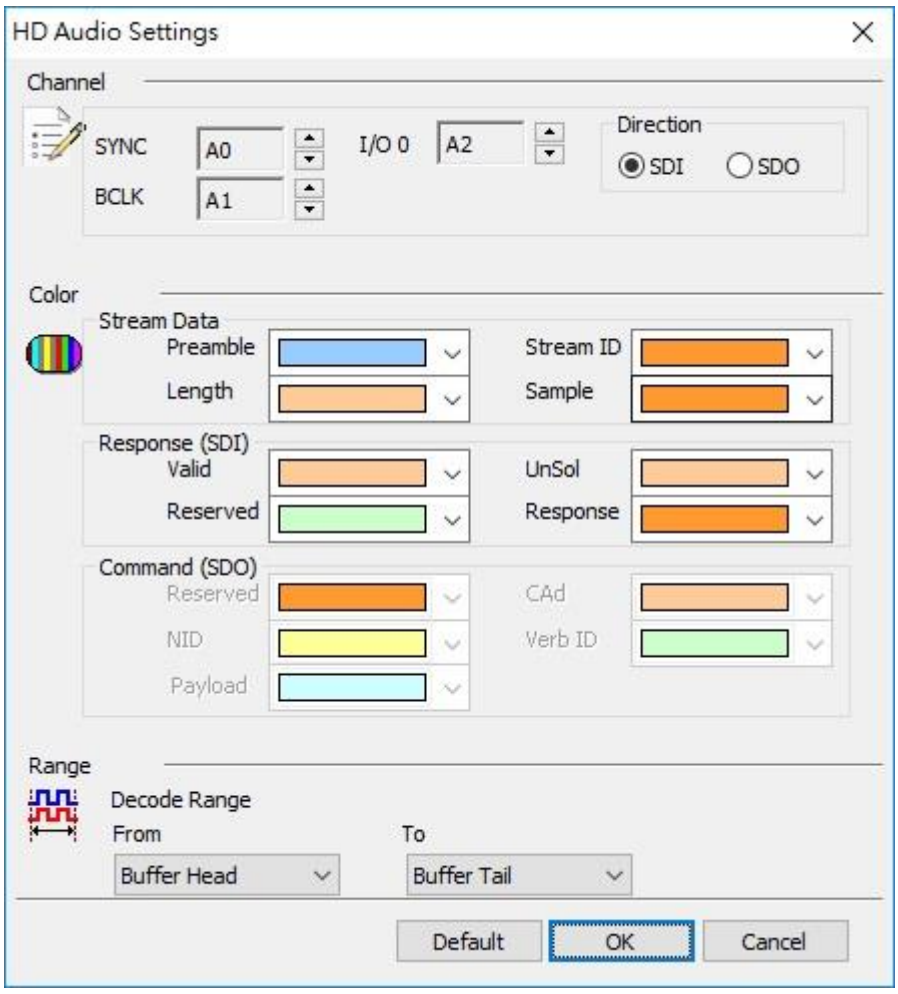
10Mbps FlexRay Communication Data(RxD)



HD Audio

High Definition Audio, also known as HD Audio or by its codename, Azalia, is an audio standard created by Intel to be used on their chipsets, i.e., it is a standard for high-quality on-board audio. In this tutorial we will explain more about this feature.

Settings

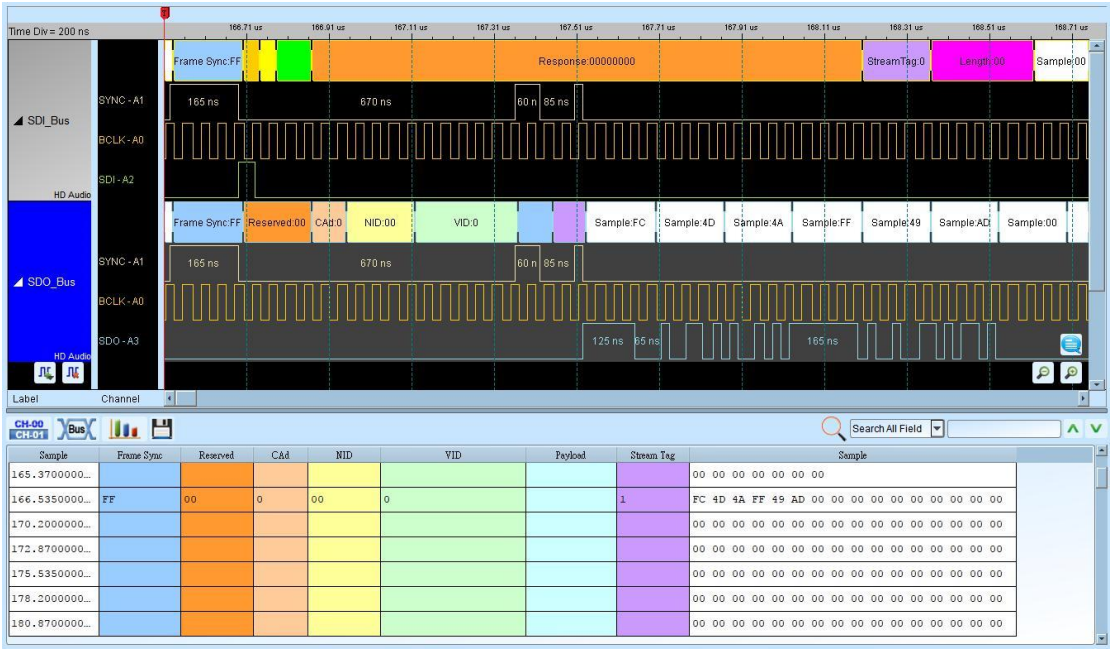


Channel: Show the selected channel (CH 0-CH3).

Direction: Show the data with SDI or SDO decoding.

Result

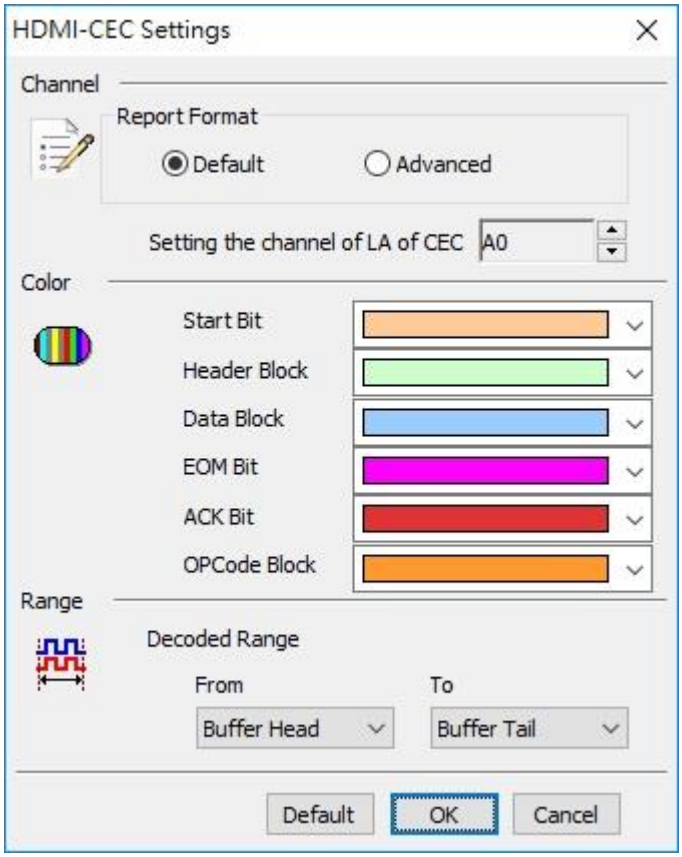
Click **OK** to run the HD Audio decode and see the result on the Waveform Window below.



HDMI-CEC

The HDMI-CEC bus is a one-wire, “party line” that connects up to ten (10) AV devices through standard HDMI cabling. The CEC protocol includes automatic mechanisms for physical address (topology) discovery, (product type based) logical addressing, arbitration, retransmission, broadcasting, and routing control. Message opcodes support both device specific (e.g. set-top-box, DTV, and player) and general features (e.g. for power, signal routing, remote control pass-through, and on-screen display).

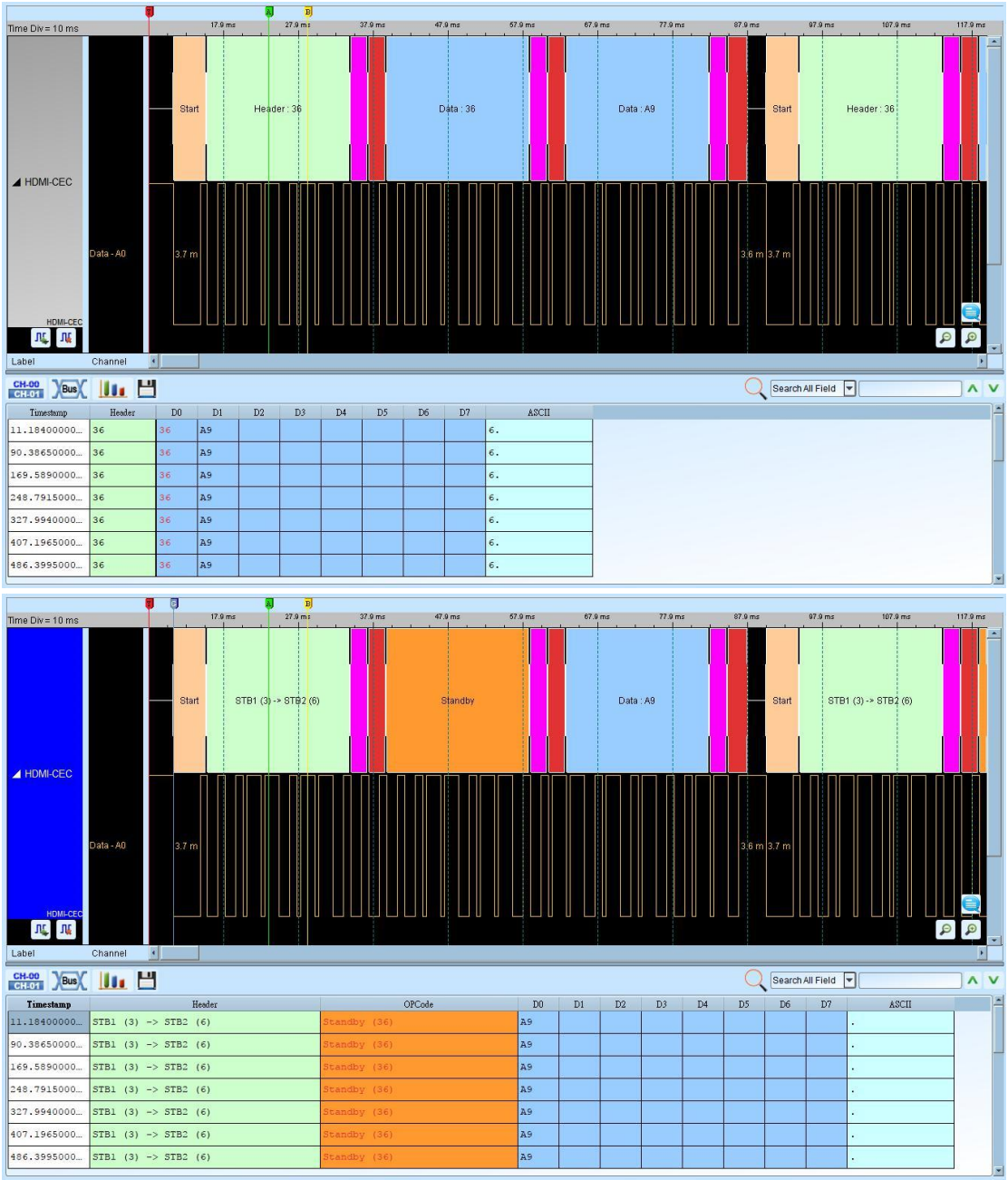
Settings



Latch data: Nominal (1.05 micro seconds) or User Define.

Result

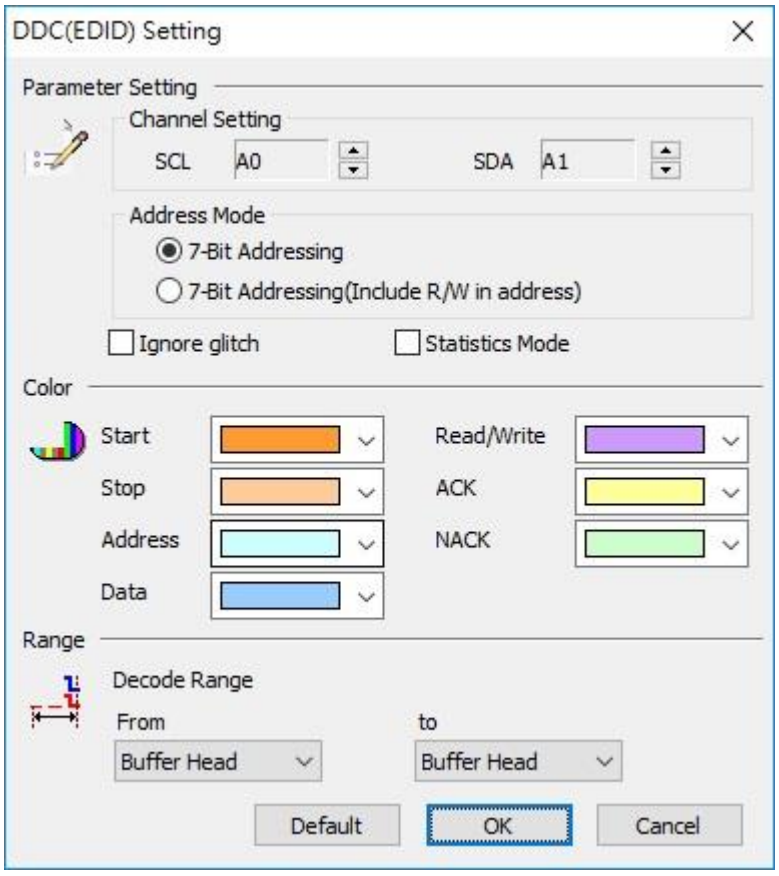
Click **OK** to run the HDMI-CEC decode and see the result on the Waveform Window below.



HDMI-DDC (EDID)

EDID (Extended Display Identification Data) is I2C protocol base on DDC wire and transmitted monitor information. Now, HDMI, DVI and VGA are support this protocol.

Settings



Channel: Display the channels (CH0 and CH1).

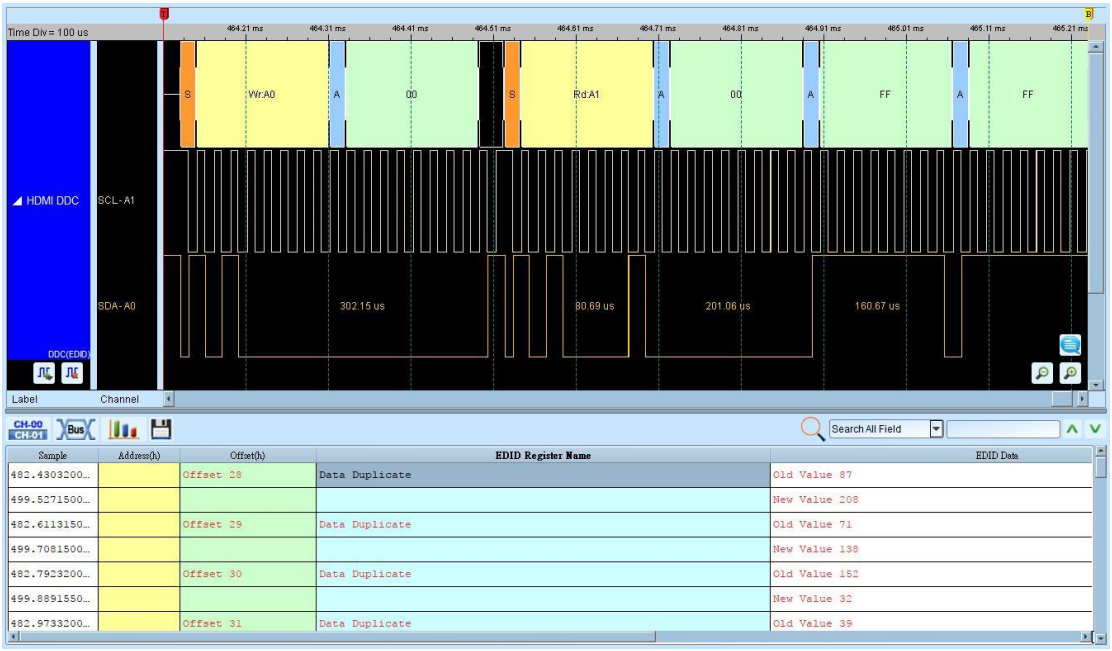
7-bit addressing: Show 7-bit addressing

7-bit addressing(Include R/W in Address): Show 8-bit addressing(include 7-bit addressing and 1-bit Rd/Wr).

Ignore glitch: Ignore the glitches occurred due to the slow transitions.

Statistic Mode: Collect all the data frames into one report by register address order.

Result

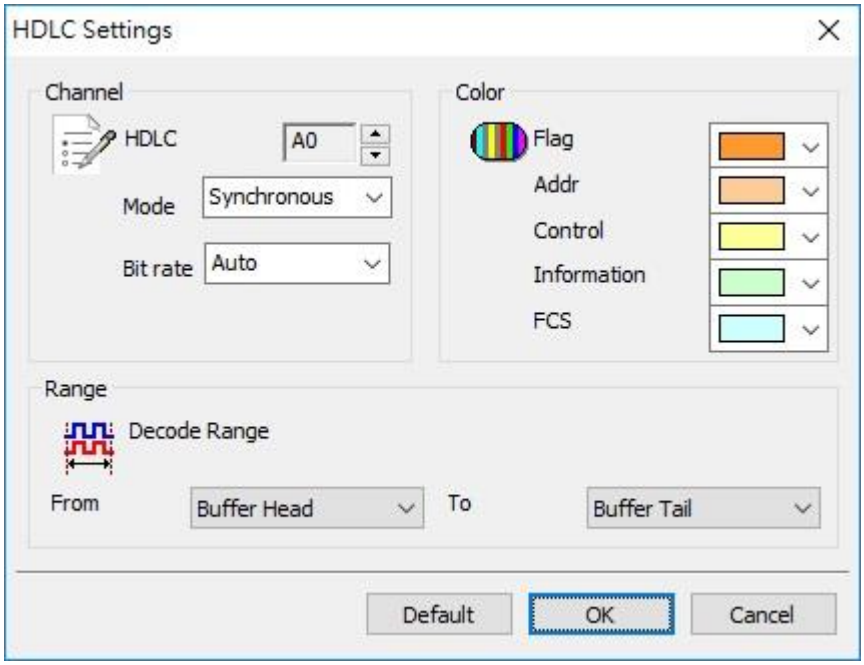


Sample	Address(h)	Offset(h)	EDID Register Name	EDID Data
482.4303200...		Offset 28	Data Duplicate	Old Value 87
499.5271500...				New Value 208
482.6113150...		Offset 29	Data Duplicate	Old Value 71
499.7081500...				New Value 138
482.7923200...		Offset 30	Data Duplicate	Old Value 152
499.8891550...				New Value 32
482.9733200...		Offset 31	Data Duplicate	Old Value 39

HDLC

HDLC (High-level Data Link Control) is the default synchronous data link layer protocol used in the equipment of Cisco.

Settings

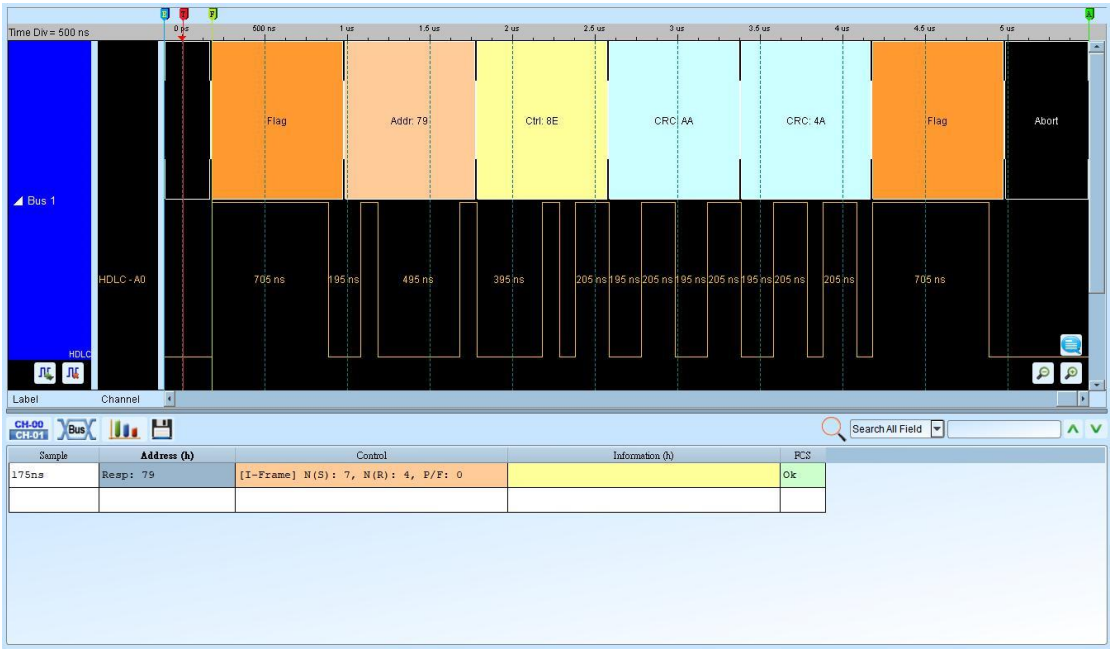


HDLC: Set the channel of the signal.

Mode: Synchronous or Asynchronous mode.

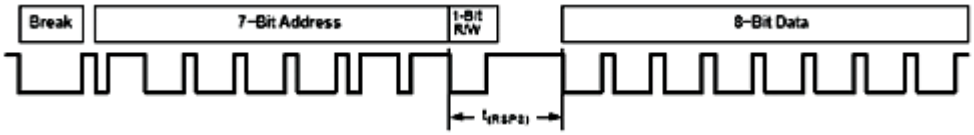
Bit rate: Set the specific data rate or auto detection.

Result



HDQ

The HDQ bus has two kinds of formats: 8 bits or 16 bits signals as the diagram below.



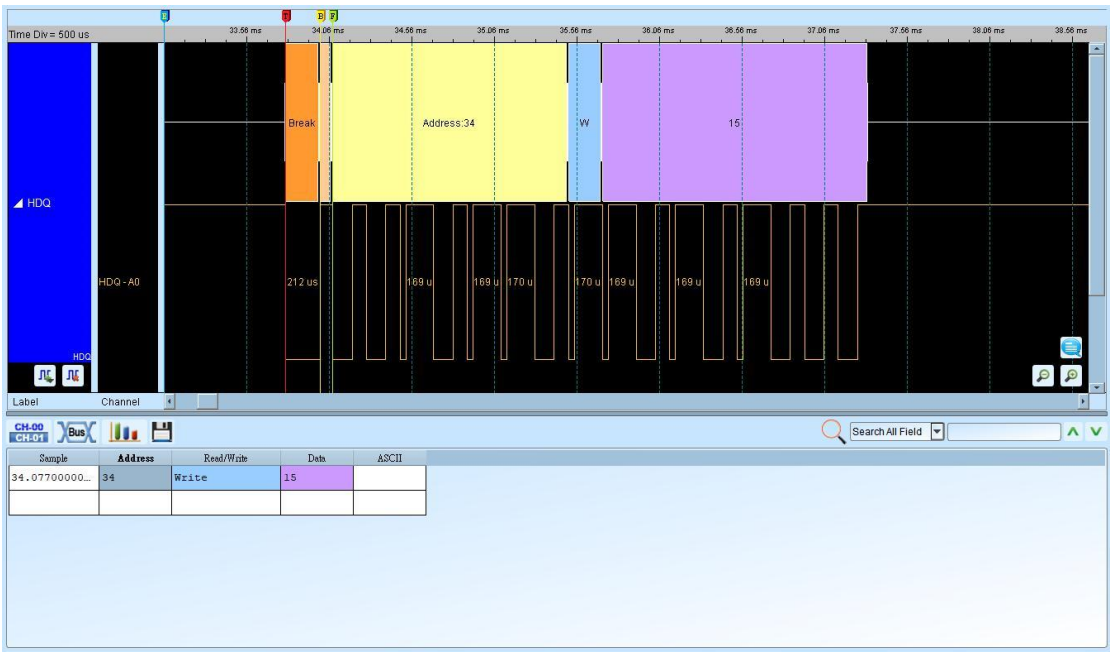
Settings

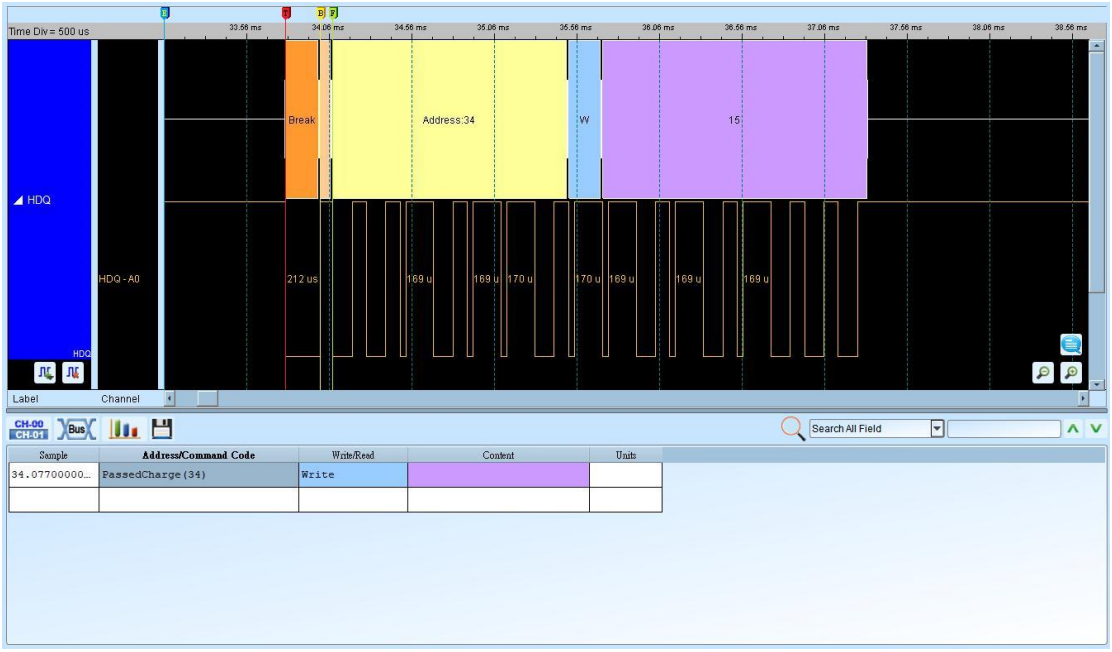
Channel: Set the HDQ channel: Show the selected channel (CH 0).

Show Battery Information: monitor the command between battery and IC.

Result

Click **OK** to run the HDQ decode and see the result on the Waveform Window below.

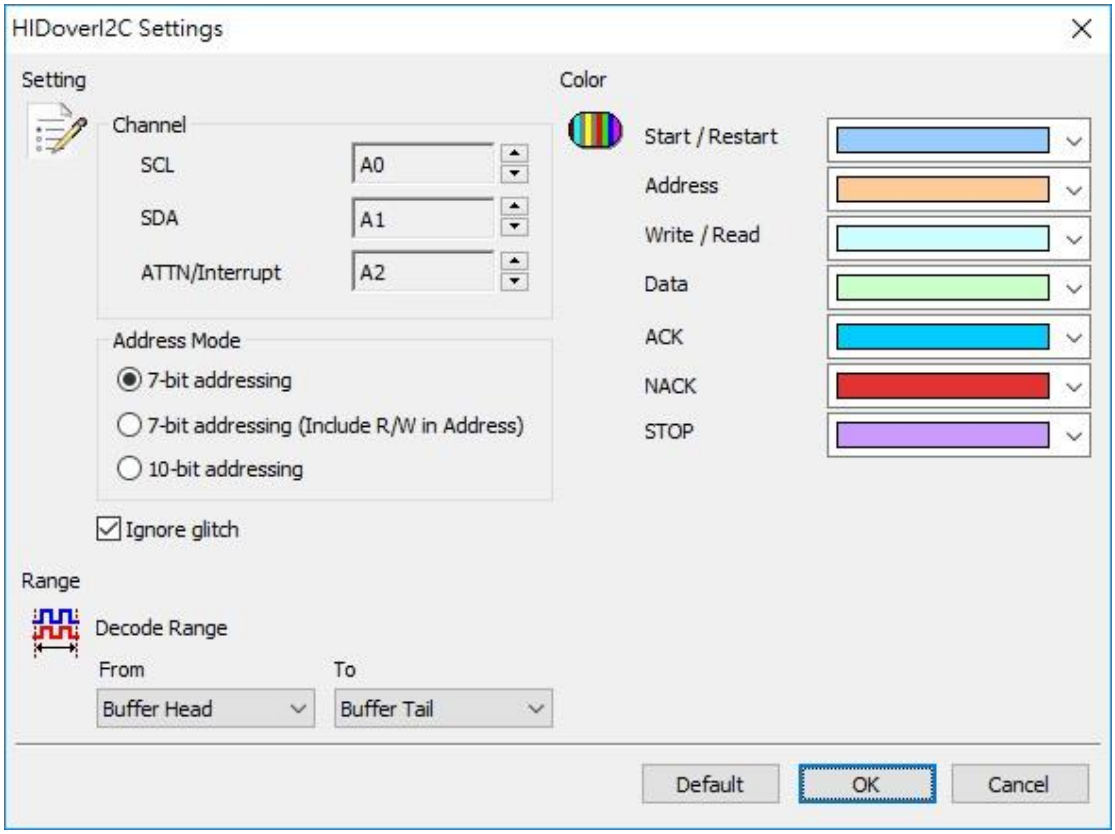




HID Over I^2C

HID Over I2C (Human Interface Device Over I2C) protocol is established by Microsoft. It's applied for Windows 8 ARM platform.

Settings



Channel: Show the selected channels (SCL:CH0, SDA:CH1, ATTN:CH2).

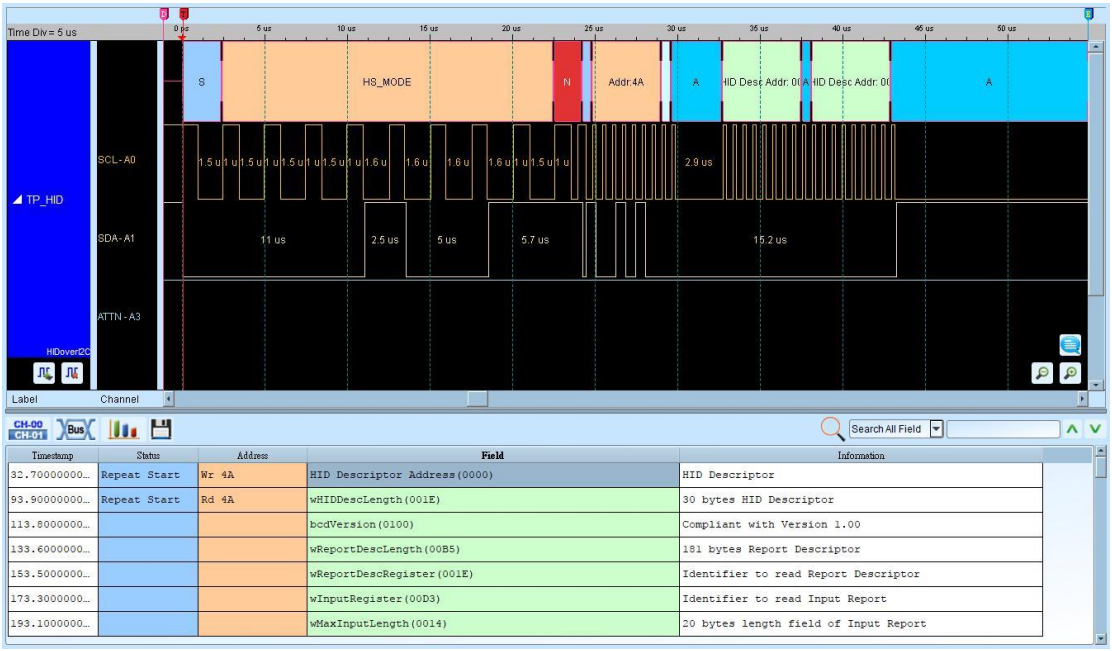
7-bit addressing: Show 7-bit addressing.

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit Rd/Wr).

10-bit addressing: show 10-bit addressing.

Ignore glitch: Ignore the glitches occurred due to the slow transitions.

Result

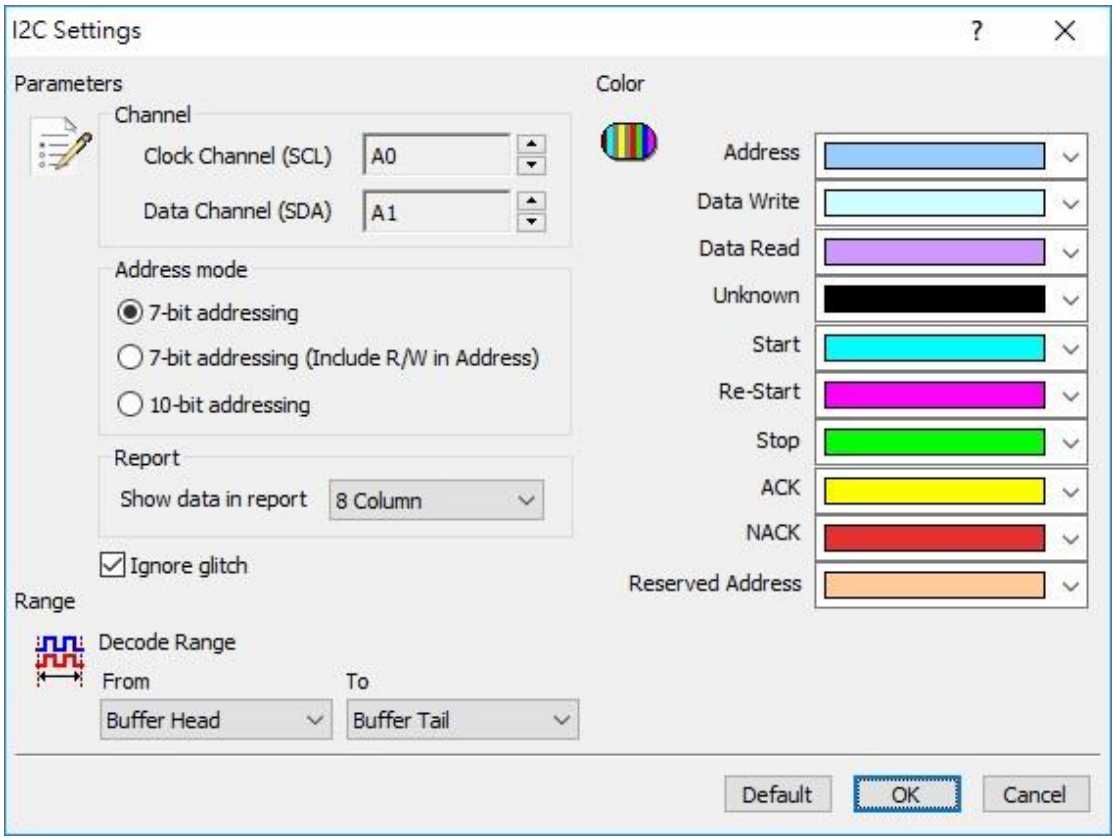


Timestamp	Status	Address	Field	Information
32.70000000...	Repeat Start	Wr 4A	HID Descriptor Address(0000)	HID Descriptor
93.90000000...	Repeat Start	Rd 4A	wHIDDescLength(001E)	30 bytes HID Descriptor
113.8000000...			bcdVersion(0100)	Compliant with Version 1.00
133.6000000...			wReportDescLength(00B5)	181 bytes Report Descriptor
153.5000000...			wReportDescRegister(001E)	Identifier to read Report Descriptor
173.3000000...			wInputRegister(00D3)	Identifier to read Input Report
193.1000000...			wMaxInputLength(0014)	20 bytes length field of Input Report

I²C

The Inter-Integrated Circuit (I²C) bus has two data bits: Serial Data (SDA) and Serial Clock (SCL).

Settings



Channel: Display the channels (CH0 and CH1).

Address Mode: Select the 7-bit or 10-bit address.

7-bit addressing: Show 7-bit addressing.

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit Rd/Wr).

10-bit addressing: show 10-bit addressing.

Report: Show either 8 or 16-columns data in the report window.

Ignore glitch: Ignore the glitches occurred due to the slow transitions.

Result

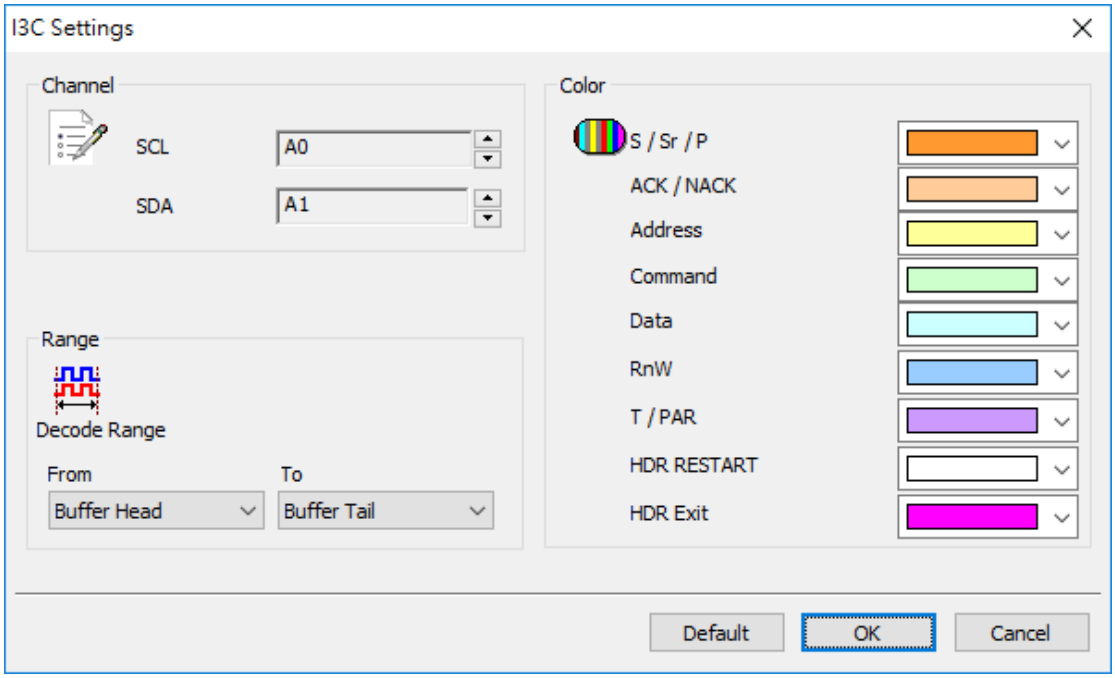
Click **OK** to run the I^2C decode and see the result on the Waveform Window below.

It shows frequency in the Information field.

I3C

I^{3}C is a bus interface for connecting sensors to an application processor. It is a core sensor integration technology that can combine multiple sensors from different vendors in a device to streamline integration and improve cost efficiencies. It gives developers unprecedented opportunity to craft innovative designs for any mobile product, from smartphones, to wearables, to safety systems in automobiles.

Settings

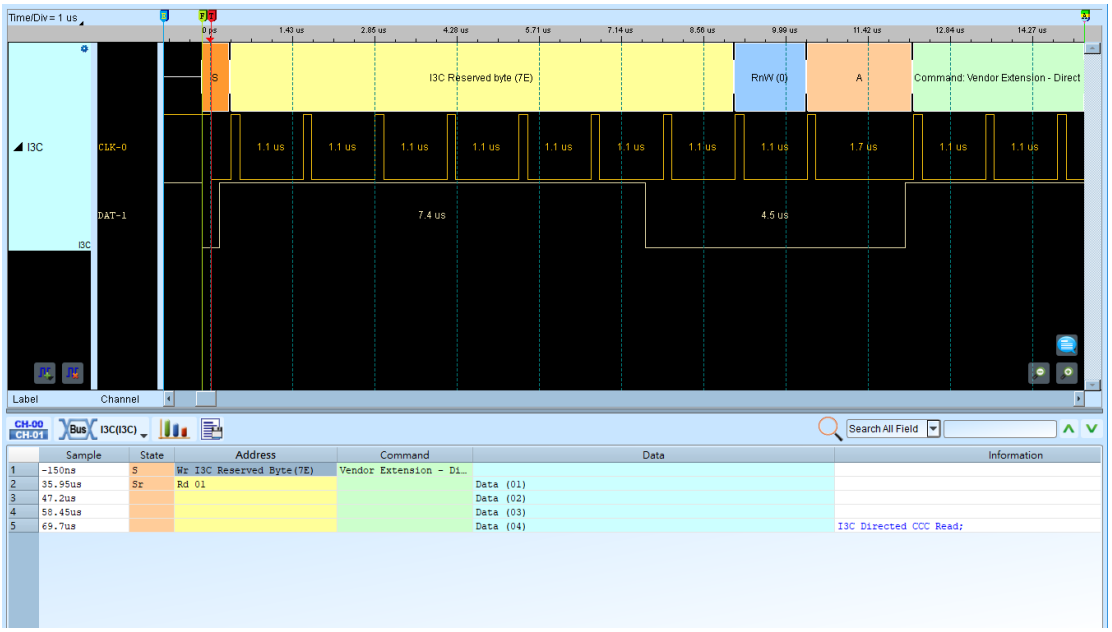


Channel: Display the channels (CH0 and CH1).

Result

Click **OK** to run the I^3C decode and see the result on the Waveform Window below.

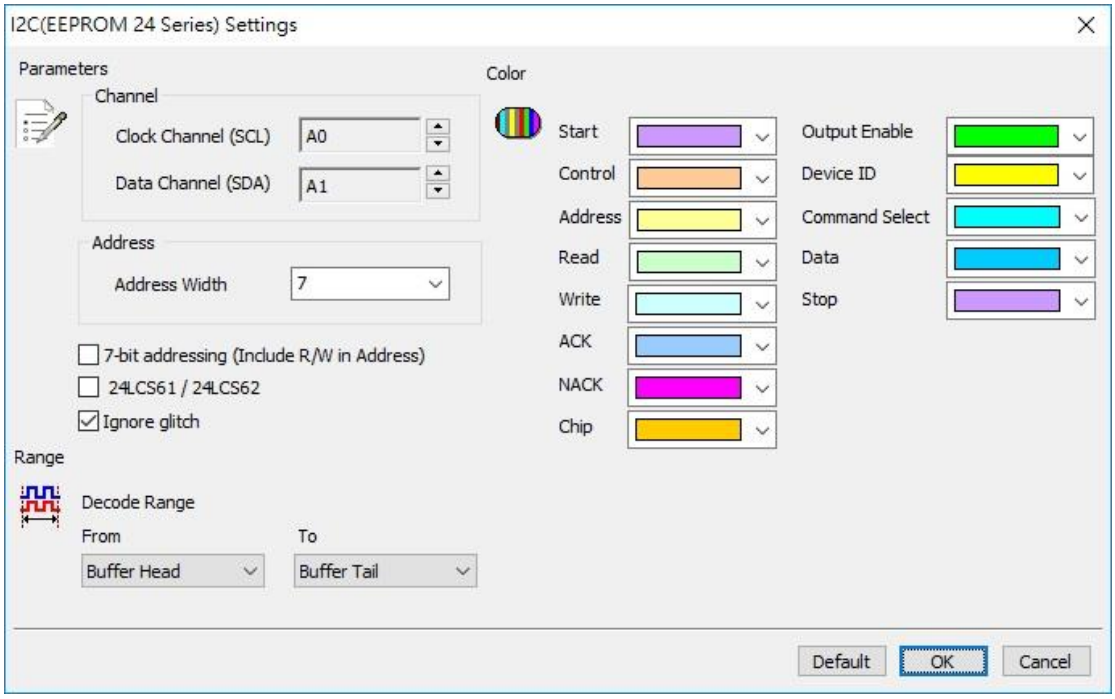
It shows frequency in the Information field.



I²C EEPROM

EEPROM can be erased and reprogrammed (written to) repeatedly through the application of higher than normal electrical voltage generated externally or internally in the case of modern EEPROMs.

Settings



Channel: Display the channels (CH0 and CH1)

Address: The default address width is 7.

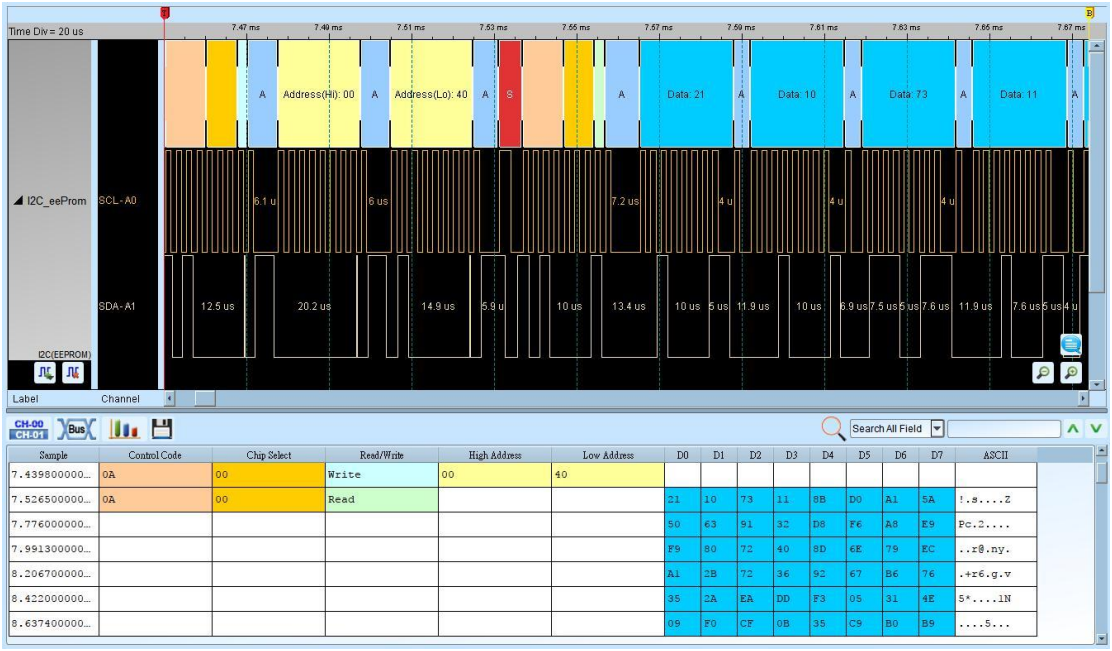
7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit Rd/Wr).

24LCS61/24LCS62: 24LCS61/24LCS62 EEPROM protocol.

Ignore glitch: Ignore the glitch when the slow transitions.

Result

Click OK to run the I²C EEPROM decode and see the result on the Waveform Window below.

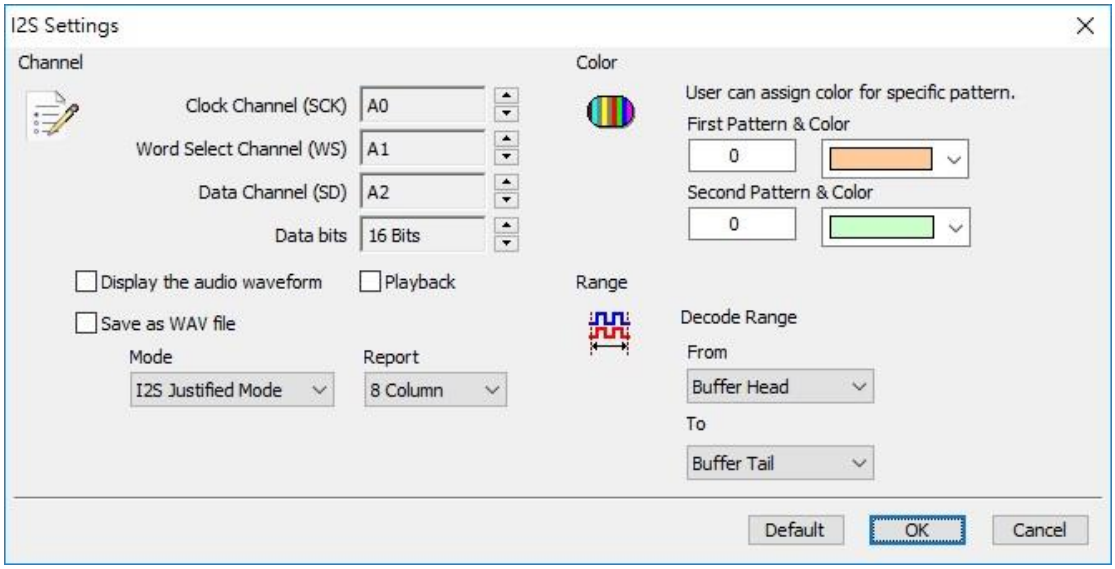


Sample	Control Code	Chip Select	Read/Write	High Address	Low Address	D0	D1	D2	D3	D4	D5	D6	D7	ASCII
7.439800000...	0A	00	Write	00	40									
7.526500000...	0A	00	Read			21	10	73	11	8B	D0	A1	5A	!.s....Z
7.776000000...						50	63	91	32	D8	F6	A8	E9	Pc.2....
7.991300000...						F9	80	72	40	8D	6E	79	EC	..r@.ny.
8.206700000...						A1	2B	72	36	92	67	B6	76	.+r6.g.v
8.422000000...						35	2A	EA	DD	F3	05	31	4E	5*....1N
8.637400000...						09	F0	CF	0B	35	C9	B0	B9	....5...

I²S

The Inter-Integrated Circuit Sound (I2S) bus has three data bits: Serial Clock (SCK), Word Select Line (WS) and Multiplex Data Line (SD).

Settings



Channel: Show the selected channels (CH0, CH1 and CH2) and set Data bits (16 bits).

Display the audio waveform: Click to display the audio waveform in the Waveform Window.

Playback: Click to display the audio from the speaker..

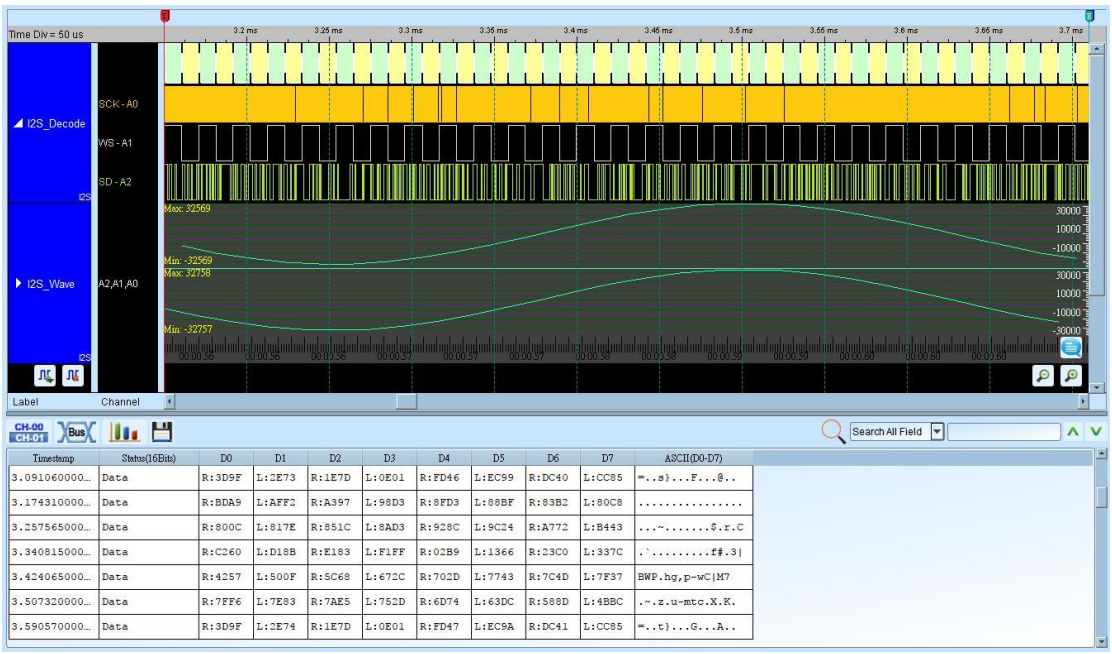
Save as WAV file: Click to save the data to a audio file(.wav) in the work directory.

Mode: I²S Justified/MSB Justified/LSB Justified/PCM/TDM.

Report: Select the column number.

Result

Click **OK** to run I²S decode and see the result on the Waveform Window below.

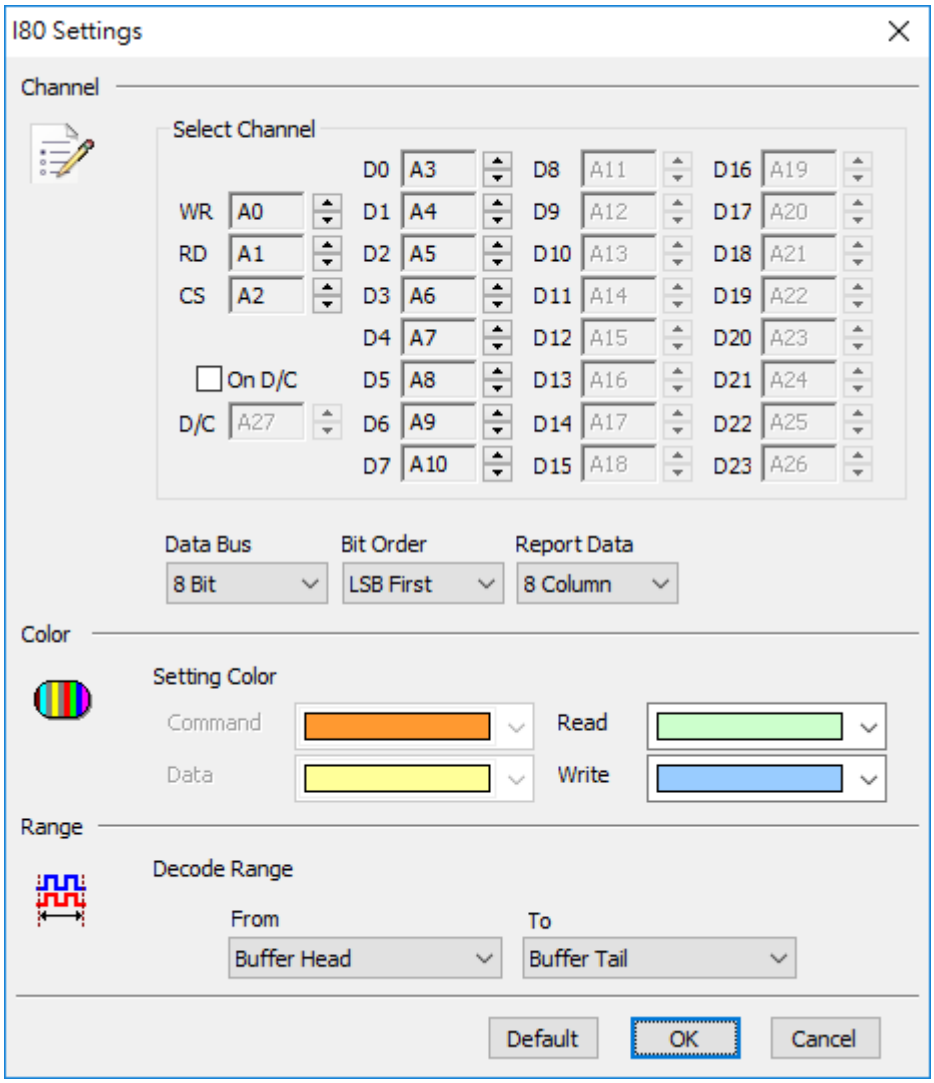


Timestamp	Status(16Bits)	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)
3.091060000...	Data	R:3D9F	L:2E73	R:1E7D	L:0E01	R:FD46	L:EC99	R:DC40	L:CC85	=..s}...F...@..
3.174310000...	Data	R:BDA9	L:AFF2	R:A397	L:98D3	R:8FD3	L:88BF	R:83B2	L:80C8	.....
3.257565000...	Data	R:800C	L:817E	R:851C	L:8AD3	R:928C	L:9C24	R:A772	L:B443	...~.....$.r.C
3.340815000...	Data	R:C260	L:D18B	R:E183	L:F1FF	R:02B9	L:1366	R:23C0	L:337C	.`.....f#.3|
3.424065000...	Data	R:4257	L:500F	R:5C68	L:672C	R:702D	L:7743	R:7C4D	L:7F37	BWP.hg,p-wC|M7
3.507320000...	Data	R:7FF6	L:7E83	R:7AE5	L:752D	R:6D74	L:63DC	R:588D	L:4BBC	.~.z.u-mtc.X.K.
3.590570000...	Data	R:3D9F	L:2E74	R:1E7D	L:0E01	R:FD47	L:EC9A	R:DC41	L:CC85	=..t}...G...A..

I80

The I80 controls 3 or 4-pins (WR, RD, CS, D/C) data.

Settings



Select Channel: Show the selected channels (WR, RD, CS, D0, D1, D2, D3, D4, D5, D6,…).

On D/C: Use the D/C pin as Command (Low) or Data (High).

Data Bus: Select 4 Bit, 8 Bit, 12 Bit, 16 Bit, 20 Bit, or 24 Bit.

Bit Order: Select LSB First or MSB First.

Report Data: Select 8 columns or 16 columns.

Result

Click **OK** to run the I80 decode and see the result on the Waveform Window below.

IDE

IDE (Integrated Device Electronics) is a computer hardware bus and has the following data bits:

General Channel (11 pins): DASP-, DIOR-:HDMARDY-:HSTROBE, DIOW-:STOP, DMACK-, DMARQ, INTRQ, IORDY:DDMARDY-:DSTROBE, PDIAG-:CBLID-, RESET-, CSEL, IOCS16-.

Register Channel (5 pins): CS(0:1)-, DA(2:0).

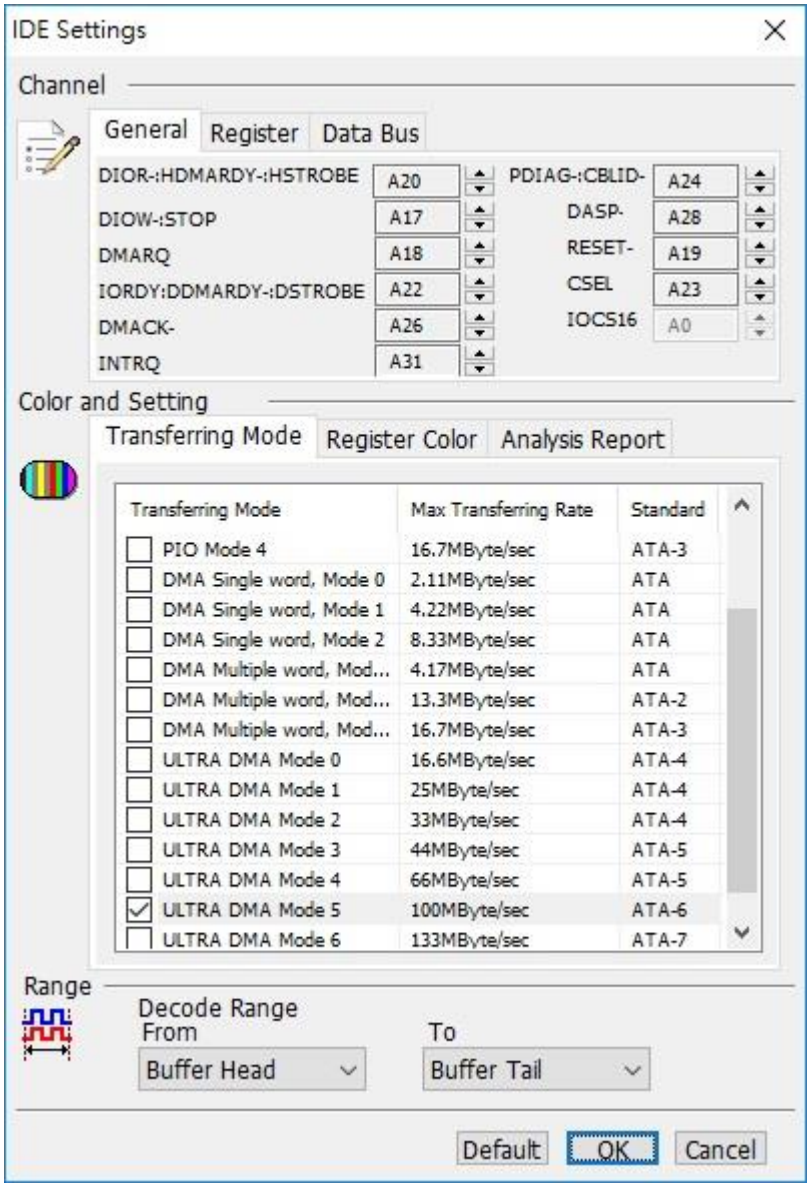
Data Bus (16 pins): DD(15:0)

We recommend that IDE bus of the target system to be connected to the instrument as the following table:

IDE Pin No.	IDE Pin name	IDE Pin Description	LA default Channel No.
Pin1	Reset-	Hardware reset	Channel 0
Pin2	Ground		
Pin3	DD7	Device data	Channel 1
Pin4	DD8	Device data	Channel 2
Pin5	DD6	Device data	Channel 3
Pin6	DD9	Device data	Channel 4
Pin7	DD5	Device data	Channel 5
Pin8	DD10	Device data	Channel 6
Pin9	DD4	Device data	Channel 7
Pin10	DD11	Device data	Channel 8
Pin11	DD3	Device data	Channel 9
Pin12	DD12	Device data	Channel 10
Pin13	DD2	Device data	Channel 11
Pin14	DD13	Device data	Channel 12
Pin15	DD1	Device data	Channel 13
Pin16	DD14	Device data	Channel 14

Pin17	DD0	Device data	Channel 15
Pin18	DD15	Device data	Channel 16
Pin19	Ground		
Pin20	Key pin		
Pin21	DMARQ	DMA request	Channel 17
Pin22	Ground		
Pin23	DIOW-:STOP	Device I/O write: Stop Ultra DMA burst	Channel 18
Pin24	Ground		
Pin25	DIOR-:HDMARDY-:HSTROBE	Device I/O read: Ultra DMA ready: Ultra DMA data strobe	Channel 19
Pin26	Ground		
Pin27	IORDY:DDMARDY-:DSTROBE	I/O channel ready: Ultra DMA ready: Ultra DMA data strobe	Channel 20
Pin28	CSEL	Cable select	Channel 21
Pin29	DMACK-	DMA acknowledge	Channel 22
Pin30	Ground		
Pin31	INTRQ	Device interrupt	Channel 23
Pin32	Obsolete (see note)	Device 16-bit I/O in ATA-2	Channel 24
Pin33	DA1	Device address	Channel 25
Pin34	PDIAG-:CBLID-	Passed diagnostics: Cable assembly type identifier	Channel 26
Pin35	DA0	Device address	Channel 27
Pin36	DA2	Device address	Channel 28
Pin37	CS0-	Chip select	Channel 29
Pin38	CS1-	Chip select	Channel 30
Pin39	DASP-	Device active, device 1 present	Channel 31
Pin40	Ground		

Settings



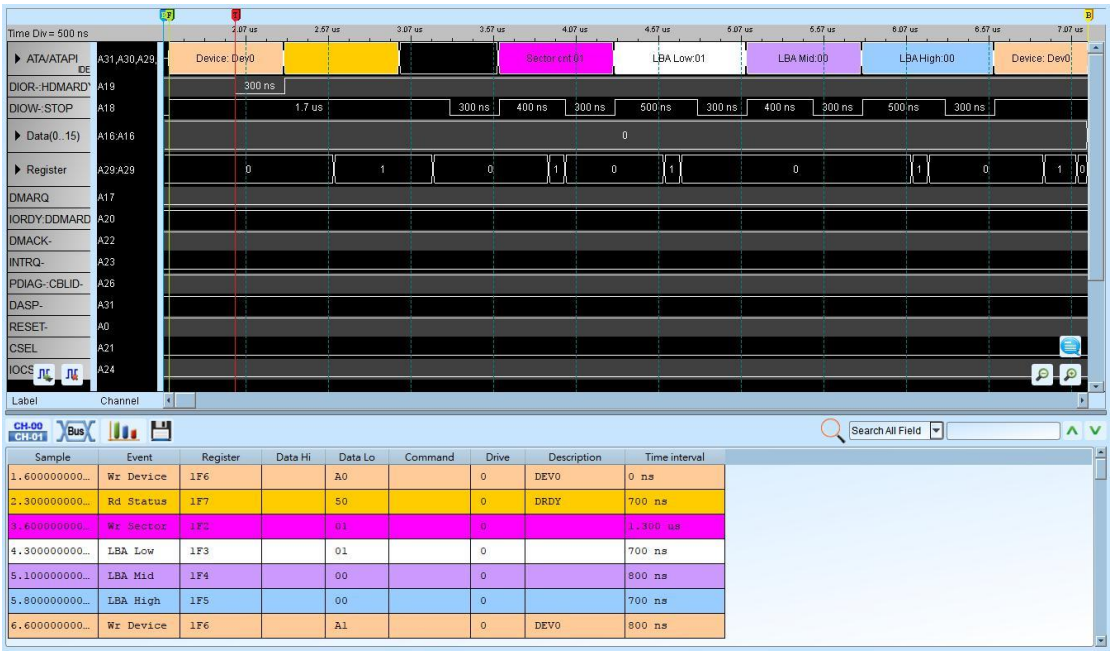
Channel: Set channel number for General, Register, and Data Bus.

Transferring Mode: Select the target system.

Analysis Report: Filter the data in the Report Window.

Result

Click **OK** to run the IDE decode and see the result on the Waveform Window below.

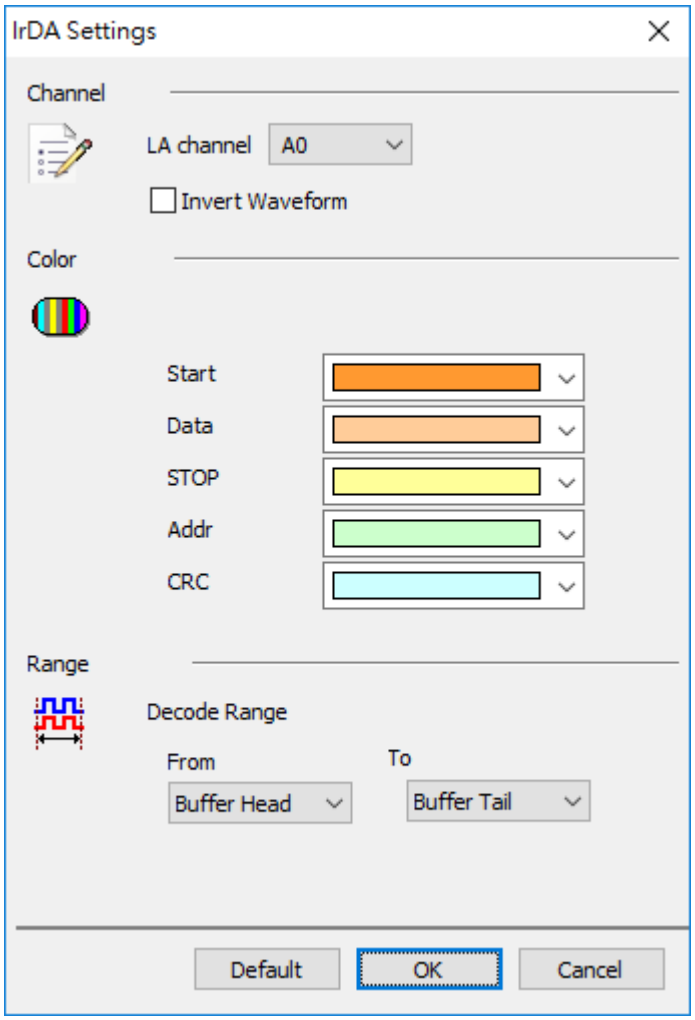


Sample	Event	Register	Data Hi	Data Lo	Command	Drive	Description	Time interval
1.600000000...	Wr Device	1F6		A0		0	DEV0	0 ns
2.300000000...	Rd Status	1F7		50		0	DRDY	700 ns
3.600000000...	Wr Sector	1F2		01		0		1.300 us
4.300000000...	LBA Low	1F3		01		0		700 ns
5.100000000...	LBA Mid	1F4		00		0		800 ns
5.800000000...	LBA High	1F5		00		0		700 ns
6.600000000...	Wr Device	1F6		A1		0	DEV0	800 ns

IrDA

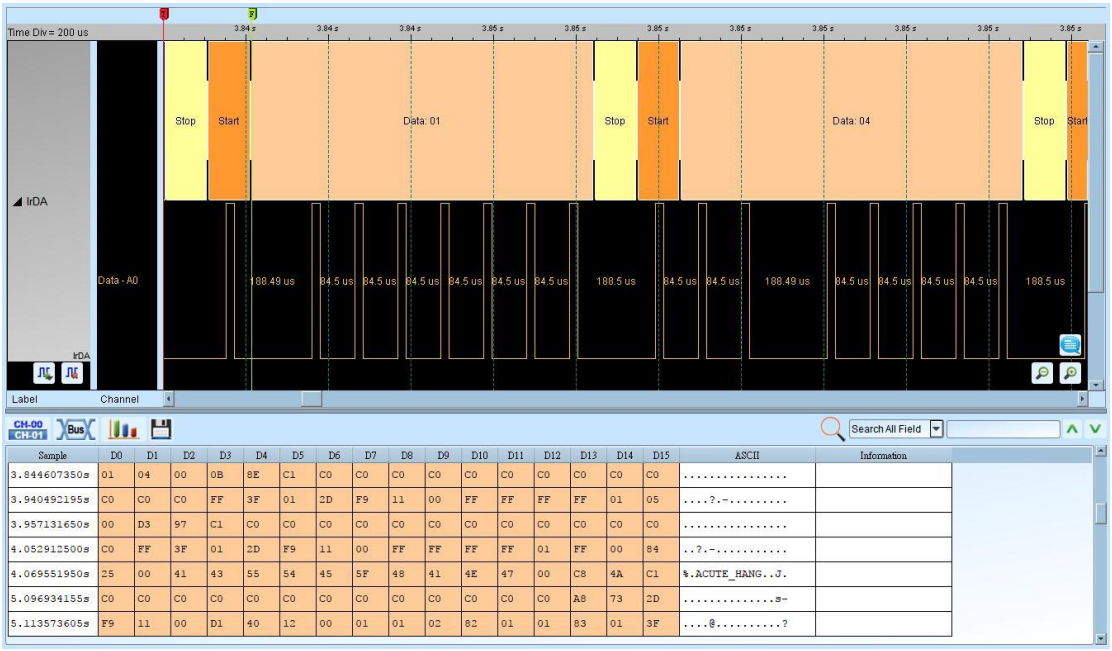
The Infrared Data Association (IrDA) was formed in 1993. The IrDA is point to point user model for a wide range of appliances and devices.

Settings



Channel: Show the selected channel.

Result

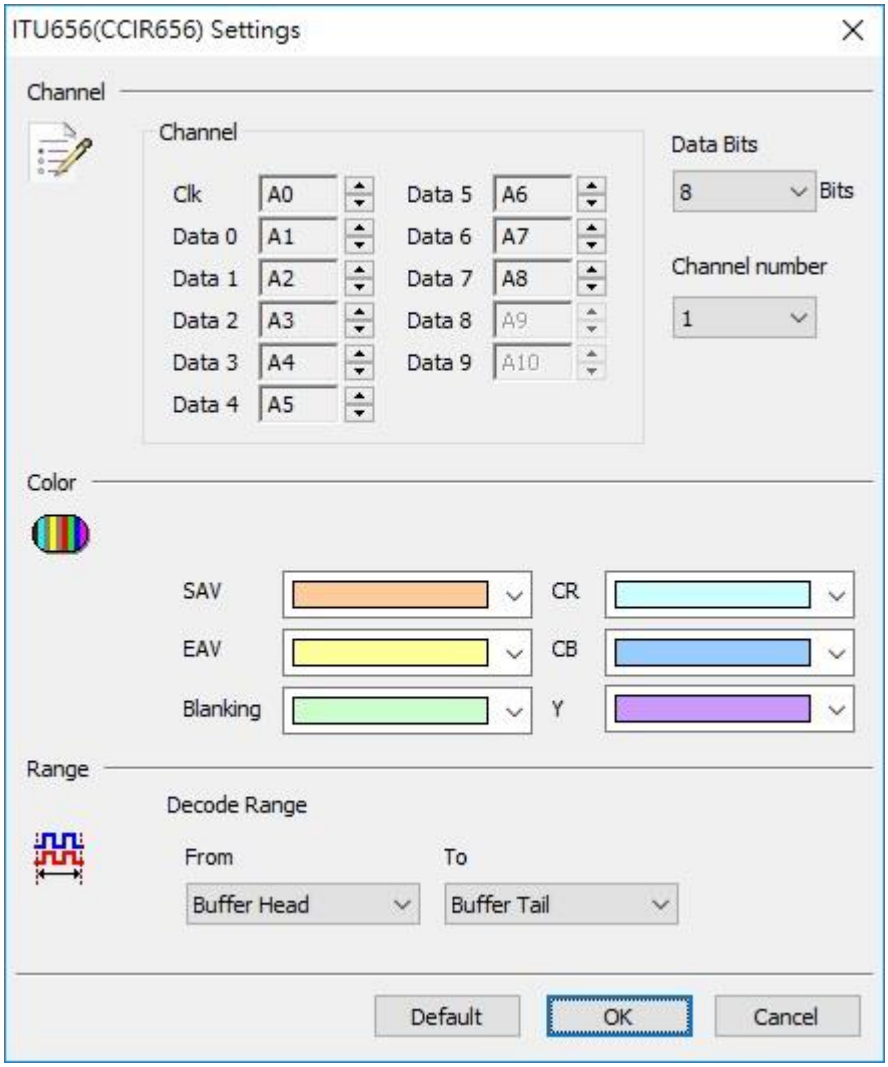


Sample	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	ASCII	Information
3.844607350s	01	04	00	0B	8E	C1	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	.....	
3.940492195s	C0	C0	C0	FF	3F	01	2D	F9	11	00	FF	FF	FF	FF	01	05	....?.-.....	
3.957131650s	00	D3	97	C1	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	.....	
4.052912500s	C0	FF	3F	01	2D	F9	11	00	FF	FF	FF	FF	01	FF	00	84	..?.-.....	
4.069551950s	25	00	41	43	55	54	45	5F	48	41	4E	47	00	C8	4A	C1	%.ACUTE_HANG..J.	
5.096934155s	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	C0	A8	73	2D	.....s-	
5.113573605s	F9	11	00	D1	40	12	00	01	01	02	82	01	01	83	01	3F	....@.....?	

ITU656 (CCIR656)

ITU656 describes a simple digital video protocol for streaming uncompressed PAL or NTSC Standard Definition TV (525 or 625 lines) signals. The protocol builds upon the 4:2:2 digital video encoding parameters defined in ITU-R Recommendation BT.601, which provides interlaced video data, streaming each field separately, and uses the YCbCr color space and a 13.5 MHz sampling frequency for pixels.

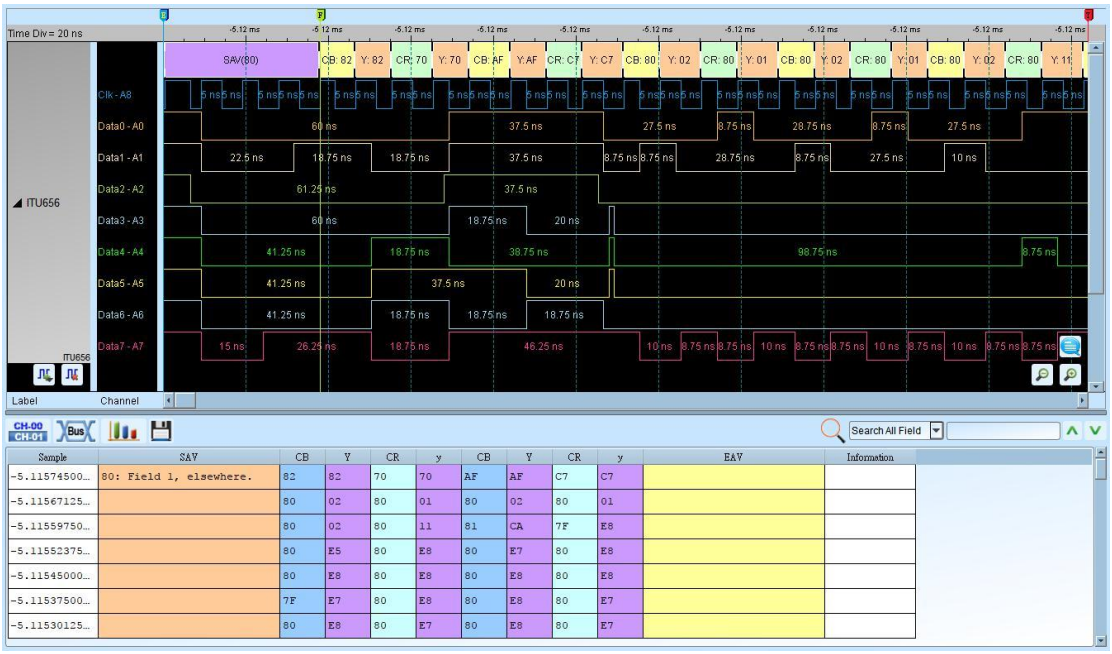
Settings



Channel: Show the selected channel (Clk, Data 0 – Data 9).

Data Bits: Show the number of data bits.

Result



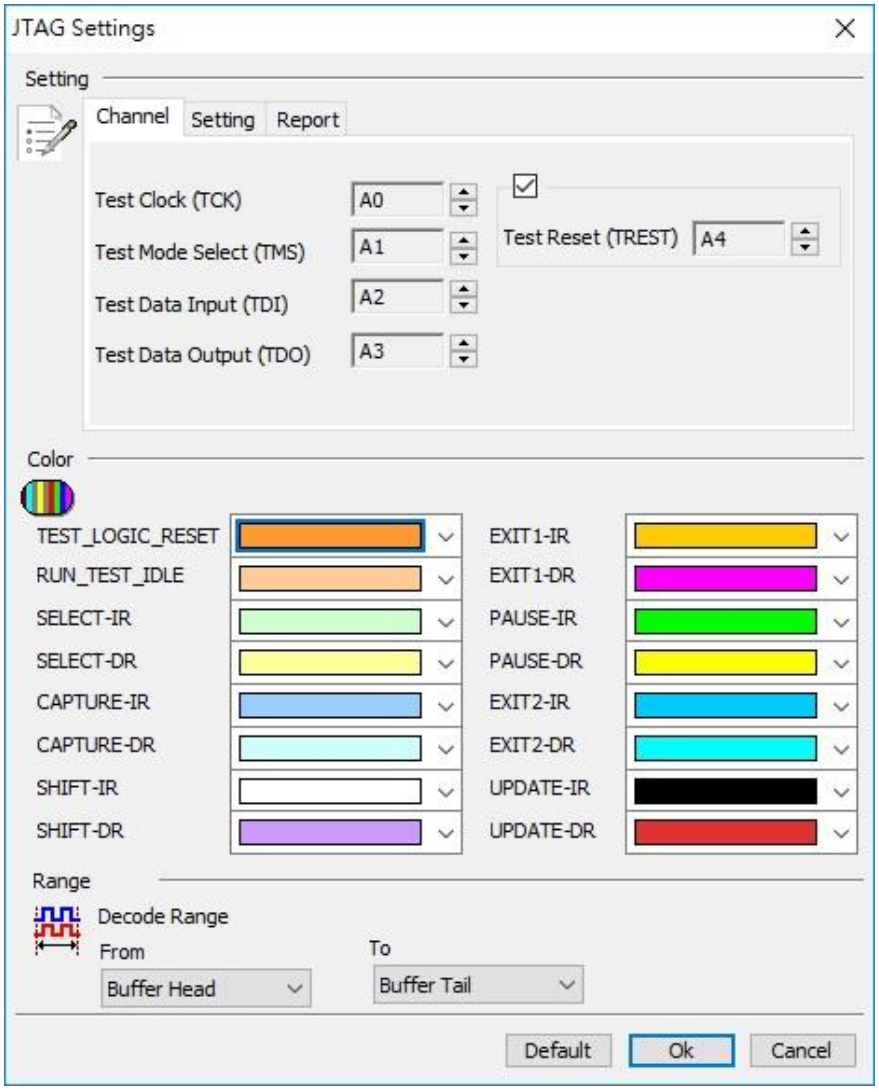
Sample	SAV	CB	Y	CR	y	CB	Y	CR	y	EAV	Information
-5.11574500...	80: Field 1, elsewhere.	82	82	70	70	AF	AF	C7	C7		
-5.11567125...		80	02	80	01	80	02	80	01		
-5.11559750...		80	02	80	11	81	CA	7F	E8		
-5.11552375...		80	E5	80	E8	80	E7	80	E8		
-5.11545000...		80	E8	80	E8	80	E8	80	E8		
-5.11537500...		7F	E7	80	E8	80	E8	80	E7		
-5.11530125...		80	E8	80	E7	80	E8	80	E7		

JTAG

Joint Test Action Group (JTAG) is the common name used for the IEEE 1149.1 standard entitled Standard Test Access Port and Boundary-Scan Architecture for test access ports used for testing printed circuit boards using boundary scan.

A JTAG interface is a special four/five-pins interface added to a chip, designed so that multiple chips on a board can have their JTAG lines daisy-chained together if specific conditions are met, and a test probe need only connect to a single "JTAG port" to have access to all chips on a circuit board.

Settings

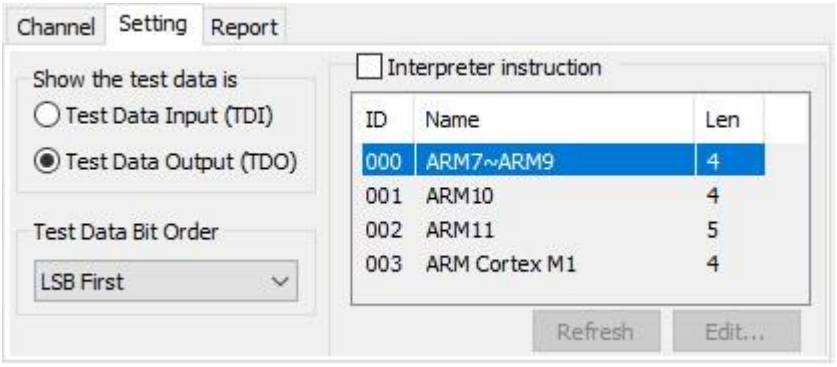


Settings: Includes Channel, Setting, and Report.

Channel: Set the channel number.

Show the test data is: The data is TDI or TDO.

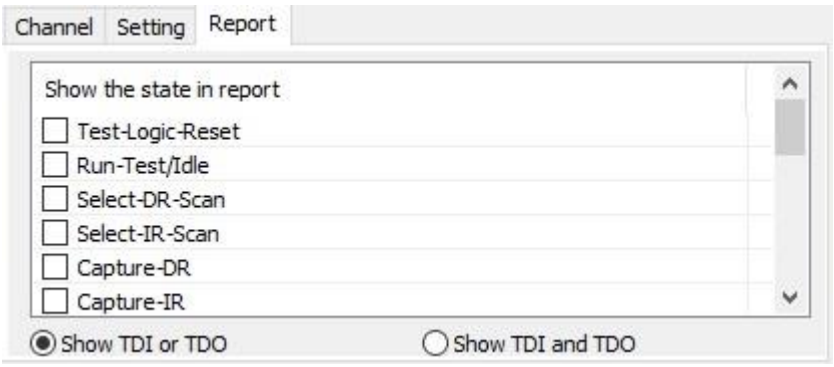
Test Data Bit Order: LSB First or MSB First.



Interpreter instruction: Check the Interpreter Instruction and you will see a list of commands. The JTAG decode will display its updated commands in the Instruction Register, which is the temporary memory buffer for the commands. Click Edit to edit the commands in the Interpreter Instructions; then click Refresh to update the commands in the Interpreter Instructions.

Acute JTAG Instruction table (JtagInst.txt): This file is supported by the JTAG DLL and can be modified if needed. The JTAG Decode also supports the BSDL format. You can load the BSDL file in order to save time on editing commands. If you are interested in more details, please refer to the Acute JTAG Instruction table Syntax Description in the end of the JTAG Decode chapter.

Report: You can filter the data you want to see on the Report Window.



Show TDI or/and TDO

Result

Sample	TAP state	Instruction reg	TDI/TDO Data
660.2400000...	Run-Test/Idle		
668.5800000...	Select-DR-Scan		
676.9400000...	Select-IR-Scan		
685.2800000...	Capture-IR		
693.6400000...	Shift-IR		TDI:FFFFFFFF 05253000
1.249340000...	Shift-IR		TDI:FFFFFFFF FFFFFFFF
1.783660000...	Shift-IR		TDI:FFFFFFFF FFFFFFFF

Acute JTAG Instruction table Syntax Description (JtagInst.txt):

The numbers used in this file are hexadecimal.

##: is comment.

#ID: Command list number; the range is 00 - FF and , MUST be entered in order or will be seen as the end of commands.

#NAME: Command Name, 32 bytes most will be shown in the command list.

#LENGTH: Command length, unit in bits.

#CAPTURE: Command Capture Code, is stored in Instruction Register..

#INST: Command List, listed by Command Code and Command Name or will be seen as the end of commands..

#TRST: Enter 1 if TREST is needed or enter 0 or nothing if TREST is not needed.

#BSDL: Load the BSDL file. Use the BSDL file as step 1-6.

Example:#ID:00

#NAME:ARM7-ARM9

#LENGTH:4

#CAPTURE:1

#INST:0, EXTEST

#INST:2, SCAN_N

#INST:3, SAMPLE/PRELOAD

#INST:4, RESTART

#INST:5, CLAMP

#INST:7, HIGHZ

#INST:9, CLAMPZ

#INST:C, INTEST

#INST:E, IDCODE

#INST:F, BYPASS

#INST:

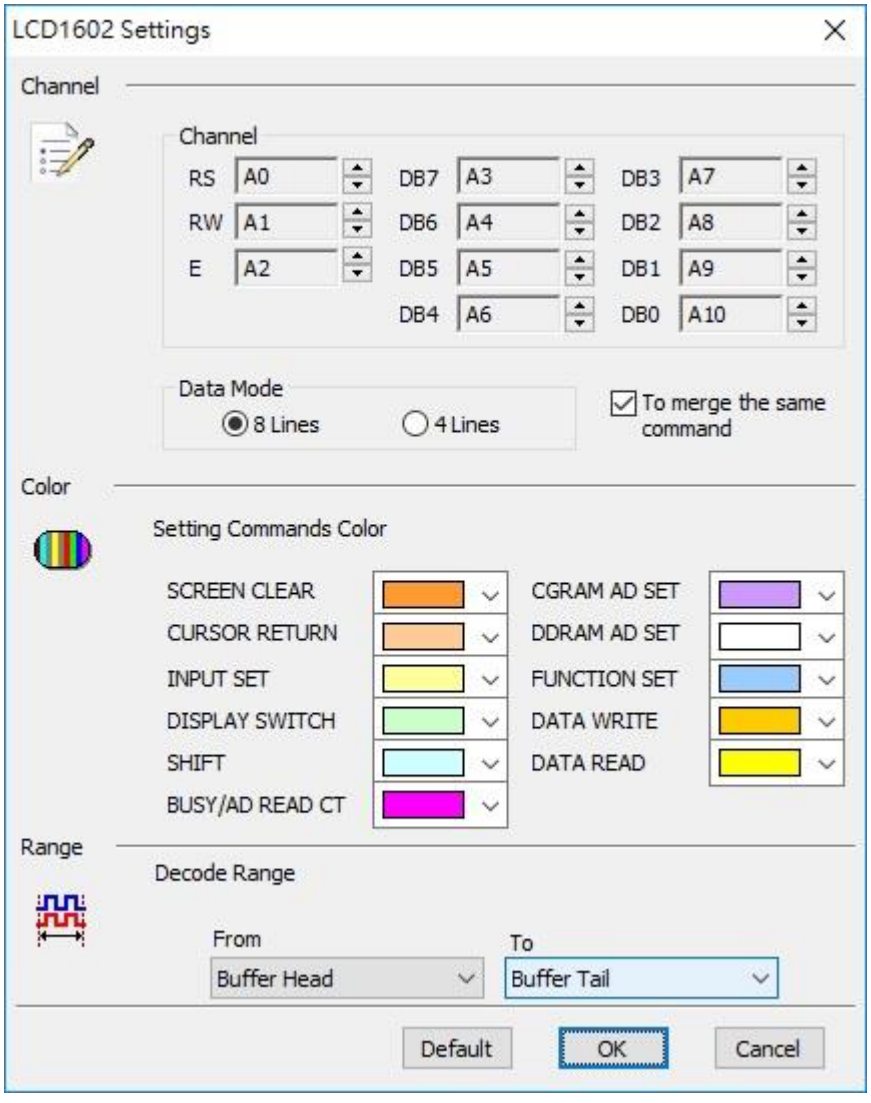
#ID:01

#BSDL:C:\3256at144_1532.bsd

LCD1602

The Liquid Crystal Display 1602 (LCD1602) bus has 11 data bits: Instruction/Data Register Select (RS), Read/Write Select (RW), Enable Select (E) and 8 bits or 4 bits Data Input/Output lines (DB0~DB7/DB0~DB3).

Settings



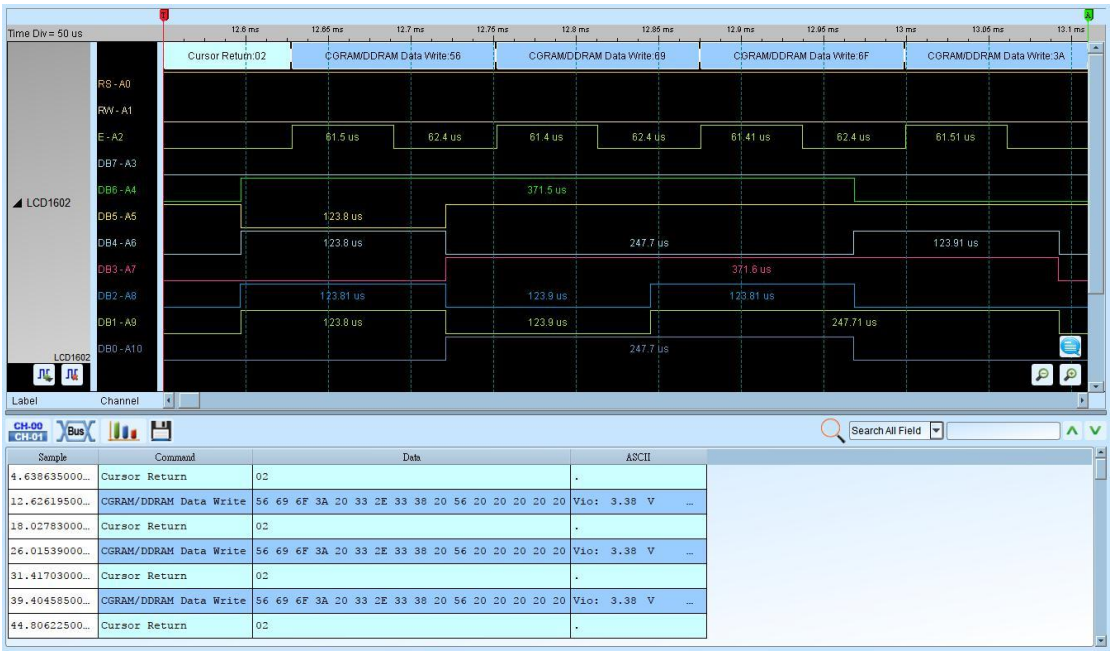
Channel: Show the selected channels (RS: CH0, RW: CH1,..., DB0: CH10).

Data Mode: 8 lines or 4 lines.

To merge the same command: Merge data with its command.

Result

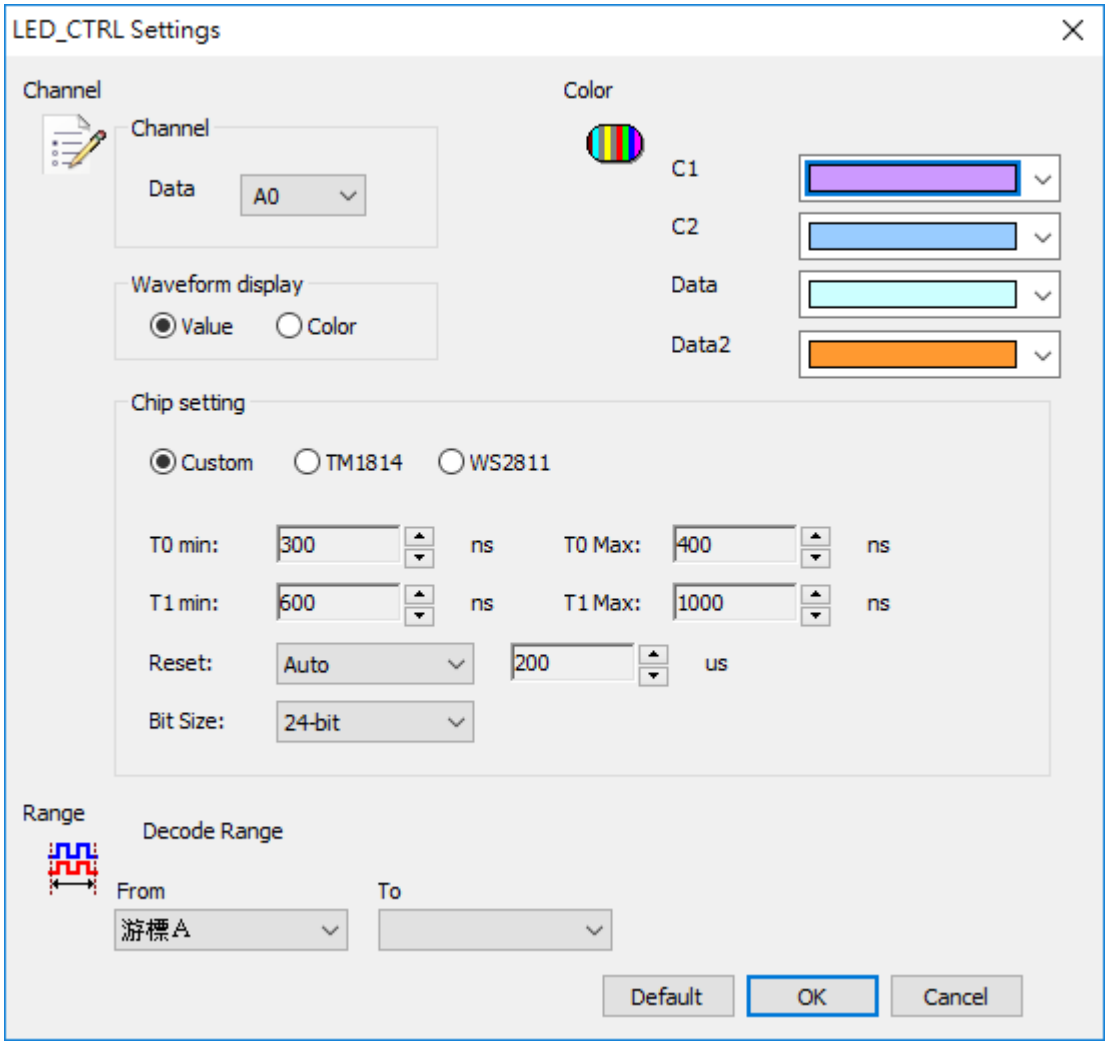
Click **OK** to run the LCD1602 decode and see the result on the Waveform Window below.



LED_Ctrl

LED Controls are made specifically for digital type LEDs. These LEDs contain a special IC chips that allow the user to control each LED or section of LEDs.

Settings



Channel: Show the selected channels.

Waveform display: show value or RGB color in waveform area.

Chip setting: Custom, TM1814, WS2811

Condition: Idle high

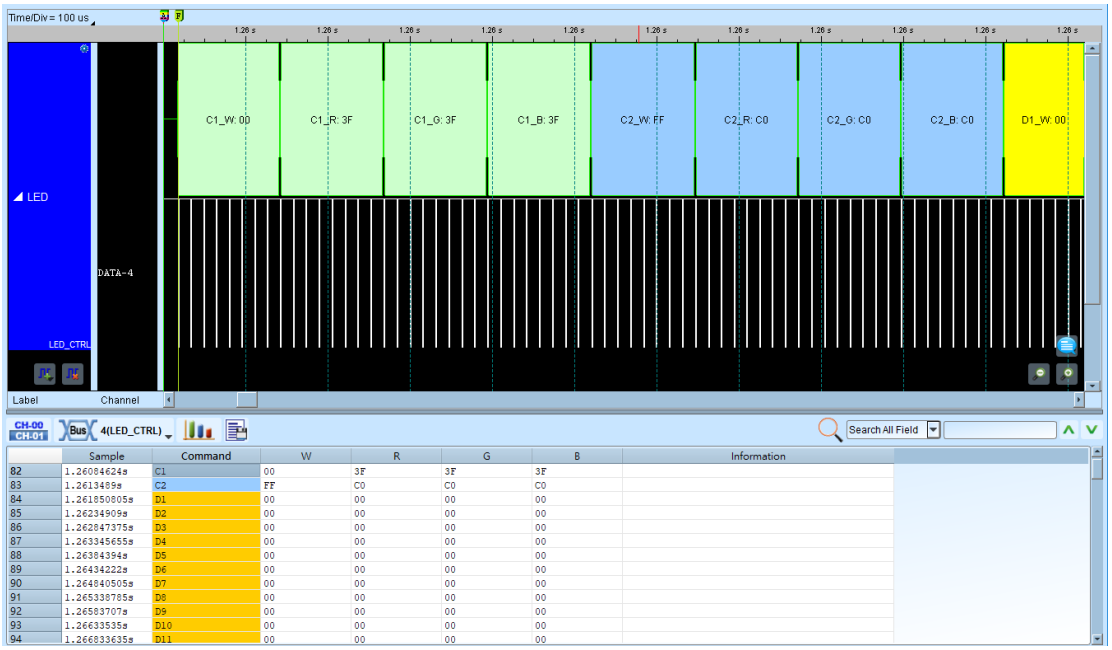
If the time that waveform goes to low between T0 min and T0 max, the bit will decode as zero. If it's between T1 min and T1 max, the bit will decode as one.

Reset: if the waveform keeps at high potential over the time, the decoder will reset the start bit.

Bit size: choose 32-bit (WRGB) or 24-bit (RGB).

Result

Click **OK** to run the LED_Ctrl decode and see the result on the Waveform Window below.



LIN

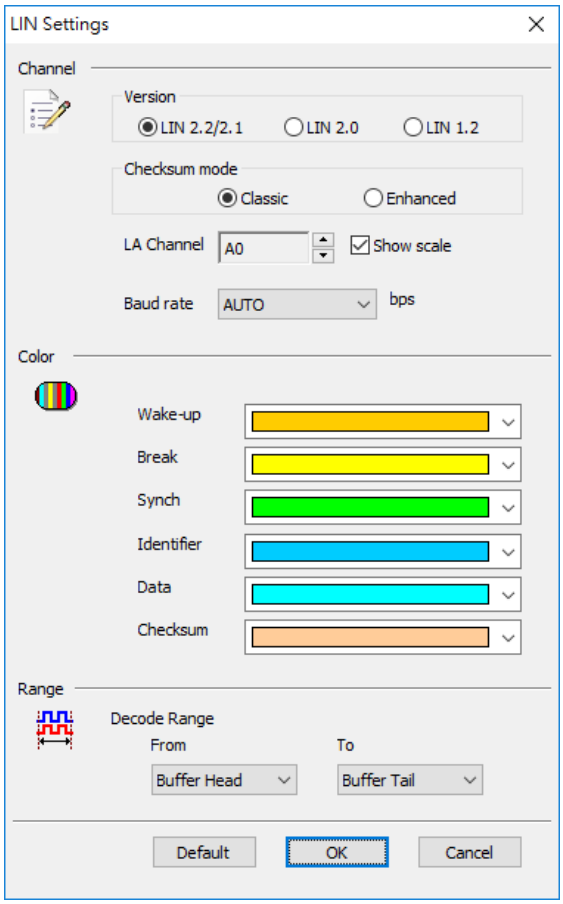
The Local Interconnect Network (LIN) bus (version 2.1) has two message types: Header and Response.

(1) Header contains three data frames: Synchronization Break (Break), Synchronization Field (Sync) and Identifier Field (Identifier).

(2) Response contains two data frames: Data Field (Data) and Checksum Field (Checksum). Checksum contains data and identifier (Enhanced mode), but version 1.3 or below (Classic mode) contains data only.

LIN bus has two states - Sleep mode and Active mode. While data is on the bus, all LIN nodes are in active state; but after a specified timeout, the nodes enter Sleep mode and will be released back to active state by a WAKEUP frame.

Settings



Version: Select LIN version.

Checksum Mode: Select Classic: data only or Enhanced: data and identifier.

LA Channel: Show the selected channel (CH0 for LIN).

Show Scale: Show scale on the waveform.

Baud rate: Show the selected baud rate.

Result

Click **OK** to run the Lin decode and see the result on the Waveform Window below.

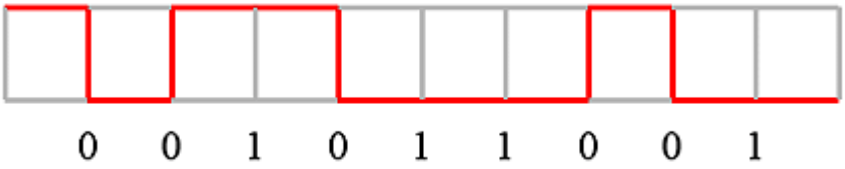
Timestamp	Event Type	PID(ID+P)	ID	Parity	Data	Checksum(h)	ASCII	Frame Duration	Informa
1.042500000...	Wakeup							1.458 ms	
2.501000000...	LIN Frame	B1	31	2	EA 8B 48 3F ED 9C B5 A7	1A	..H?....	6.822 ms	
9.376500000...	LIN Frame	25	25	0	31 B4 2C 3F	AE	1.,?	4.791 ms	
14.16800000...	Diagnostic Frame	3C	3C	0	00 FF FF FF FF FF FF FF	00	.....	6.458 ms	
20.62650000...	Wakeup							1.458 ms	
22.08500000...	LIN Frame	B1	31	2	EA 8B 48 3F ED 9C B5 A7	1A	..H?....	6.822 ms	
28.96050000...	LIN Frame	25	25	0	31 B4 2C 3F	AE	1.,?	4.791 ms	

Line Decoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes:

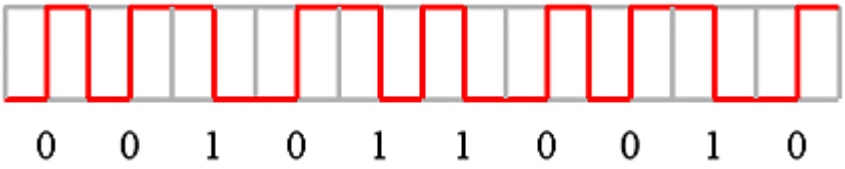
NRZI (Transition occurs for a one): A 1 is represented by a transition of the physical level, a 0 has no transition.

NRZI (Transition occurs for a zero): A 0 is represented by a transition of the physical level, a 1 has no transition.

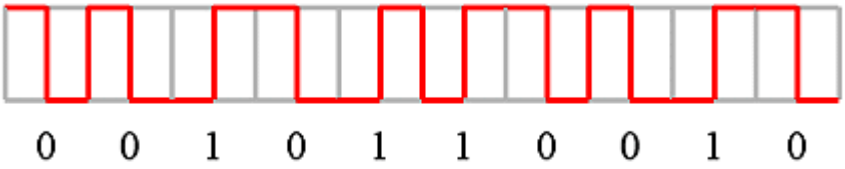


Manchester: In telecommunication, Manchester code is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. There are three modes:

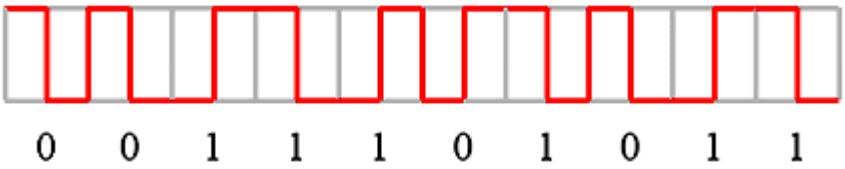
Manchester (Thomas): A 0 is expressed by a low-to-high transition, a 1 by high-to-low transition.



Manchester (IEEE802.3): A 1 is expressed by a low-to-high transition, a 0 by high-to-low transition.

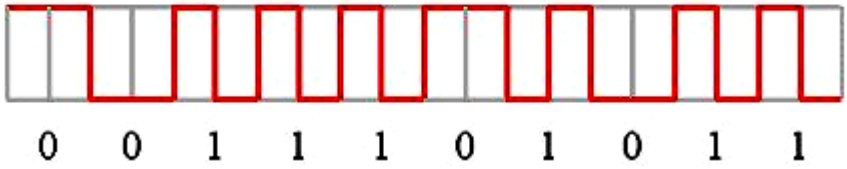


Differential Manchester: A 1 bit is indicated by making the first half of the signal equal to the last half of the previous bit's signal i.e. no transition at the start of the bit-time. A '0' bit is indicated by making the first half of the signal opposite to the last half of the previous bit's signal i.e. a zero bit is indicated by a transition at the beginning of the bit-time. In the middle of the bit-time there is always a transition, whether from high to low, or low to high. A reversed scheme is possible, and no advantage is given by using either scheme.



Bi-phase Mark: The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions which makes clock recovery and synchronization difficult. When

encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that together form a bit.

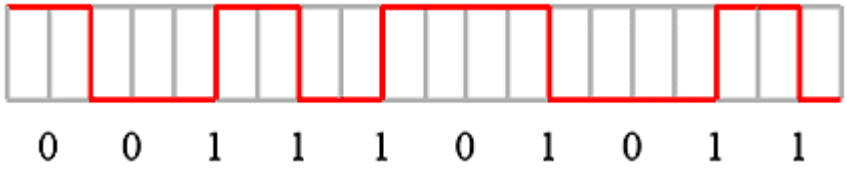


Miller: Delay encoding is also known as Miller encoding.

In telecommunications, delay encoding is the encoding of binary data to form a two-level signal such that (a) a "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period; and (b) a "1" causes a transition from one level to the other in the middle of the bit period.

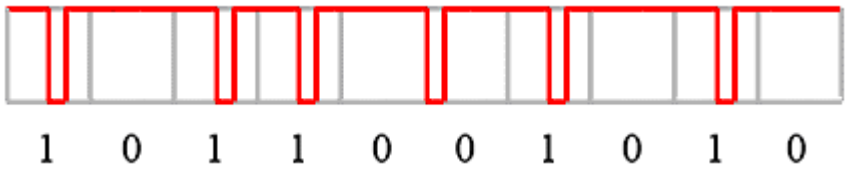
Delay encoding is used primarily for encoding radio signals because

the frequency spectrum of the encoded signal contains less low-frequency energy than a conventional non-return-to-zero (NRZ) signal and less high-frequency energy than a bi-phase signal.

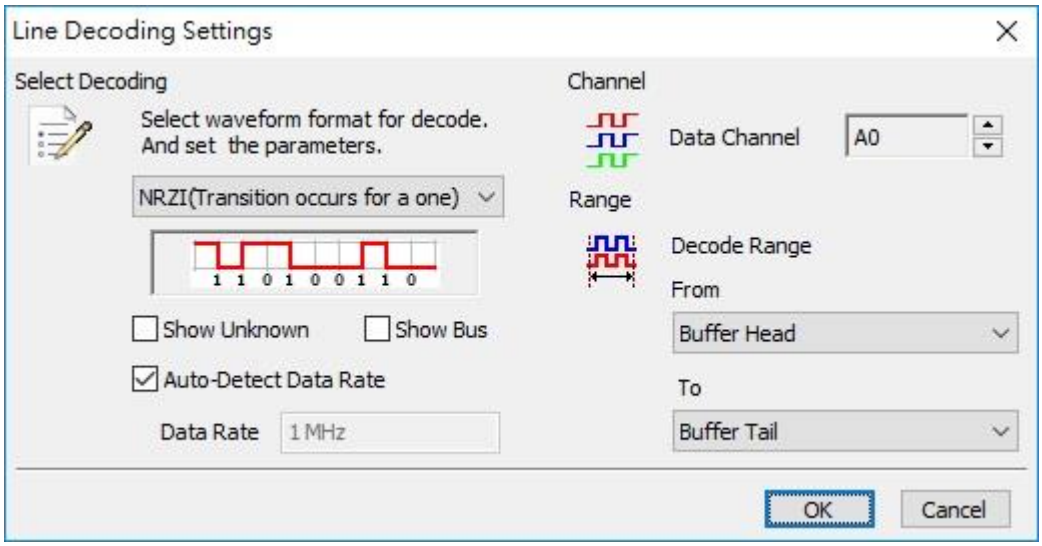


Modified Miller: The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation data demodulation circuit for producing NRZ - L data by utilizing the clock bits, data bits

and synchronizing clock pulses which are output from the data separation circuit. This structure enables the M 2 modulation data which is input to the M 2 demodulation circuit to be easily demodulated to an NRZ - L type data signal by means of a very simple circuit structure. An example is as below:



Settings



Select Decoding: Select the line code you want to decode.

Show Unknown: Display unknown data.

Show Bus: Display bus data.

Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Date Rate is not selected.

Channel: Show the selected channel (CH 0).

Range: Select the range within the waveform you want to decode.

Line Encoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes:

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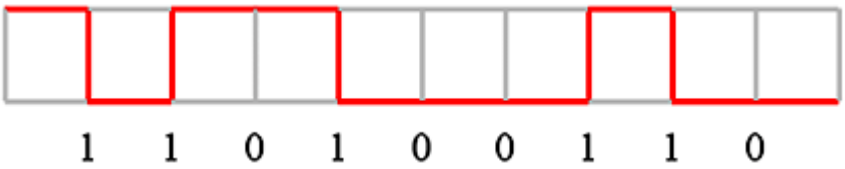
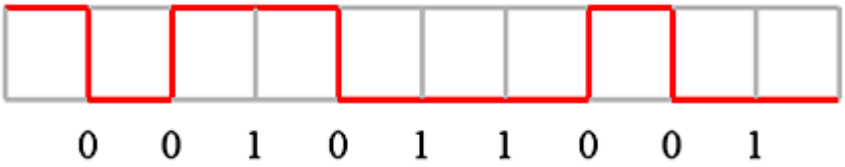


NRZI (Transition occurs for a zero): A 0 is represented by a transition of the physical level, a 1 has no transition.



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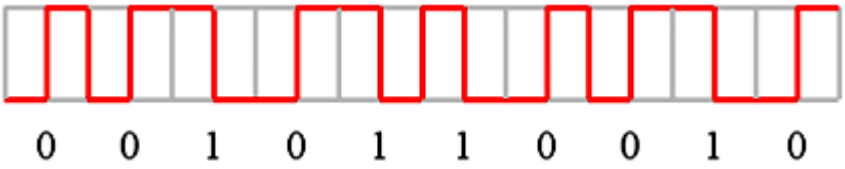
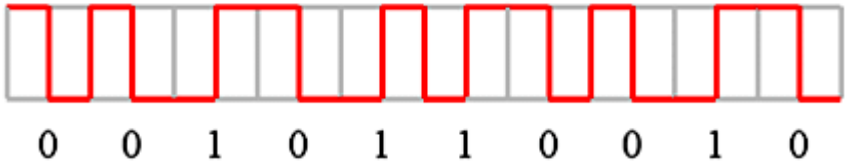


Manchester (IEEE802.3): A 1 is expressed by a low-to-high transition, a 0 by high-to-low transition.



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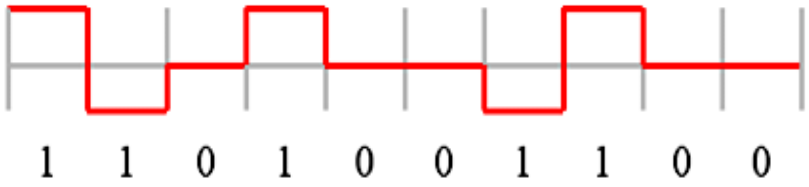
AMI (Alternate Mark Inversion): There are four modes:

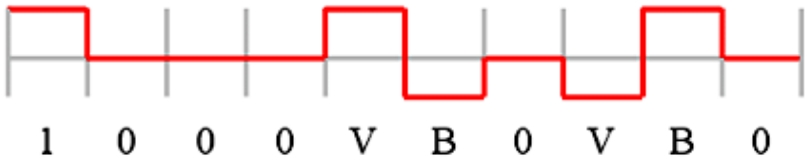
AMI (Standard): AMI (Alternate Mark Inversion) is a synchronous clock encoding technique that uses bipolar pulses to represent logical 1 value. It is therefore a three level system. A logical 0s is represented by no symbol, and a logical 1 is represented by alternating-polarity pulses.



AMI (B8ZS): Bipolar-8-Zero Substitution

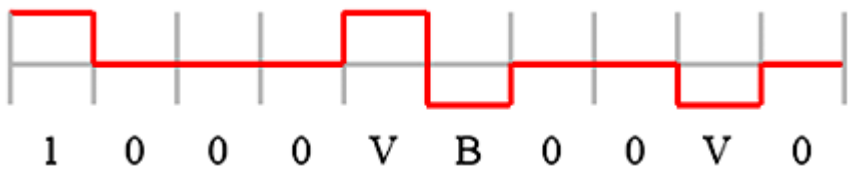
If 1 is +, 00000000 is represented to 000+-0-+

1 is -, 00000000 is represented to 000-+0+-



AMI (HDB3): High Density Bipolar 3

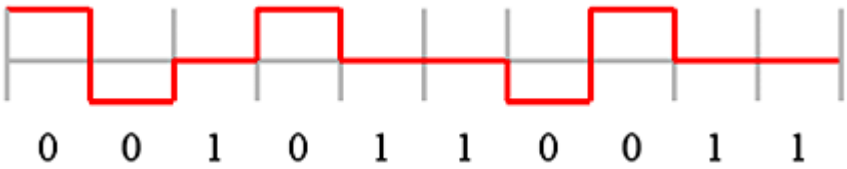
The HDB3 code is a bipolar signaling technique (i.e. relies on the transmission of both positive and negative pulses). It is based on Alternate Mark Inversion (AMI), but extends this by inserting violation codes whenever there is a run of 4 or more 0's. This and similar (more complex) codes have replaced AMI in modern distribution networks. The encoding rules follow those for AMI, except that sequences of four consecutive 0's are encoding using a special "violation" bit. This bit has the same polarity as the last 1-bit which was sent using the AMI encoding rule. The purpose of this is to prevent long runs of 0's in the data stream that may otherwise prevent a DPLL from tracking the center of each bit. Such a code is sometimes called a "run length limited" code, since it limits the runs of 0's that would otherwise be produced by AMI. One refinement is necessary, to prevent a dc voltage being introduced by excessive runs of zeros. This refinement is to encode any pattern of more than four bits as B00V, where B is a balancing pulse. The value of B is assigned as + or -, so as to make alternate "V"s of opposite polarity. The receiver removes all Violation pulses, but in addition a violation preceded by two zeros and a pulse is treated as the "B00V" pattern and both the violation and balancing pulse are removed from the received bit stream. This restores the original bit stream.



MLT-3: Multilevel Transmission 3: A 0 means no transition happens, a 1 is

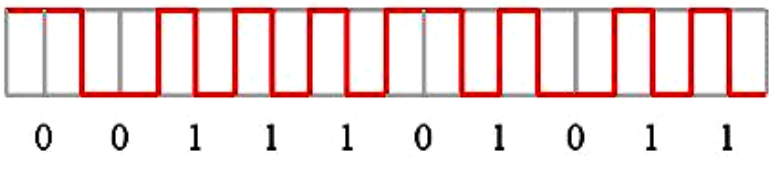
represented by a transition (0, +, 0, -).

Pseudoternary: A 1 is always zero, a 0 is represented by a transition (+, -).



CMI (Coded Mark Inversion): A zero is sent a low to high [01] transition, while a one is sent as either a one [1] or zero [0] depending on the previous state. If the previous state was high the one is sent as a zero [0], if it was low the one is sent as a one [1].

Bi-phase Mark: The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions that make clock recovery and synchronization difficult. When encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that form a bit.



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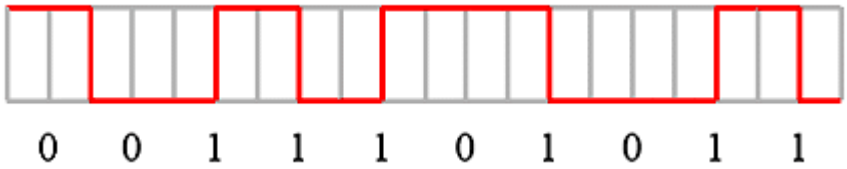
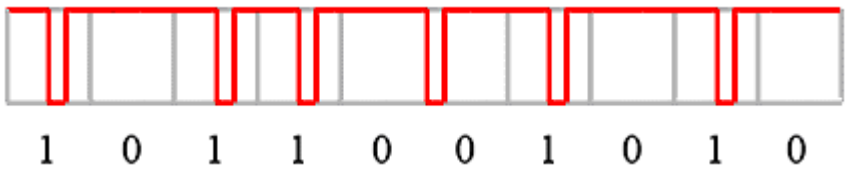
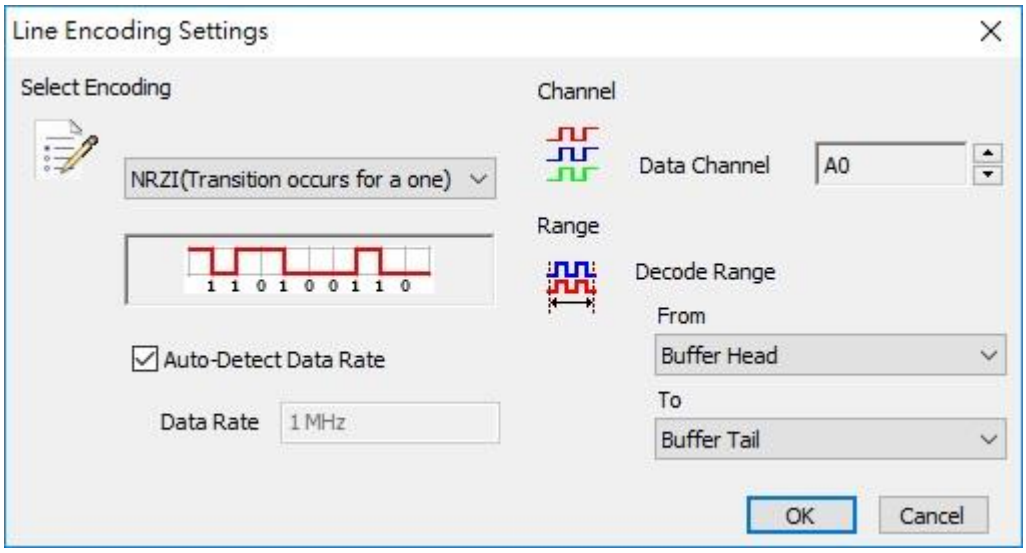


Modified Miller: The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation data demodulation circuit for producing NRZ - L data by utilizing the clock bits, data bits and synchronizing clock pulses which are output from the data separation circuit. This structure enables the M 2 modulation data which is input to the M 2 demodulation circuit to be easily demodulated to an NRZ - L type data signal by means of a very simple circuit structure. An example is as below:



Settings



Select Encoding: Select the line code you want to encode.

Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Date Rate is not selected.

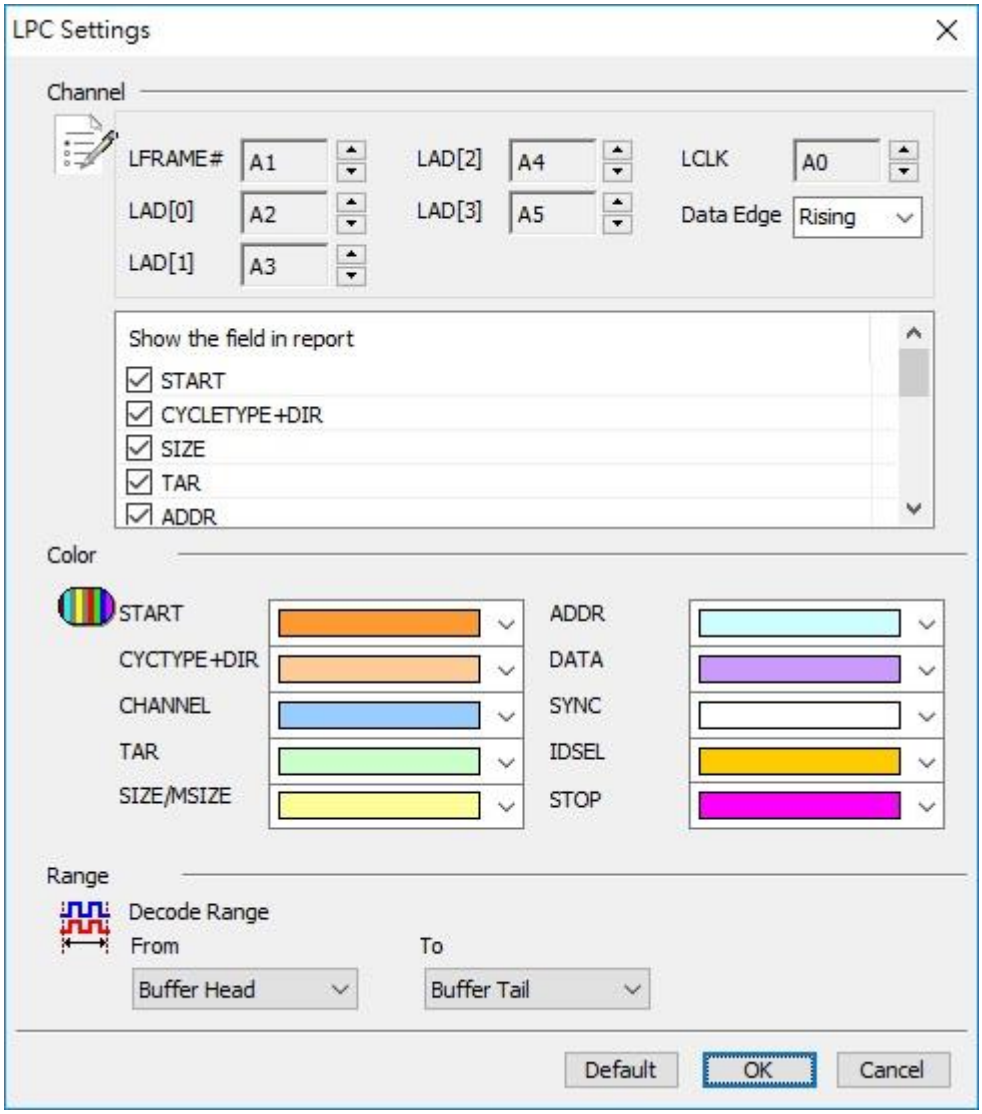
Channel: Show the selected channel (CH 0).

Range: Select the range within the waveforms you want to encode.

Low Pin Count (LPC)

The LPC bus, for the data transmissions, was developed by Intel to replace the ISA bus.

Settings



Channel: Show the selected channels.

LFRAME#: Frame indicator.

LAD[0-3]: Data bits.

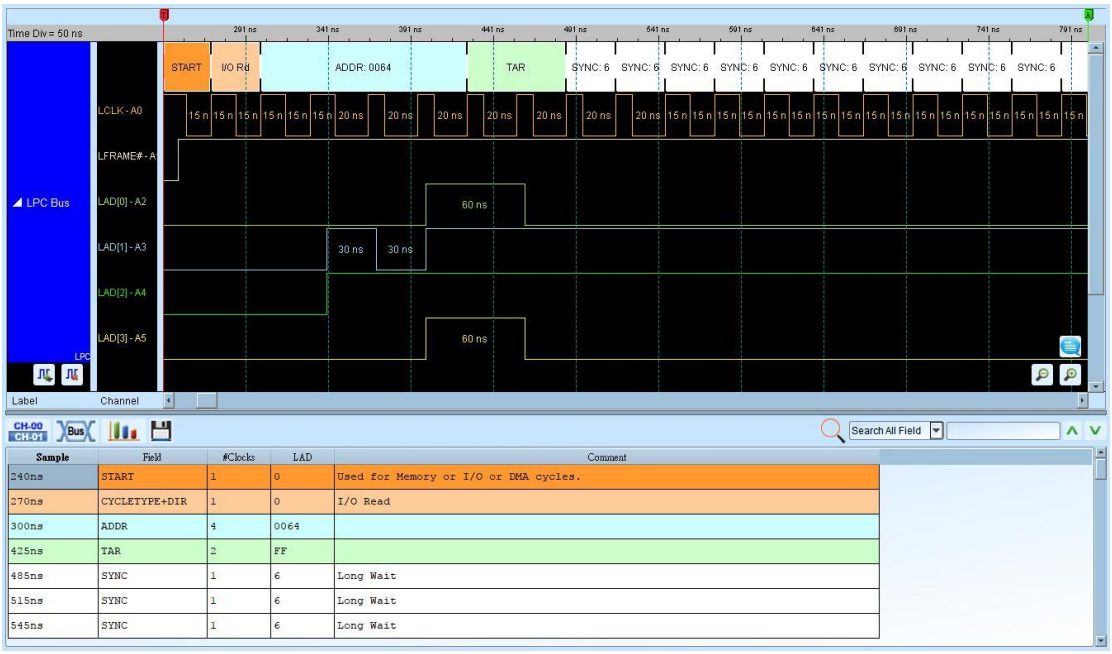
LCLK: Clock.

Filter the data in the report window: You can filter the data in the Report Window.

Result

Click **OK** to run the LPC decode and see the result on the Waveform Window below.

I/O Read Cycle.

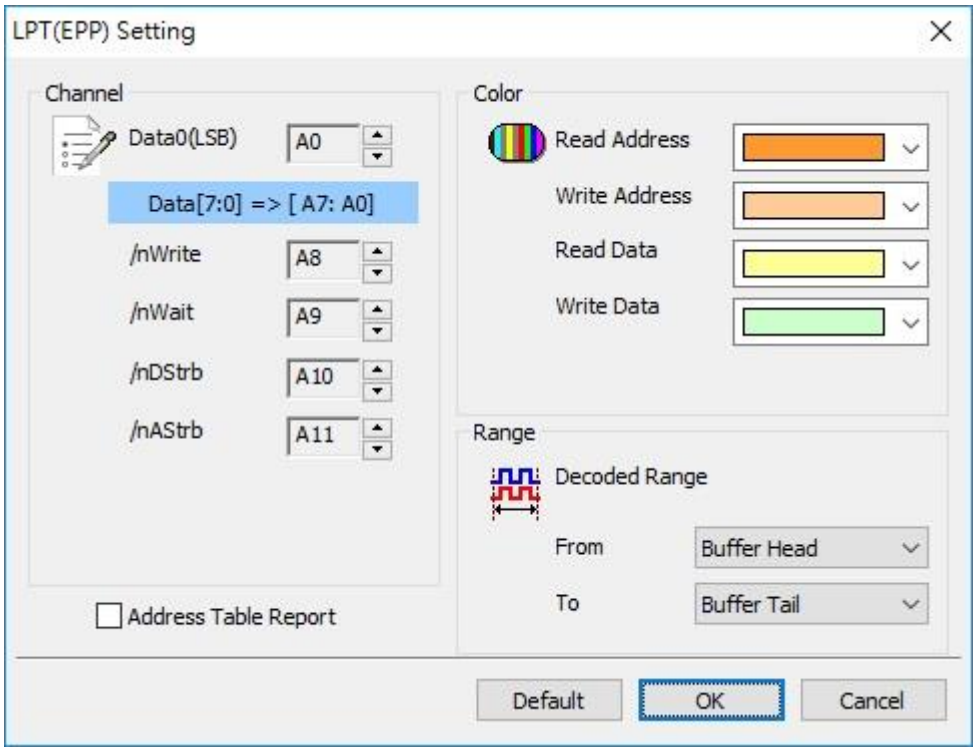


Sample	Field	#Clocks	LAD	Comment
240ns	START	1	0	Used for Memory or I/O or DMA cycles.
270ns	CYCLETYPE+DIR	1	0	I/O Read
300ns	ADDR	4	0064	
425ns	TAR	2	FF	
485ns	SYNC	1	6	Long Wait
515ns	SYNC	1	6	Long Wait
545ns	SYNC	1	6	Long Wait

Line Printer Terminal Port (LPT)

LPT is a universal parallel interface that use in PC since 1980's. It was primarily designed to operate a line printer, but could also be used to adapt other peripherals. This decode only support EPP Mode.

Settings



Data0(LSB): There are 8 data channel. Only set Data0(LSB) here, other channel will be set automatically.

/nWrite: Indicates the direction of transfer.

/nWait: To acknowledge that a transfer has finished.

/nDStrb: Indicates the data cycle.

/nAStrb: Indicates the address cycle.

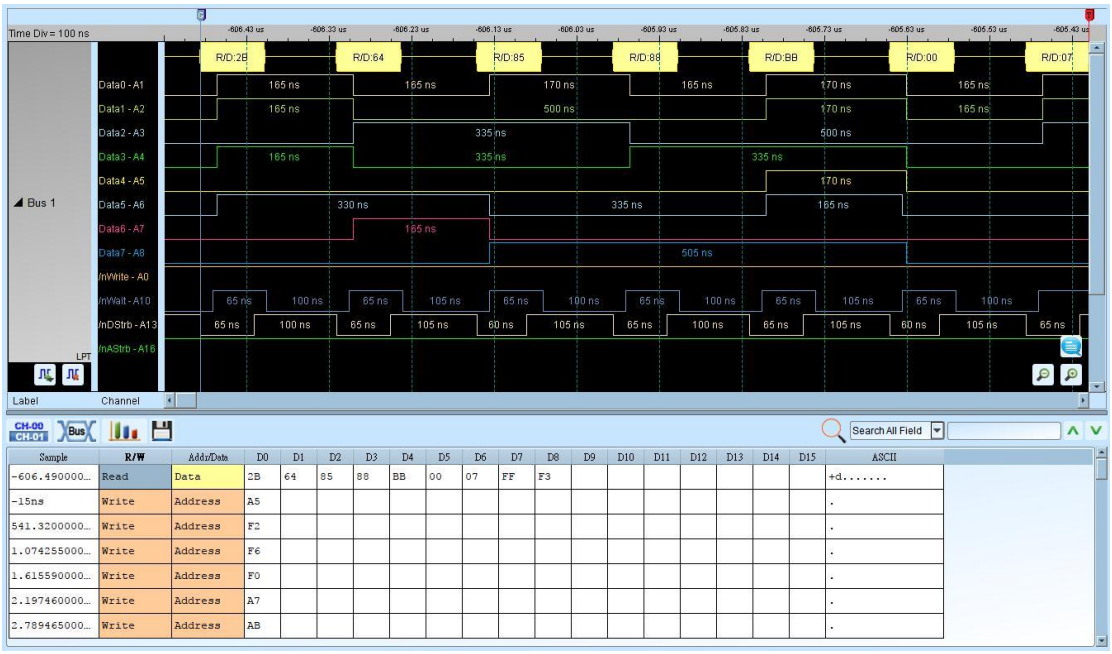
/nInit: Indicates a termination cycle in order to return the interface to the

Compatibility mode. User can option to use this channel or not.

/nIntr: This is an interrupt signal. User can option to use this channel or not.

Result

Click OK to run the LPT Decode and see result on the Waveform Windows below.

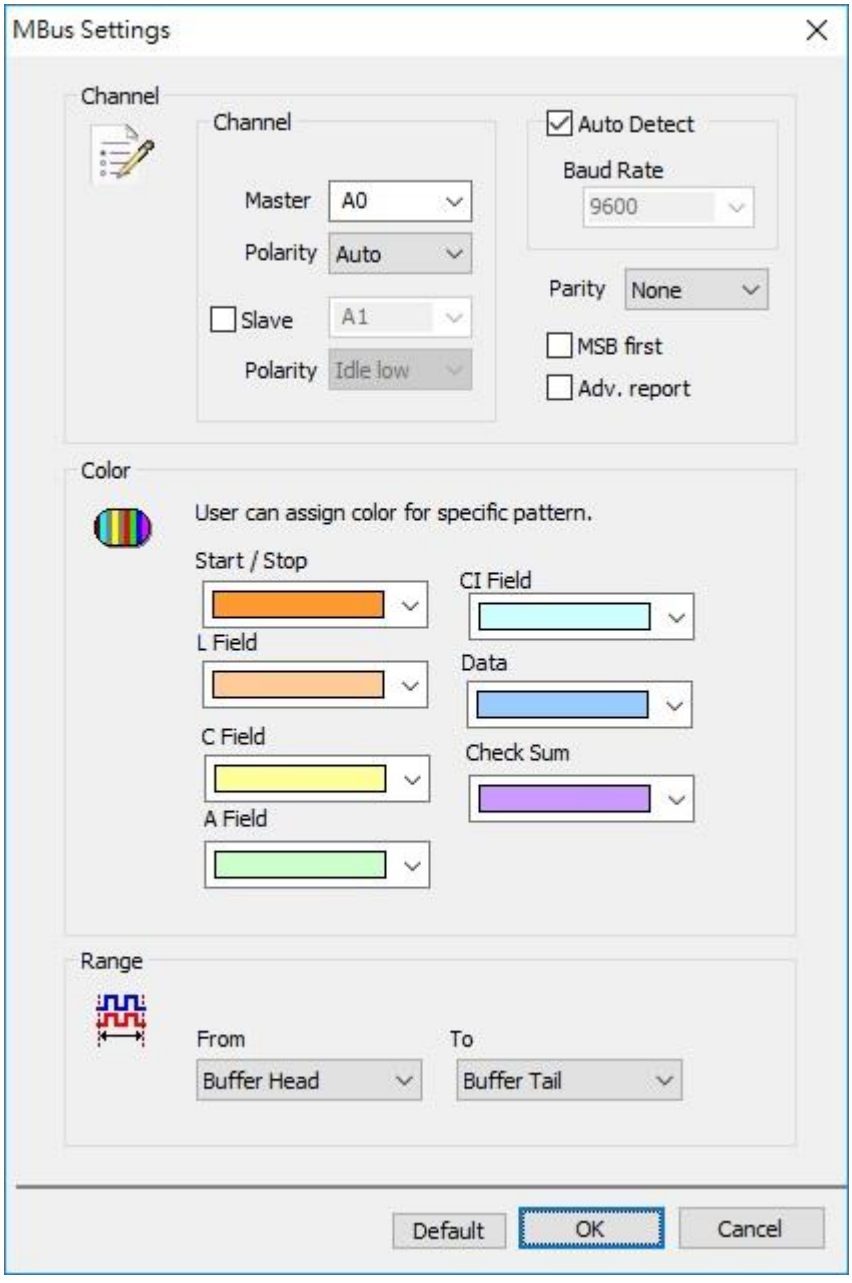


Sample	R/W	Addr/Data	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	ASCII
-606.490000...	Read	Data	2B	64	85	88	BB	00	07	FF	F3								+d.....
-15ns	Write	Address	A5																.
541.3200000...	Write	Address	F2																.
1.074255000...	Write	Address	F6																.
1.615590000...	Write	Address	F0																.
2.197460000...	Write	Address	A7																.
2.789465000...	Write	Address	AB																.

M-Bus

M-Bus (Meter-Bus) is for remote reading of heat meters and other types of consumption meters.

Settings



Channel: Set the channel of the signal and Polarity.

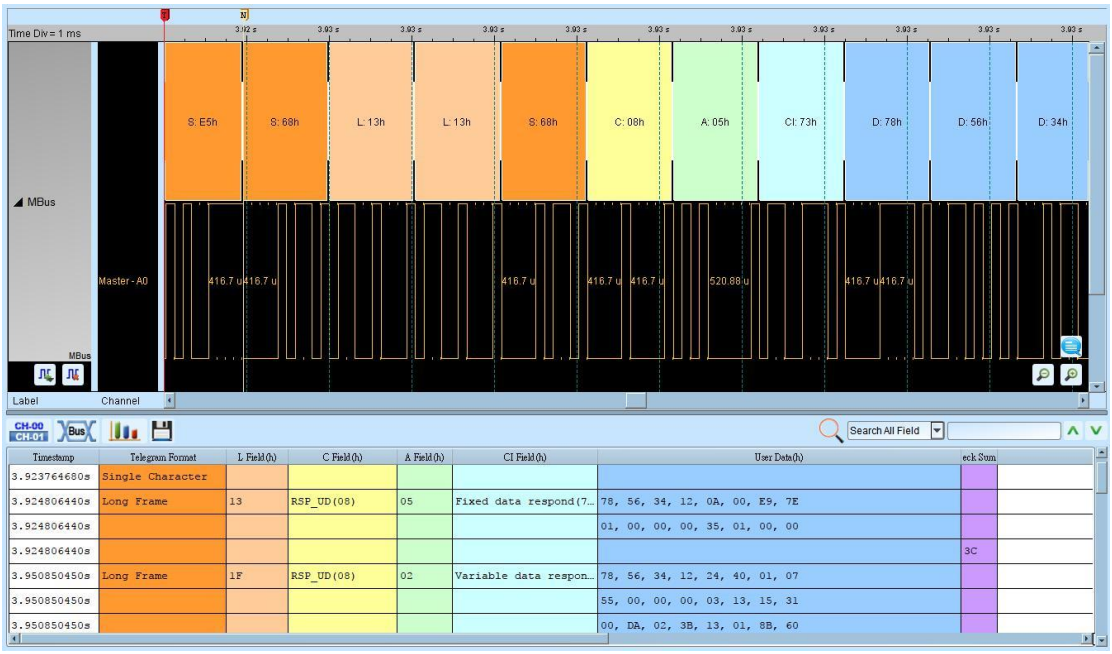
Baud rate: Set the specific data rate or auto detection.

Parity: Error detection.

MSB first: Set MSB format.

Adv. Report: Advanced report.

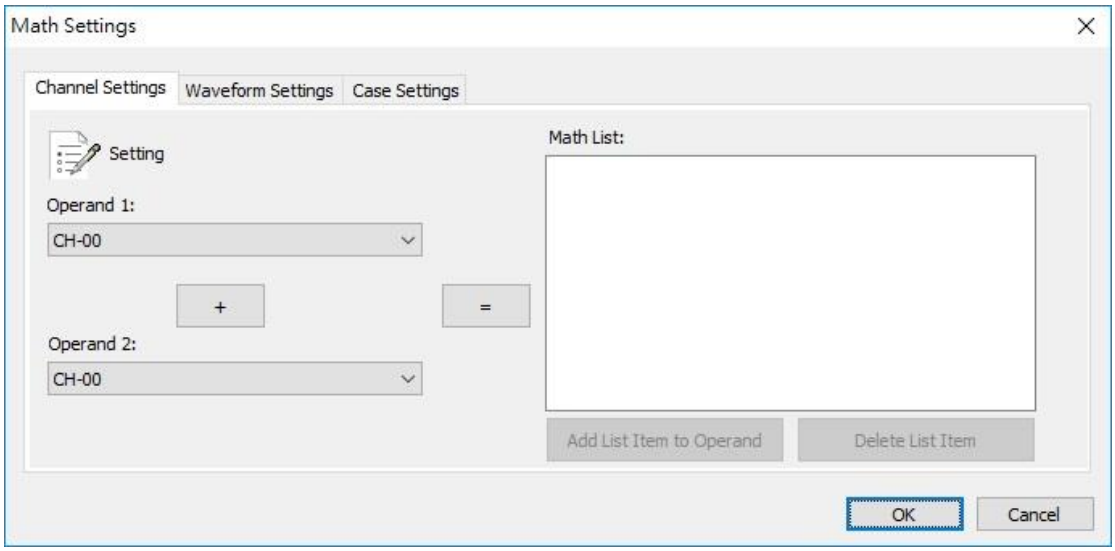
Result



Math

Math is used to conduct addition, subtraction, multiplication, division, AND, XOR, OR,NAND, NOR, XNOR operation for the channel or combined channels.

Settings



Operand: Select the channel(s) in the waveform window.

"+": Select "+", "-", "X", "/", "AND", "XOR", "OR" , "NAND", "NOR", "XNOR" operator.

"=": Add operation type.

Add List Item to Operand: Add operation type to operand.

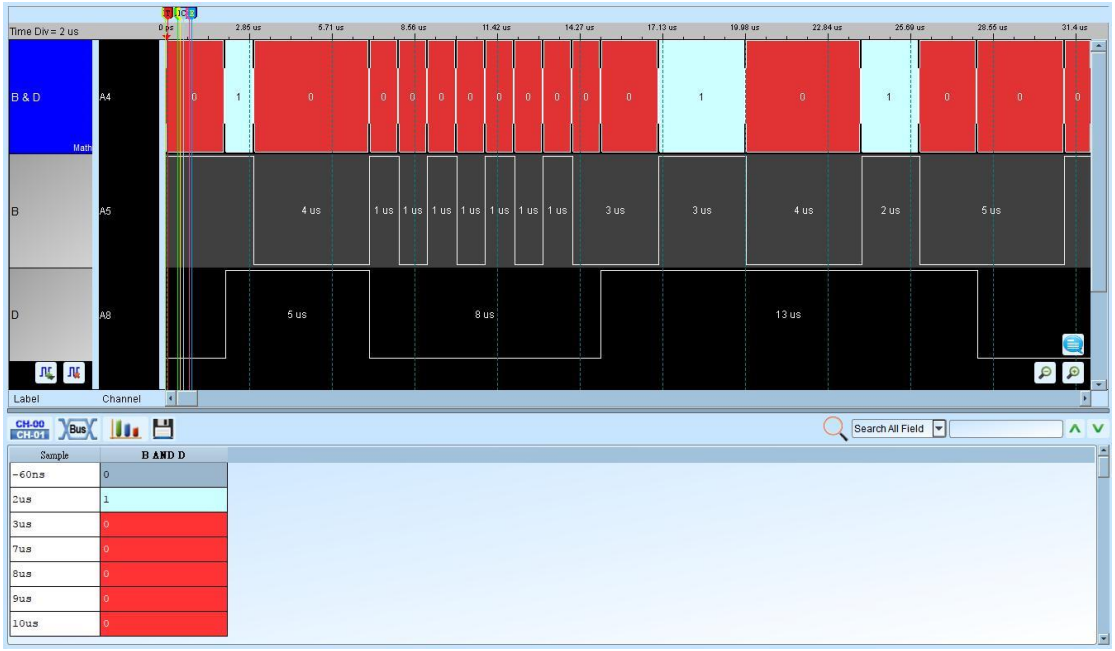
Delete List Item: Delete operation type from the list.

Color: Set the colors for the data bits.

Range: Select the range within the waveform you want to decode.

Case Settings: Select condition and frame color.

Result

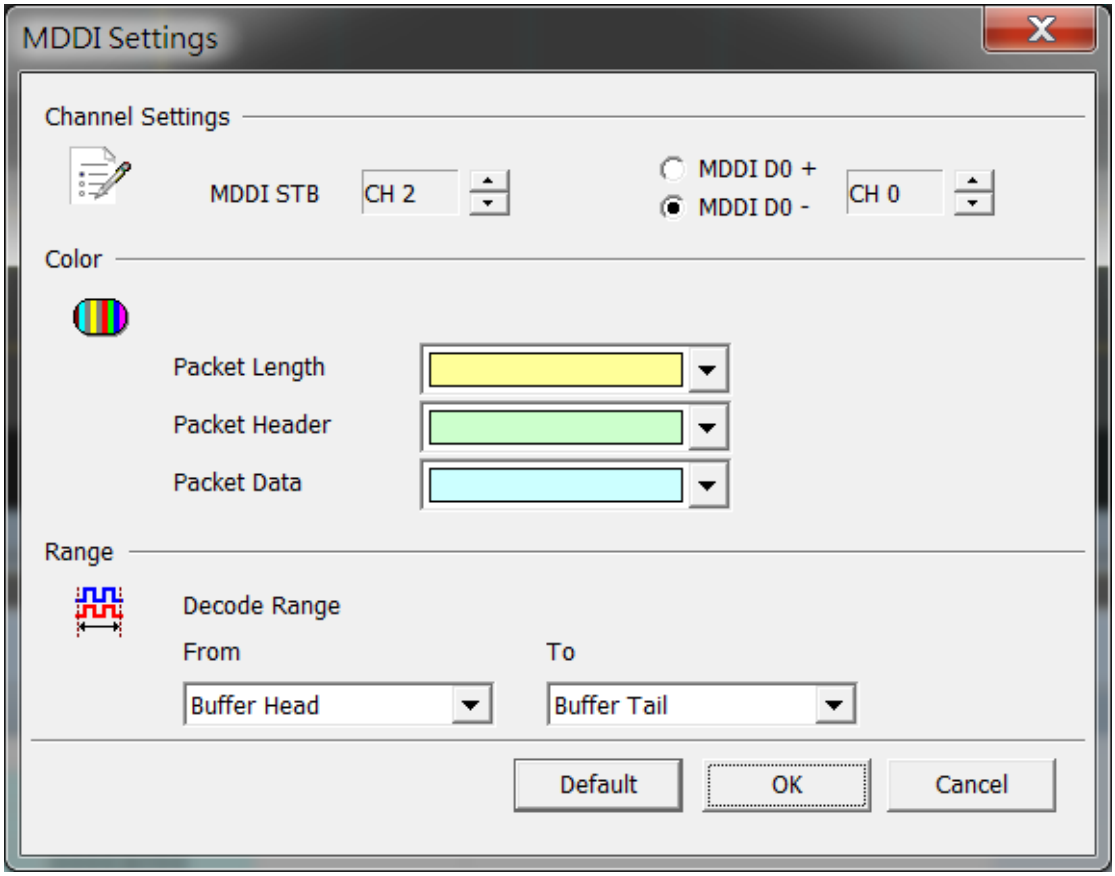


Note: When the Math settings are finished, the settings will always be saved as an independent text file named as AqMath.txt, different from the waveform file, at work directory unless other name assigned. If you need the specific Math settings, please save it, so you can reload the settings next time you open the specific waveform file.

Mobile Display Digital Interface (MDDI)

The Mobile Display Digital Interface (MDDI) is a cost-effective low-power solution that enables high-speed short-range communication with a display device using a digital packet data link for connecting portable computing, communication, and entertainment devices to wearable micro displays. This decoder is based on VESA Mobile Display Digital Interface Standard Version 1.2, only Type I communication is supported in this decoder.

1. MDDI Parameter Settings



Channel Settings

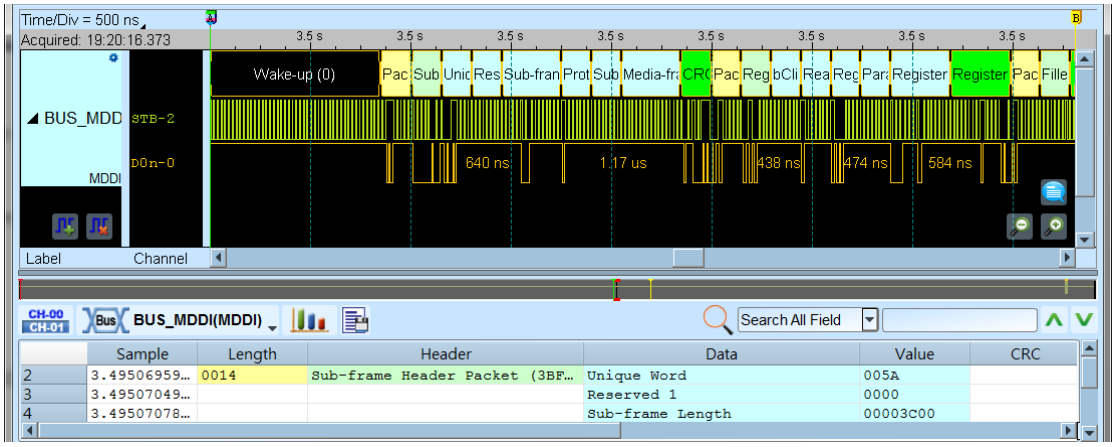
MDDI STB: MDDI Strobe

MDDI D0+/-: MDDI Data 0 +/-

Configure the Channel setup for the decoder, and choose the data source

from Data 0+ or Data 0-.

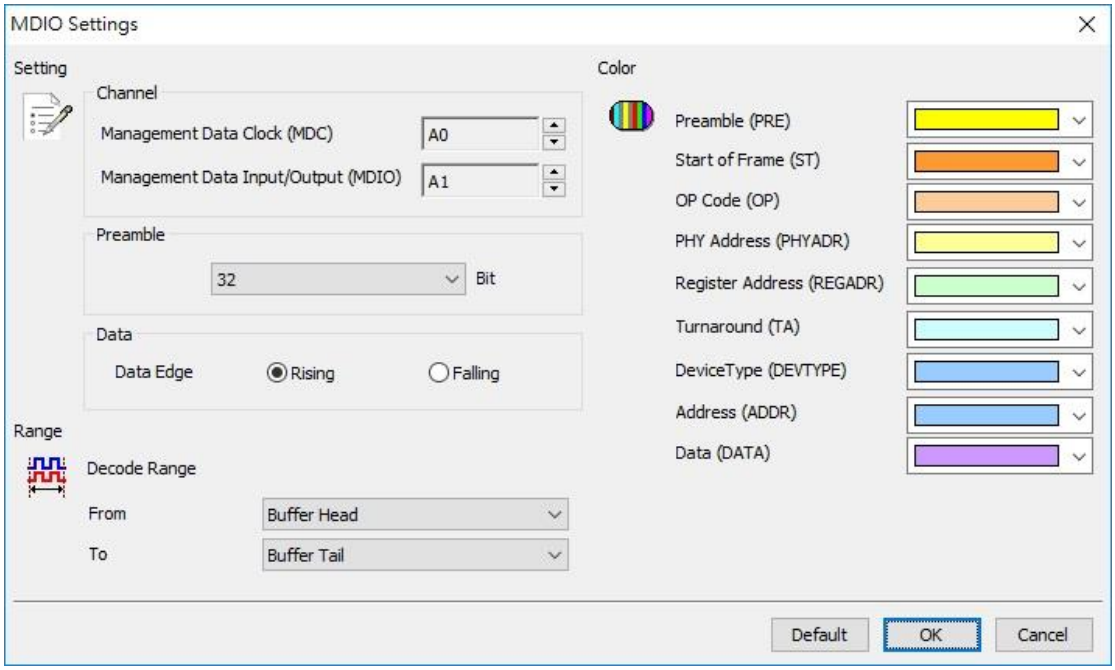
2. Result



MDIO

MDIO, also known as Serial Management Interface (SMI), is a serial bus defined for the Ethernet IEEE 802.3 specification for Media Independent Interface, or MII.

Settings



MDC: Clock.

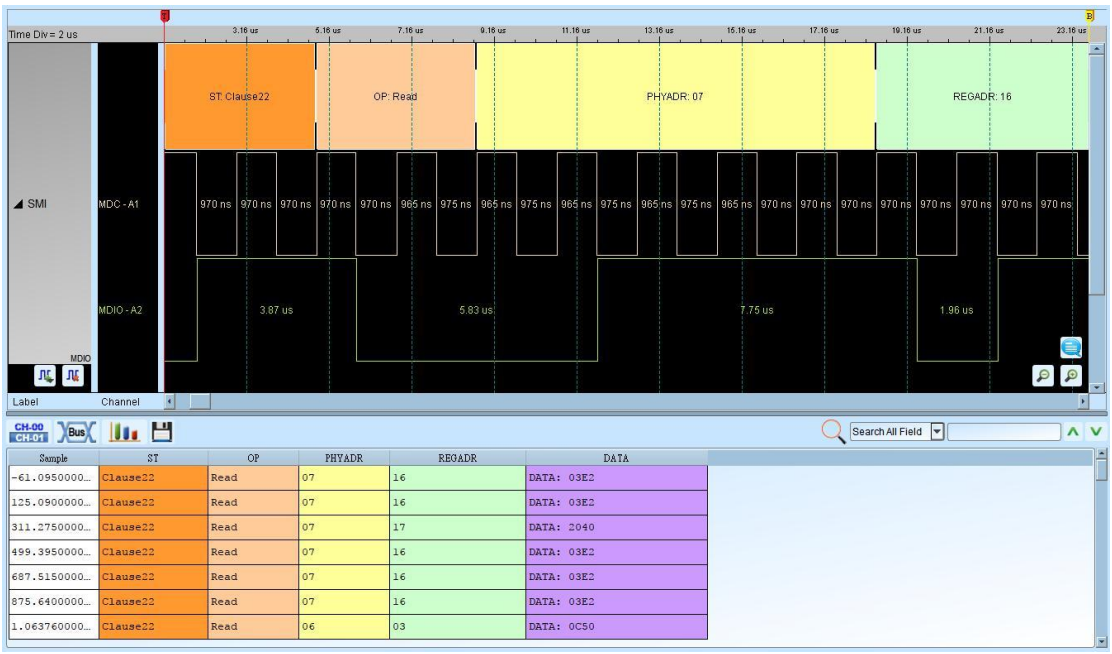
MDIO: Data Input / Output.

Preamble: Set the MDIO preamble width, 32 bit default.

Data Edge: Set the MDC Rising/Falling edge to latch the data field, Rising Edge default.

Result

Click **OK** to run the MDIO decode and see the result on the Waveform Window below.

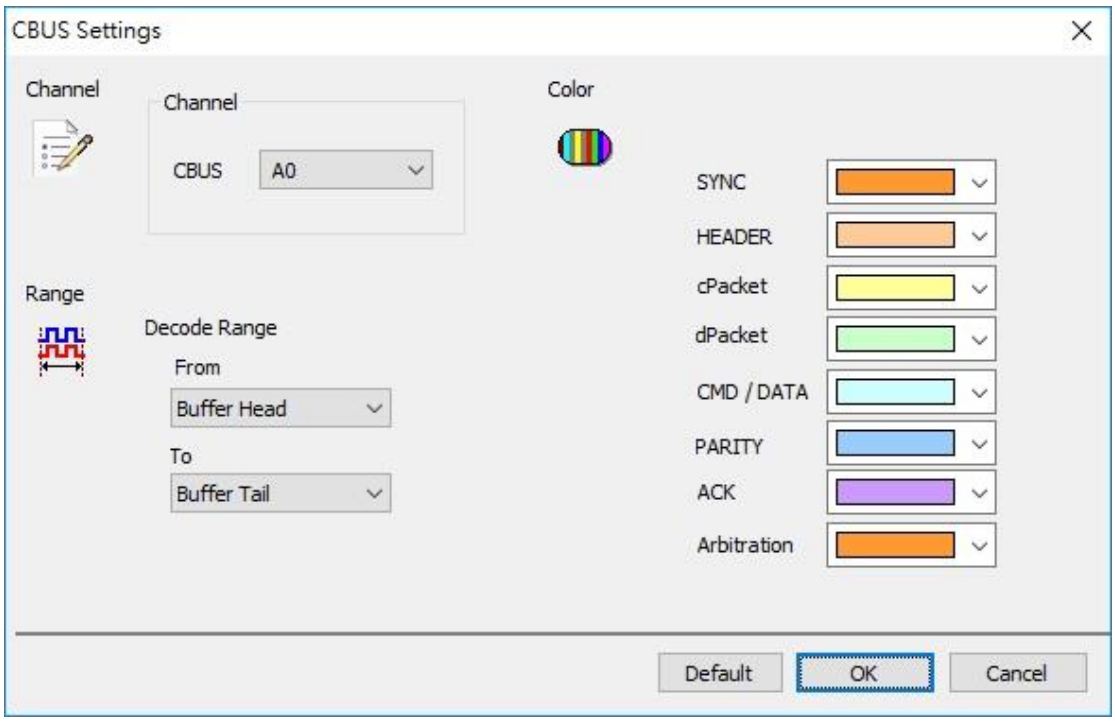


Sample	ST	OP	PHYADR	REGADR	DATA
-61.0950000...	Clause22	Read	07	16	DATA: 03E2
125.0900000...	Clause22	Read	07	16	DATA: 03E2
311.2750000...	Clause22	Read	07	17	DATA: 2040
499.3950000...	Clause22	Read	07	16	DATA: 03E2
687.5150000...	Clause22	Read	07	16	DATA: 03E2
875.6400000...	Clause22	Read	07	16	DATA: 03E2
1.063760000...	Clause22	Read	06	03	DATA: 0C50

MHL-CBUS

Mobile High-definition Link (MHL) is an HD audio and video interface, Control Bus (CBUS) is used to control it.

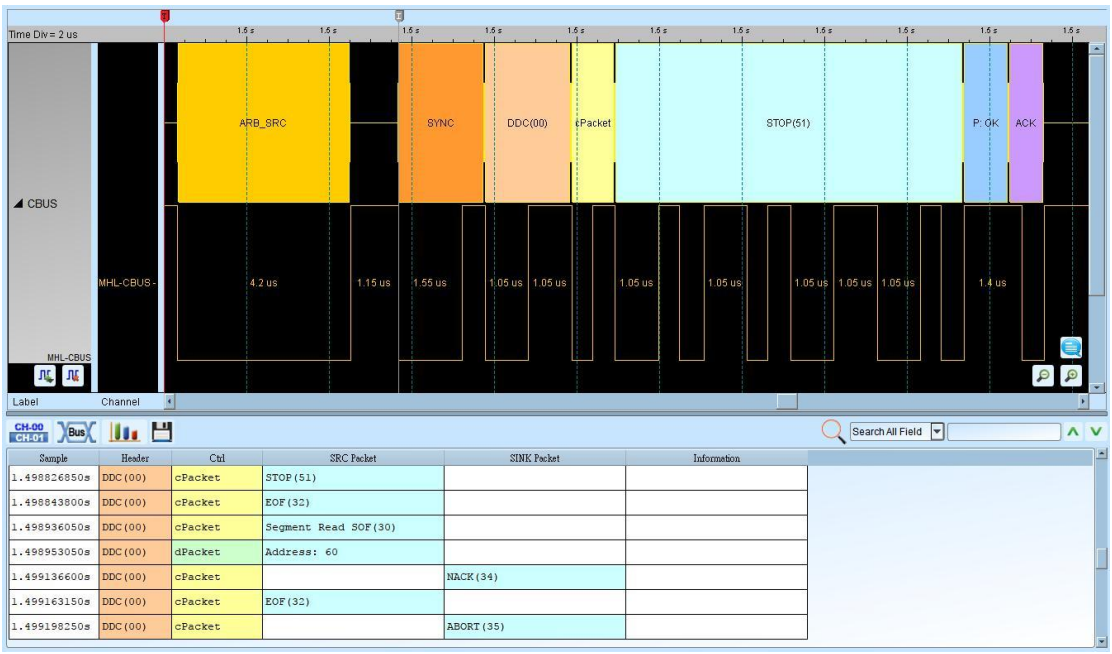
Settings



LA Channel: Show the selected channel (CH0).

Result

Click OK to run the MHL-CBUS Decode and see result on the Waveform Window below.

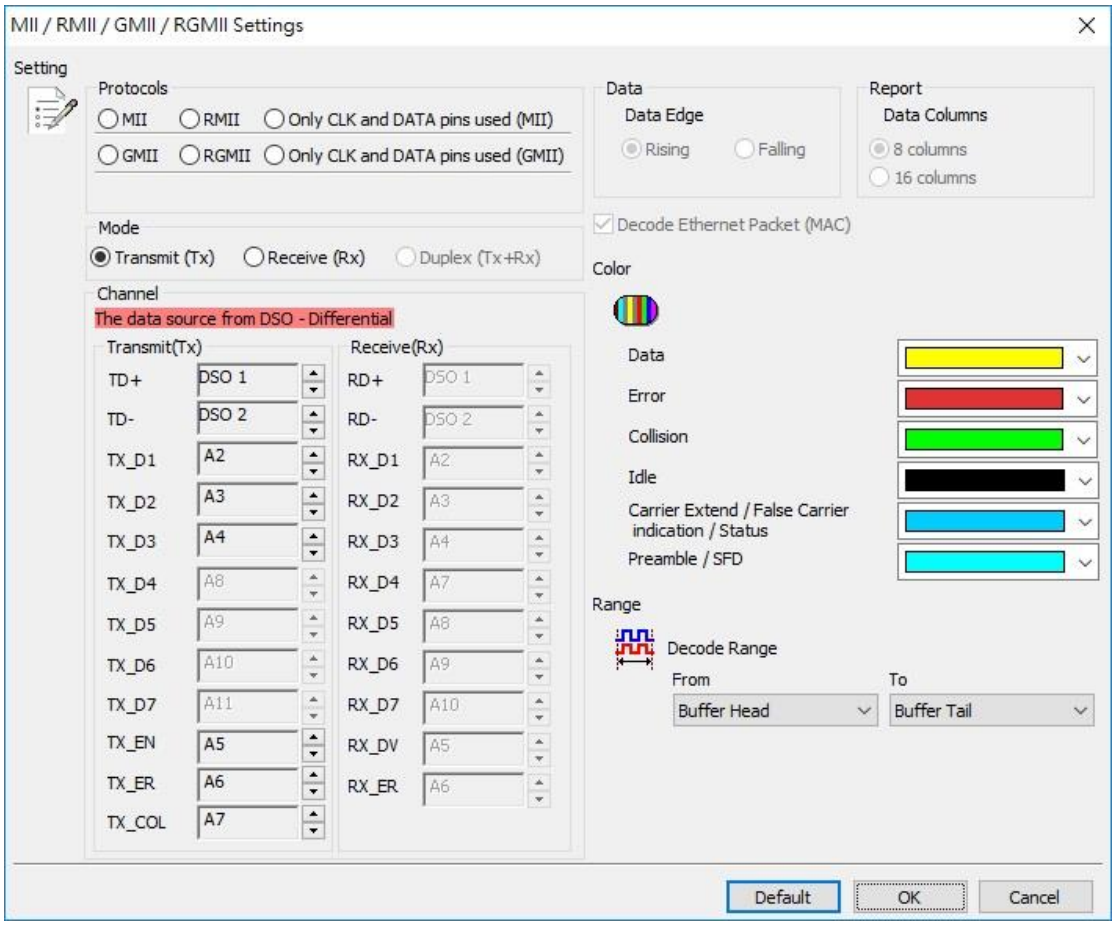


Sample	Header	Ctrl	SRC Packet	SINK Packet	Information
1.498826850s	DDC(00)	cPacket	STOP(51)		
1.498843800s	DDC(00)	cPacket	EOF(32)		
1.498936050s	DDC(00)	cPacket	Segment Read SOF(30)		
1.498953050s	DDC(00)	dPacket	Address: 60		
1.499136600s	DDC(00)	cPacket		NACK(34)	
1.499163150s	DDC(00)	cPacket	EOF(32)		
1.499198250s	DDC(00)	cPacket		ABORT(35)	

MII/RMII

MII/RMII (Media Independent Interface/Reduced Media Independent Interface) is a protocol formulated by 802.3u that applied to Fast Ethernet, connecting MAC of Data Link Layer and PHY layer. Its clock frequency is either 25MHz or 2.5MHz (Ethernet); they are TX_CLK and RX_CLK. TX [0:3], RX [0:3] are 4-bit-width bus and TX_EN, RX_EN enable the IN/OUT; TX_ER, RX_ER can detect the errors on the bus; RX_DV inform bus the data received is valid or not; COL can detect the collision on the bus. **Serial Management Interface (SMI), also known as MDIO, is also an important part of MII.**

Settings



MII / RMII: Select the MII / RMII bus decode

GMII / RGMII: Select the GMII / RGMII bus decode

Only CLK and Data pins used(M/G): Select MII / GMII the CLK and Data pins only**.**

Transmit (Tx): Select TX mode

Receive (Rx): Select Rx mode

Duplex (Tx+Rx) : Select duplex mode

Channel: Set the channel number.

Rising: Select rising edge to latch data

Falling: Select falling edge to latch data

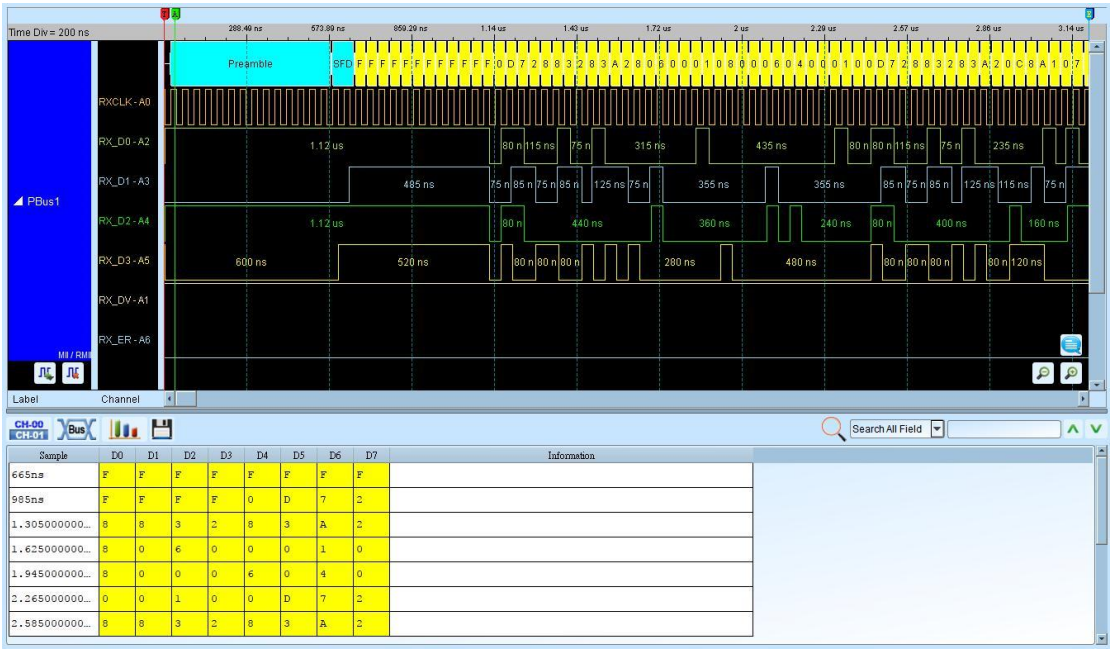
8 columns: show 8 columns data field in the report window

16 columns: show 16 columns data field in the report window

Result

Click **OK** to run the MII/RMII decode and see the result on the Waveform Window below.

MII

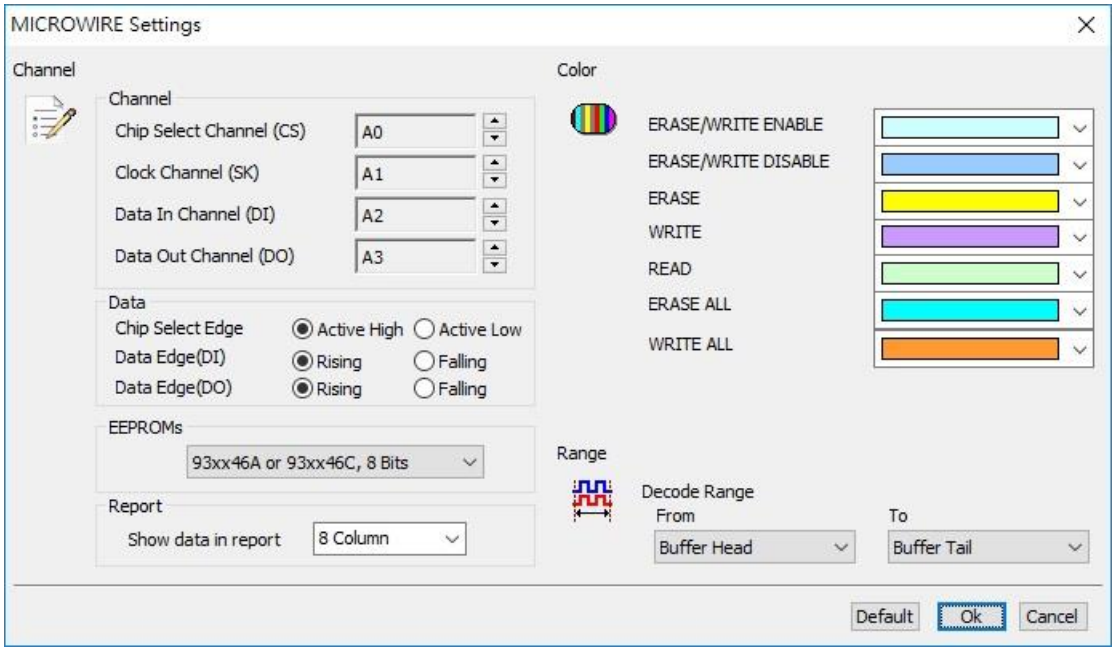


Sample	D0	D1	D2	D3	D4	D5	D6	D7	Information
665ns	F	F	F	F	F	F	F	F	
985ns	F	F	F	F	0	D	7	2	
1.305000000...	8	8	3	2	8	3	A	2	
1.625000000...	8	0	6	0	0	0	1	0	
1.945000000...	8	0	0	0	6	0	4	0	
2.265000000...	0	0	1	0	0	D	7	2	
2.585000000...	8	8	3	2	8	3	A	2	

Microwire

The Microwire bus has four data bits: Chip Select (CS), Serial Clock (SK), Data Input (DI), and Data Output (DO).

Settings



Channel: Show the selected channels.

Chip Select Edge: Active Low or Active High.

Data Edge: Rising or Falling.

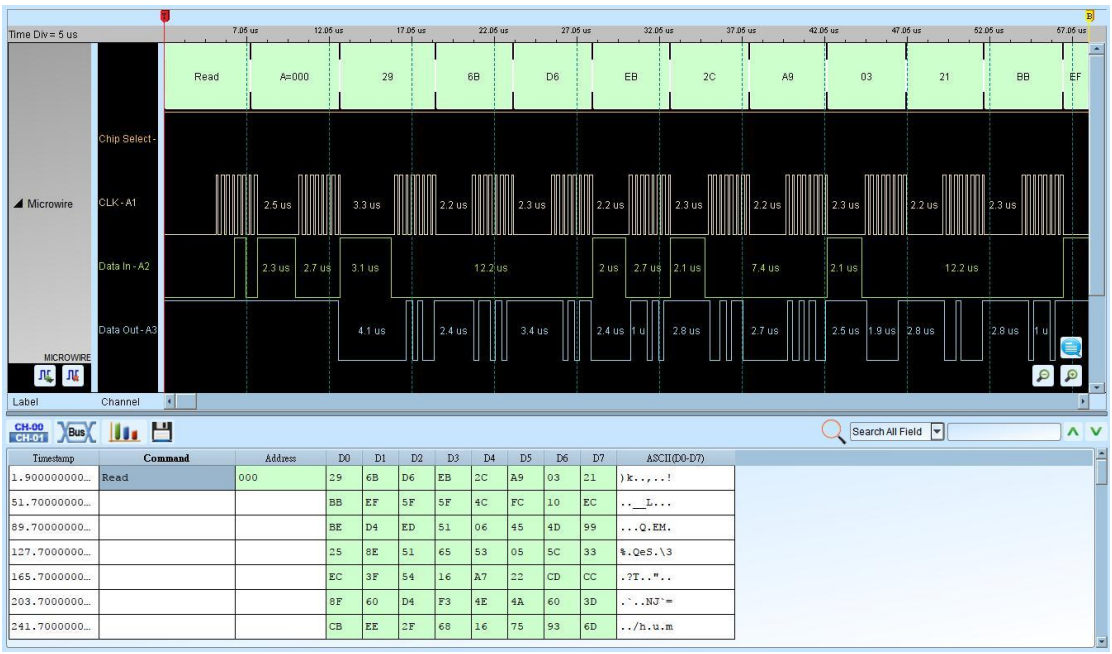
EEPROMs: Select EEPROMs.

Report: Show data in report.

Result

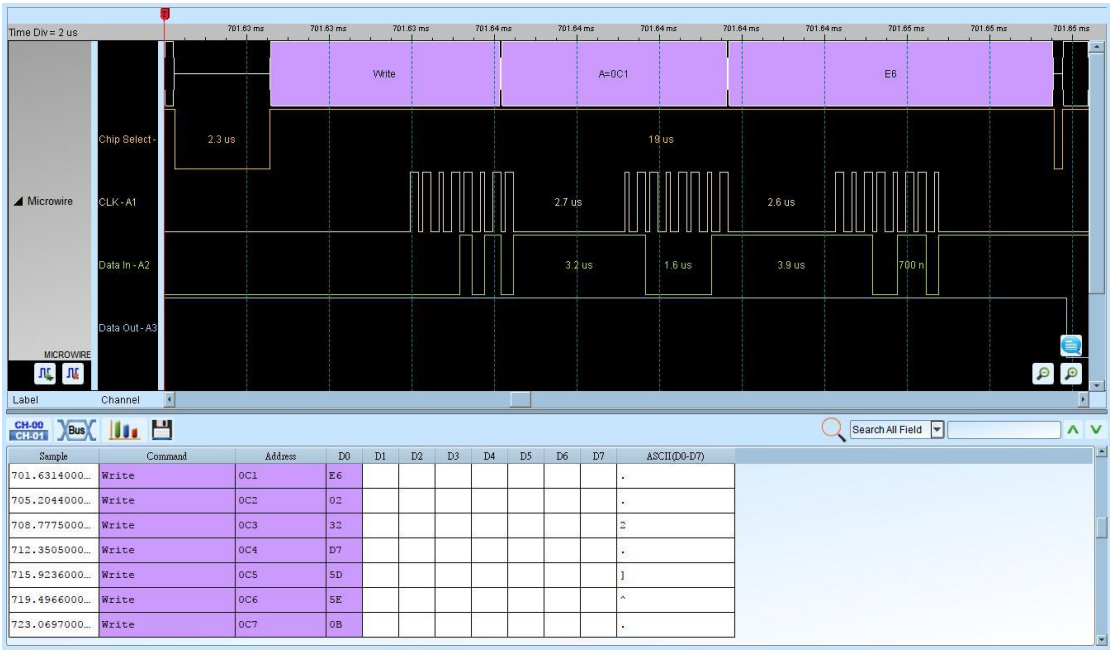
Click **OK** to run the Microwire decode and see the result on the Waveform Window below.

Read



Timestamp	Command	Address	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)
1.900000000...	Read	000	29	6B	D6	EB	2C	A9	03	21	)k.,..!
51.70000000...			BB	EF	5F	5F	4C	FC	10	EC	..__L...
89.70000000...			BE	D4	ED	51	06	45	4D	99	...Q.EM.
127.7000000...			25	8E	51	65	53	05	5C	33	%.QeS.\3
165.7000000...			EC	3F	54	16	A7	22	CD	CC	.?T.."..
203.7000000...			8F	60	D4	F3	4E	4A	60	3D	.`..NJ`=
241.7000000...			CB	EE	2F	68	16	75	93	6D	../h.u.m

Write

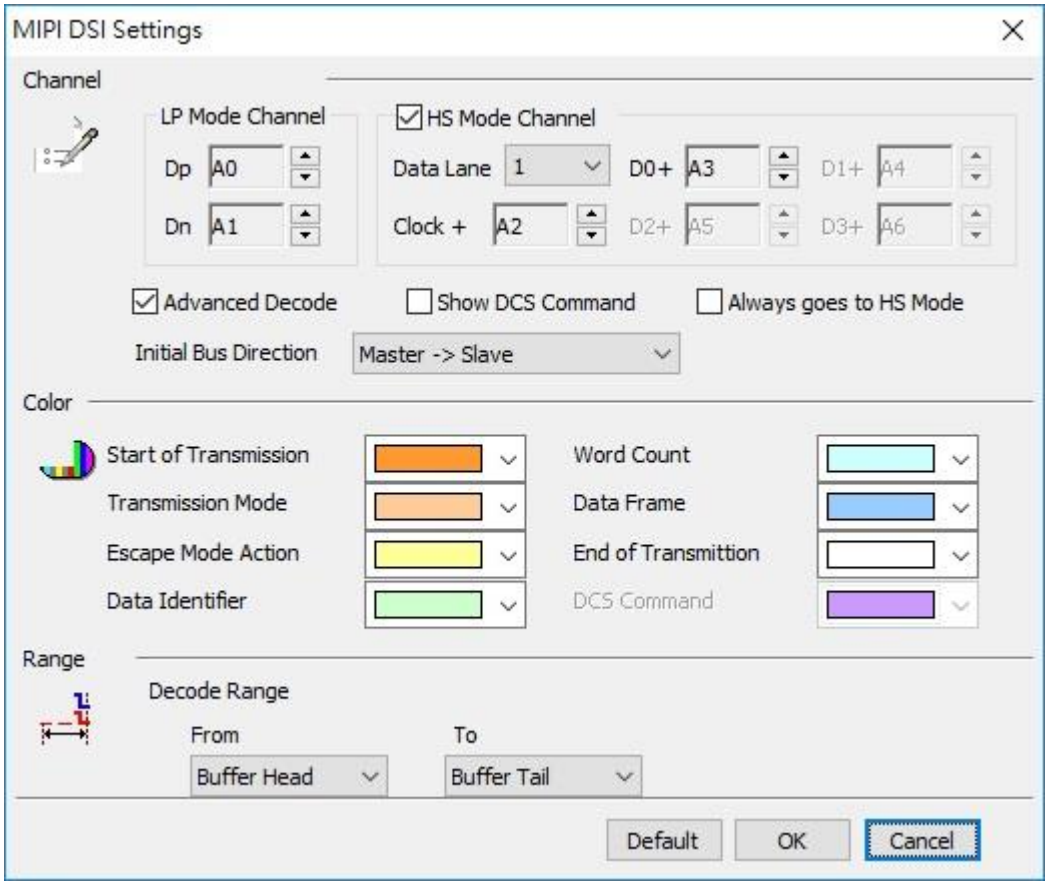


Sample	Command	Address	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)
701.6314000...	Write	0C1	E6								.
705.2044000...	Write	0C2	02								.
708.7775000...	Write	0C3	32								2
712.3505000...	Write	0C4	D7								.
715.9236000...	Write	0C5	5D								]
719.4966000...	Write	0C6	5E								^
723.0697000...	Write	0C7	0B								.

MIPI DSI

MIPI Display Serial Interface (DSI) designed by MIPI alliance for the protocols between a host processor and peripheral devices using a D-PHY physical interface. The operation mode includes High Speed Mode and Low Power Mode (LPM).

Settings



Dp, Dn: DSI-LP signal lines

Data Lane: DSI-HS mode Data Lane number

Clock+, D0+, D1+, D2+, D3+: DSI-HS signal lines

Advanced Decode: Enable DSI format decode and display.

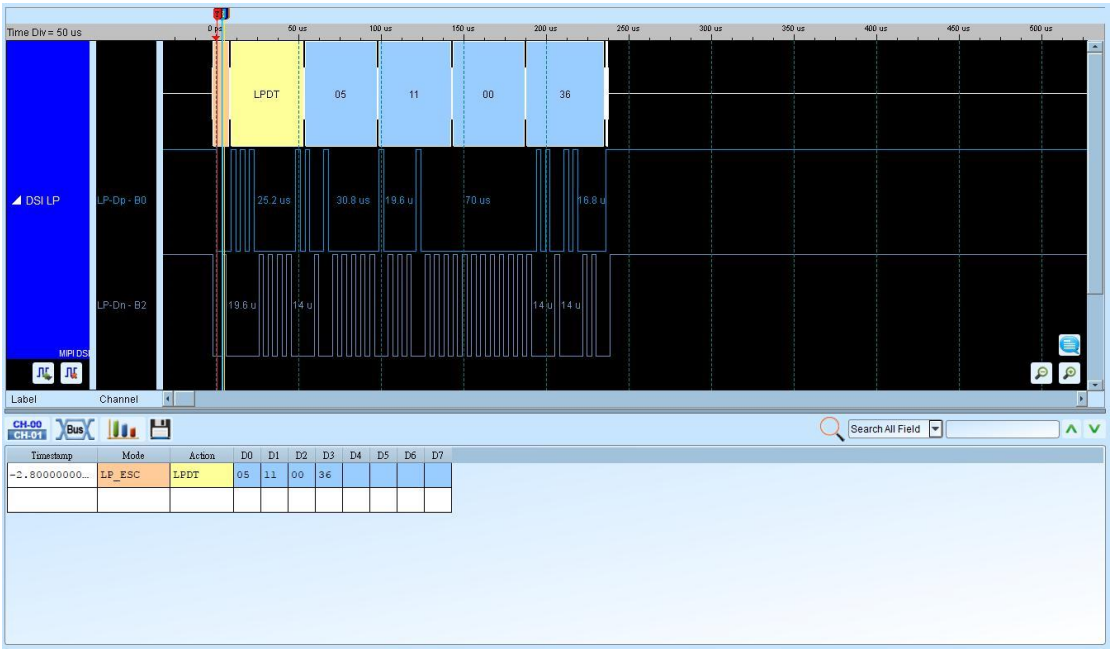
Show DCS Command: Enable DCS Command decode and display.

Always goes to HS Mode: Ignore the Dp and Dn status and decode all the data frame in HS mode

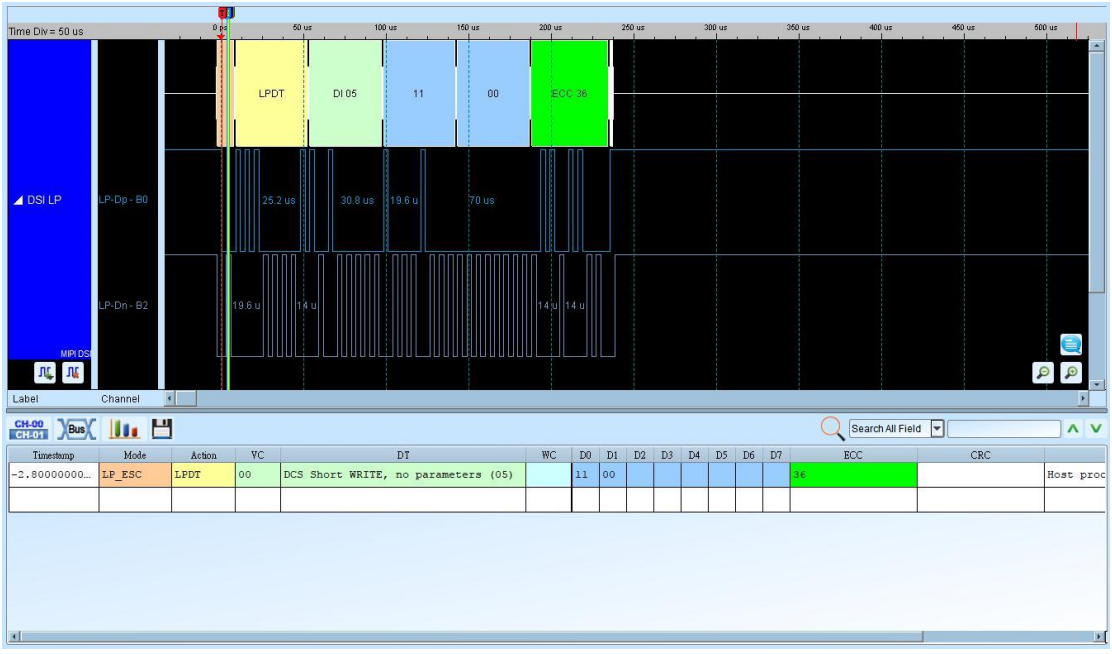
Initial Bus Direction: Select the Initial direction of the bus transmission.

Result

Advanced Decode Disabled:



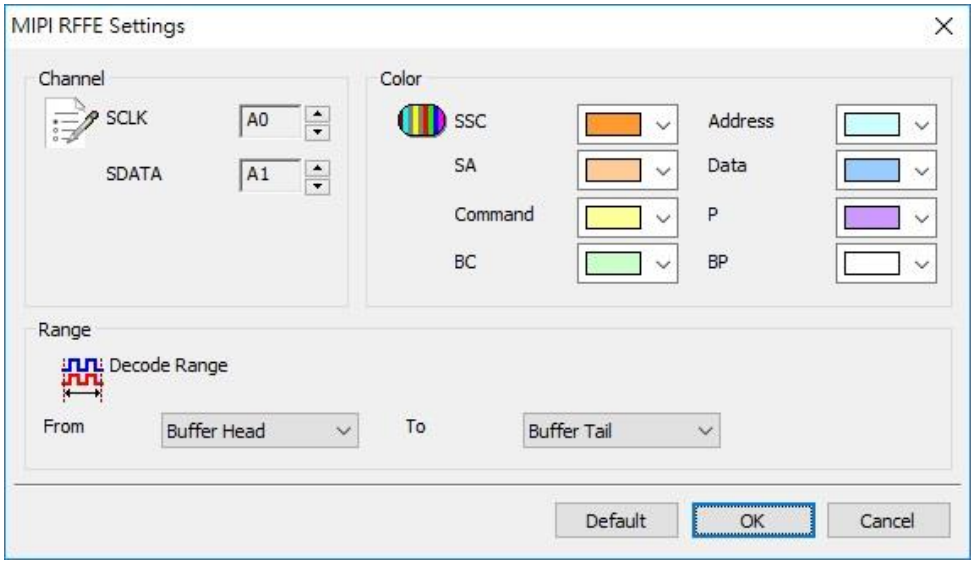
Advanced Decode Enabled:



MIPI RFFE

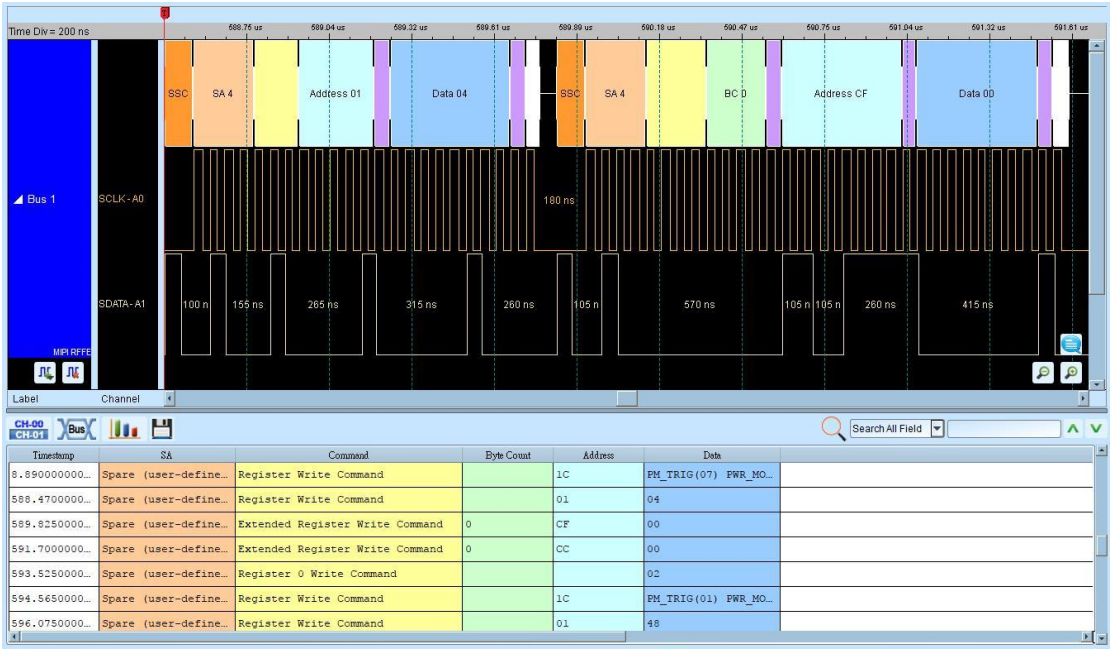
MIPI RFFE (RF Front-End Control Interface) designed by MIPI alliance is for controlling RF front-end devices including Power Amplifiers, Low-Noise Amplifiers, filters, switches, power management modules, antenna tuners and sensors.

Settings



Channel: Set the channels of SCLK and SDATA.

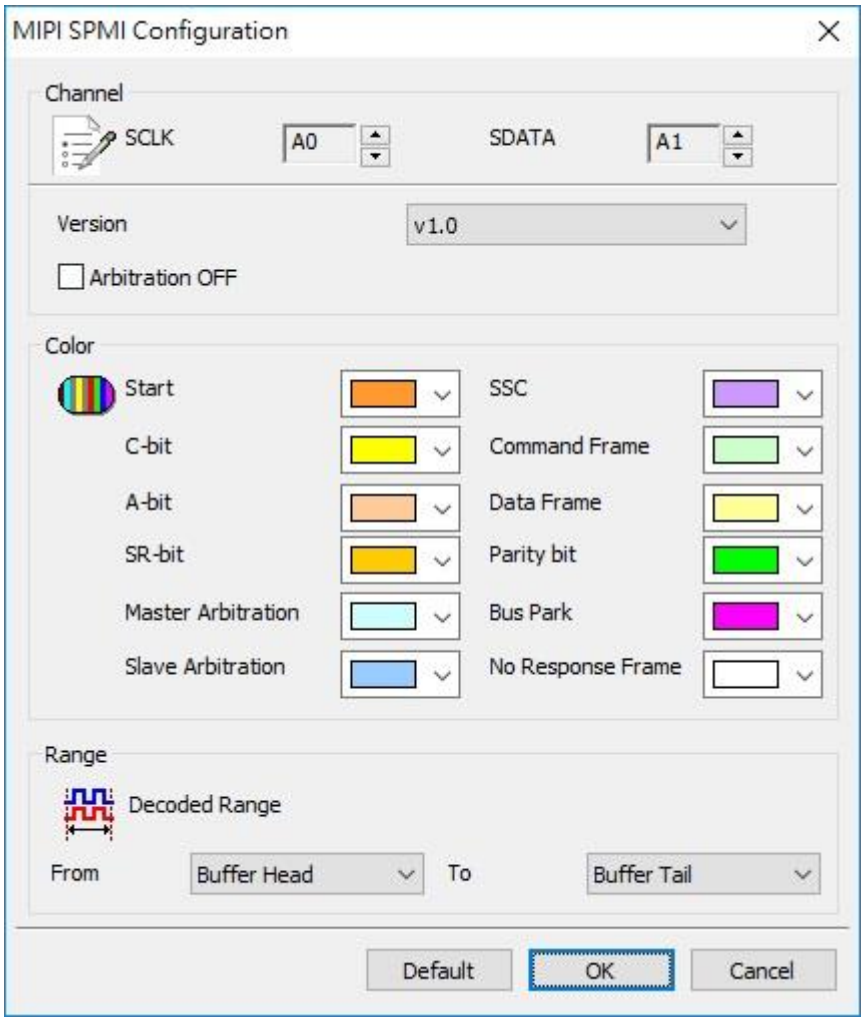
Result



MIPI SPMI

MIPI SPMI(System Power Management Interface) designed by MIPI alliance. SPMI is a serial interface that connects the integrated Power Controller(PC) with Power management Integrated Circuits(PMIC).

Settings

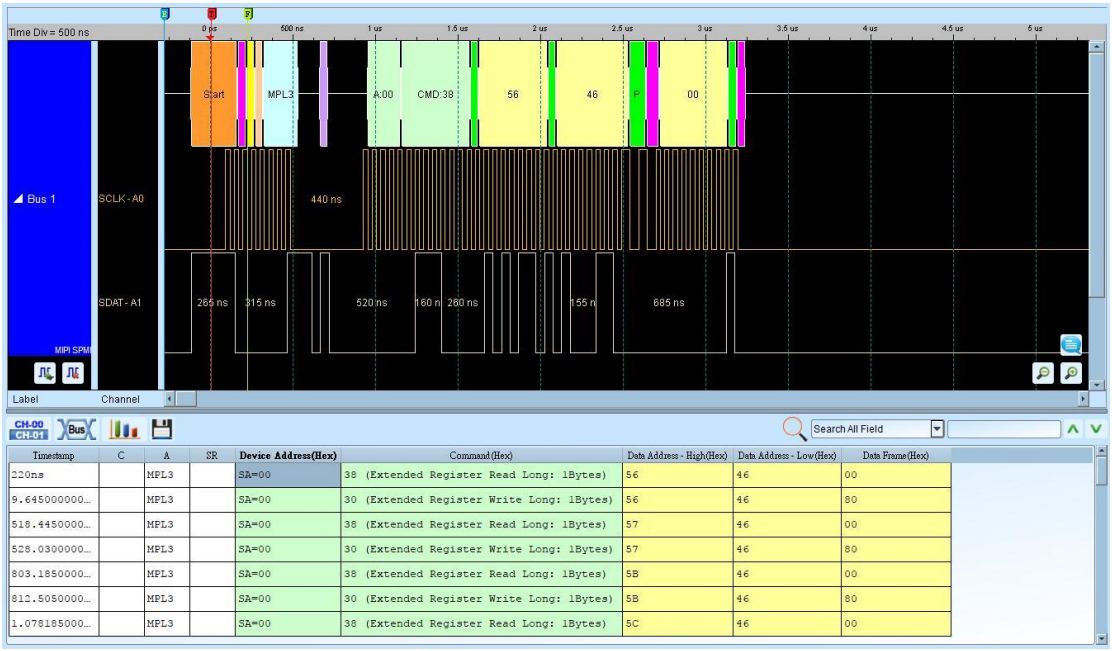


Channel: Set the channels of SCLK and SDATA.

Result

Click OK to run the MIPI SPMI Decode and see result on the Waveform Windows

below.

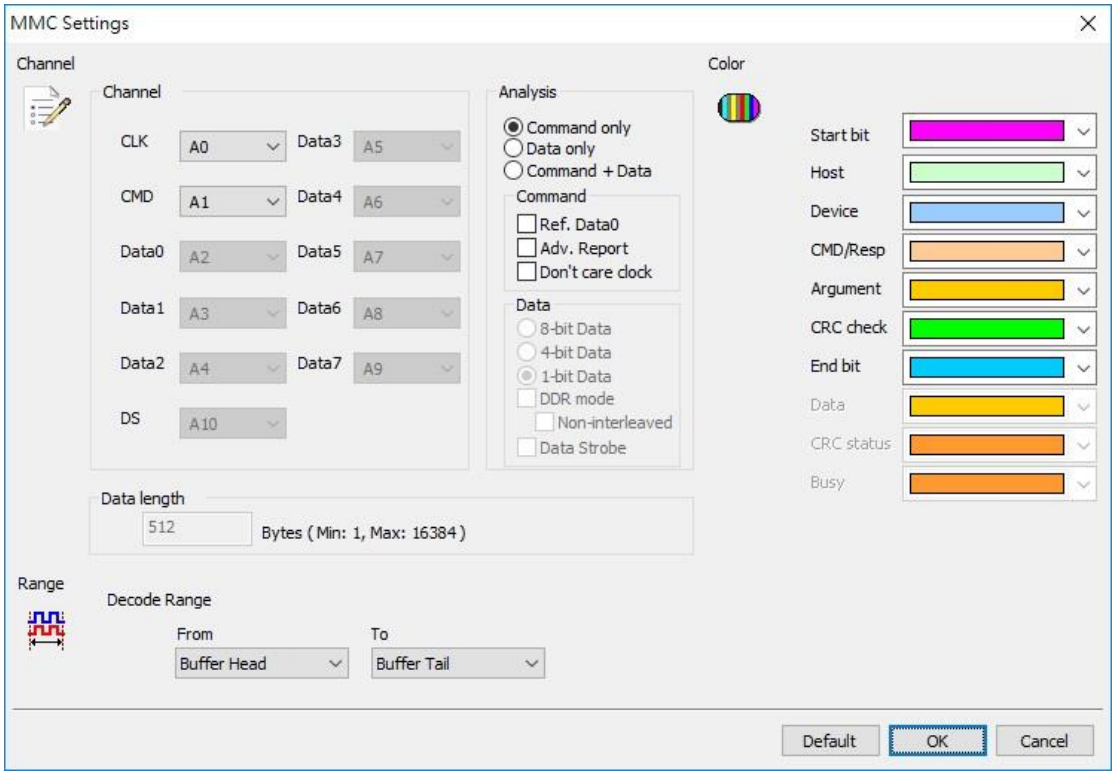


Timestamp	C	A	SR	Device Address(Hex)	Command (Hex)	Data Address - High(Hex)	Data Address - Low(Hex)	Data Frame(Hex)
220ns		MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	56	46	00
9.645000000…		MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	56	46	80
518.4450000…		MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	57	46	00
528.0300000…		MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	57	46	80
803.1850000…		MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	5B	46	00
812.5050000…		MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	5B	46	80
1.078185000…		MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	5C	46	00

MMC

The Multi Media Card (MMC) or the Embedded Multi Media Card (eMMC) version 5.1 is a flash memory card standard.

Settings



Channel: Show the selected channels.

Command only: Analyze the command.

Data only: Analyze the data

Command + Data: Analyze Command and Data in the report window.

Ref. DAT0: To help analyze the R1/R1b of the response.

Adv. Report: To analyze the command argument.

Don't care clock: To decode only depend on the CMD channel without the CLK channel.

Data: 1/4/8 bits or DDR mode, check “DDR mode” and ” “Non-interleaved” to analyze data without interleaved. Check “Data Strobe” to analyze data with the DQS channel.

Data length: Set the number of data bits.

Result

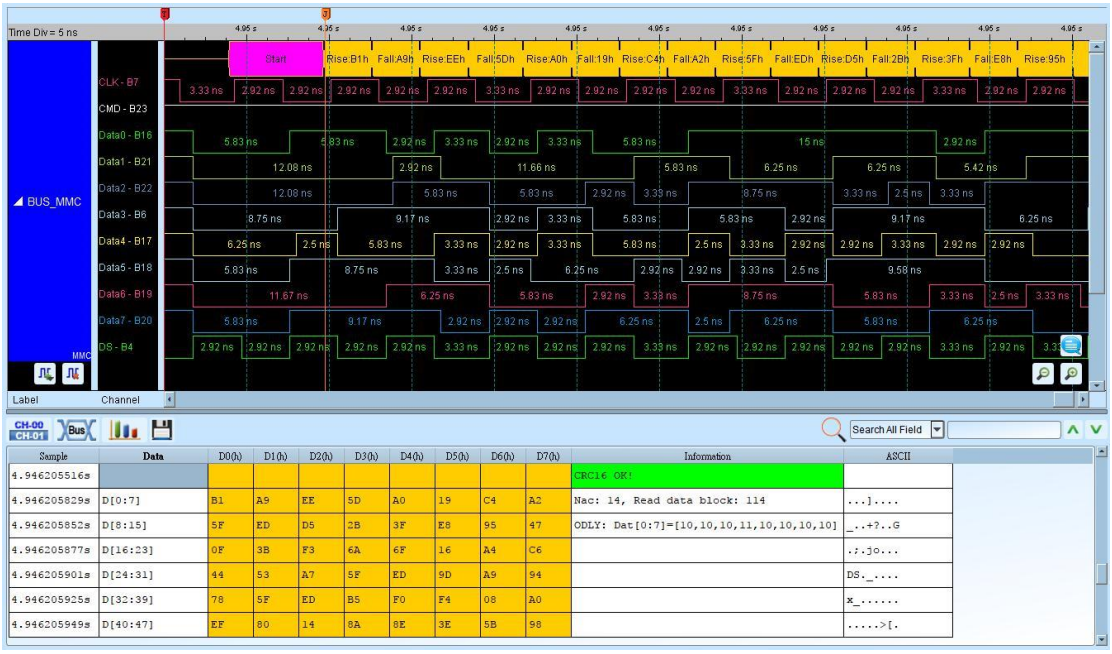
Command:

Sample	Command	Response	Argument (h)	CRC7 (h)	Frequency	Timing
4.960166510s		R1 :CMD18:READ_MULTIPLE_BLOCK	00 00 09 00	D3	166MHz	Ncr: 32
4.960743254s	CMD23:SET_BLOCK_COUNT		00 00 00 08	BF	166MHz	Nrc: 95979
4.960743738s		R1 :CMD23:SET_BLOCK_COUNT	00 00 09 00	1D	166MHz	Ncr: 32
4.960770843s	CMD18:READ_MULTIPLE_BLOCK		00 04 08 10	09	166MHz	Nrc: 4465
4.960771326s		R1 :CMD18:READ_MULTIPLE_BLOCK	00 00 09 00	D3	166MHz	Ncr: 32
4.961087460s	CMD23:SET_BLOCK_COUNT		00 00 00 18	8D	166MHz	Nrc: 52664
4.961087943s		R1 :CMD23:SET_BLOCK_COUNT	00 00 09 00	1D	166MHz	Ncr: 32

Adv. Report:

Timestamp	Command	Response	Argument (h)	CRC7 (h)	Frequency	Timing
106.7101046...	CMD09:SEND_CSD		00 01 00 00	F1	384KHz	Nrc: 74
106.7101046...			Bit[31:16] RCA: 0001h			
106.8553872...		R2 :Check bit(63)	D0 0F 00 32 0F AD A7 81 85 11 95 4D 49 5B ...	03	384KHz	Ncr: 8
106.8553872...			[127:126] CSD_STRUCTURE: Version is coded ...			
106.8553872...			[125:122] SPEC_VERS: Version 4.1 4.2 4.3			
106.8553872...			[119:112] TAAC: 10.0ms			
106.8553872...			[111:104] NSAC: 0Clk cycle			

Data:

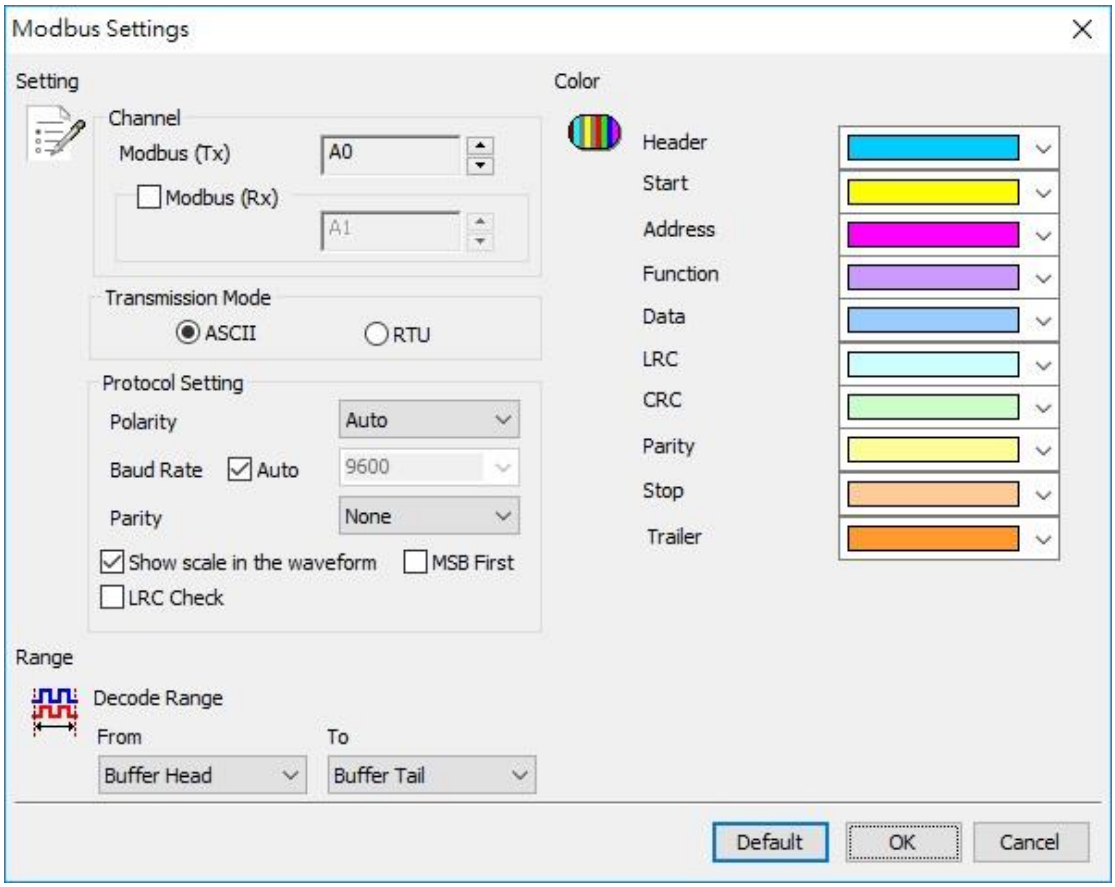


Sample	Data	D0(h)	D1(h)	D2(h)	D3(h)	D4(h)	D5(h)	D6(h)	D7(h)	Information	ASCII
4.946205516s										CRC16 OK!	
4.946205829s	D[0:7]	B1	A9	EE	5D	A0	19	C4	A2	Nac: 14, Read data block: 114	...]....
4.946205852s	D[8:15]	5F	ED	D5	2B	3F	E8	95	47	ODLY: Dat[0:7]=[10,10,10,11,10,10,10,10]	_..+?..G
4.946205877s	D[16:23]	0F	3B	F3	6A	6F	16	A4	C6		.;.jo...
4.946205901s	D[24:31]	44	53	A7	5F	ED	9D	A9	94		DS._....
4.946205925s	D[32:39]	78	5F	ED	B5	F0	F4	08	A0		x_......
4.946205949s	D[40:47]	EF	80	14	8A	8E	3E	5B	98		.....>[.

ModBus

Modbus is a serial communications protocol published by Modicon in 1979 for use with its programmable logic controllers (PLCs). Simple and robust, it has since become one of the standard communications protocols in the industry, and it is now amongst the most commonly available means of connecting industrial electronic devices.

Settings



Channel: Modbus (Tx) or Modbus (Rx).

Transmission Mode: ASCII and RTU mode.

Auto: Auto detection idle polarity.

Idle high: Idle condition shows High.

Idle low: Idle condition shows Low.

Auto Detect: Set the Baud Rate manually if not selected.

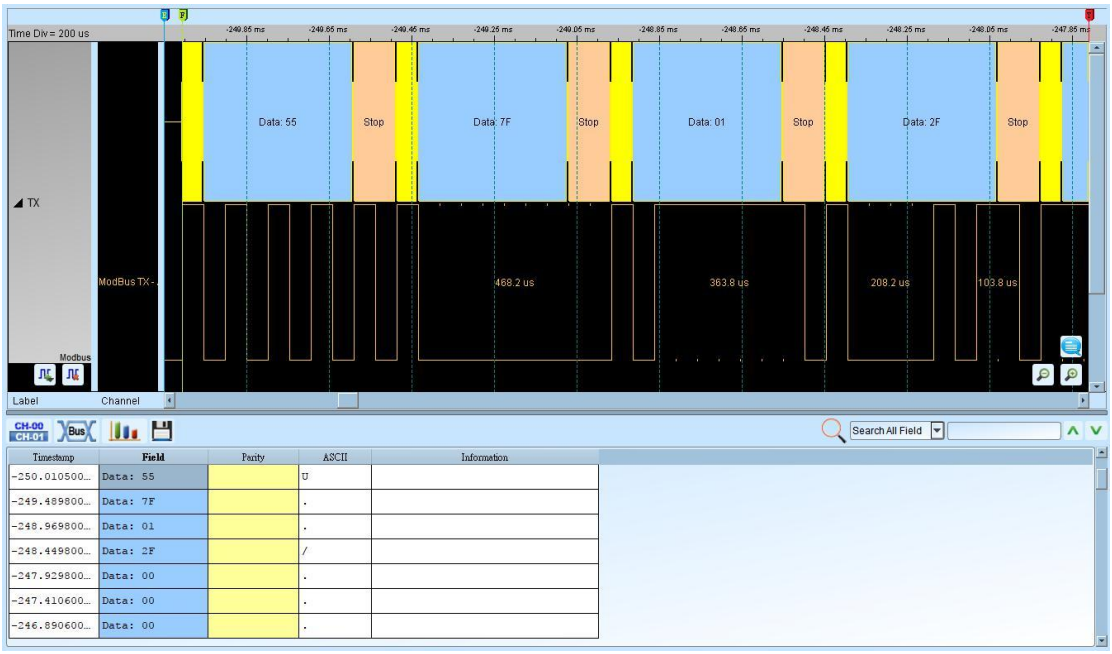
Baud Rate: Data rate (bits per second), and the range is 110 ~ 2M (bps).

Parity: N-None Parity, O-Odd Parity, E-Even Parity.

MSB First: The default is LSB first; click it to change to MSB first.

Show scale in the waveform: Display the waveforms with scales.

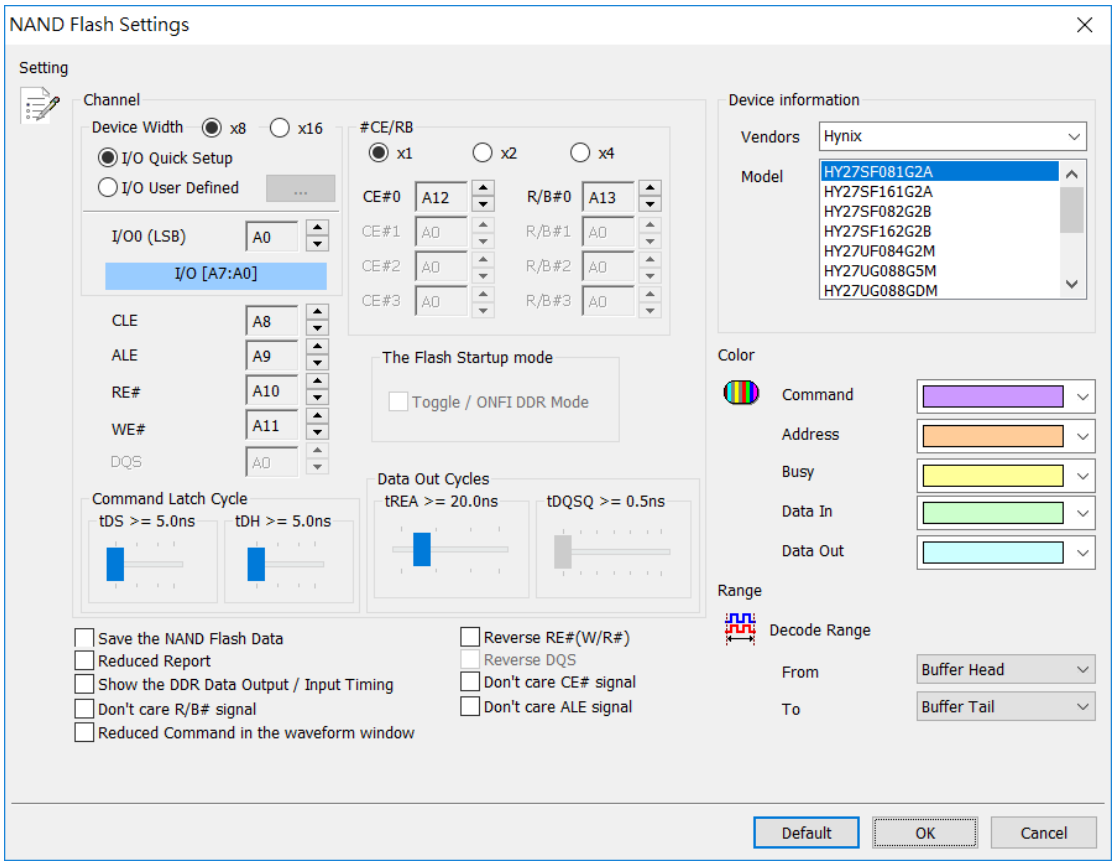
Result



NAND Flash

NAND flash uses tunnel injection for writing and tunnel release for erasing. NAND flash memory forms the core of the removable USB storage devices known as USB flash drives, as well as most memory card formats and solid-state drives available today.

Settings



Channel:

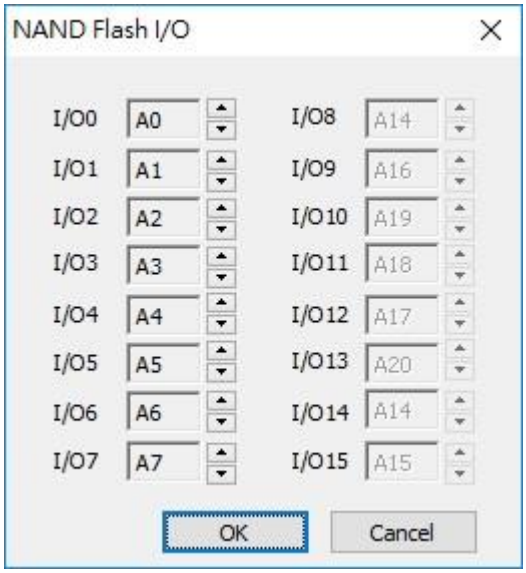
Async	Ssync	Description
I/Ox	DQx	NAND Flash data channels
CLE	CLE	Command Latch Enable channel
ALE	ALE	Address Latch Enable channel
RE	W/R	Read Enable and Write/Read channel

WE	CLK	Write Enable and Clock channel
RB#	RB#	Ready/Busy channel
CE#	CE#	Chip Enable channel
---	DQS	Data Strobe channel

Device Width: Select 8/16 bits device width.

The Flash Startup mode: Check Toggle /ONFI DDR Mode to run synchronous data interface.

I/O Quick Setup / I/O User Defined: Only set I/O0 (LSB) when select the I/O Quick Setup, other channels will be set automatically. when check the I/O User Defined and press the button will show the dialog below:



User can set NAND I/O channel by channel.

The Flash Startup mode: Check Toggle /ONFI DDR Mode to run synchronous data interface.

tREA / tDQSQ: Set the delay time to access the NAND data under SDR / DDR.

To adjust the tREA/tDQSQ when the data out value of NAND Flash is invalid.

Save the NAND Flash Data: Save the read/write data. Program will save the NAND Flash read/write data as a file when check Save the NAND Flash Data. It will be saved into the LA work directory.

mode.

Reduced Report: Only show NAND Flash command in the Report window when check it.

Show the DDR Data Output/Input Timing: Only show timing information under DDR mode.

Reduced Command in the waveform window: Only show NAND Command value in the waveform window.

Reverse RE# (W/R#) / Reverse DQS: Check this when connect the RE / DQS# under DDR mode.

Don't care ALE/RB#/CE# signal: Ignore the signal selected when decode.

Description of file name as following:

File Name	Description
NF_DI/NF_DO	NAND Flash Data In / Data Out
_Rowxxxxxxh	Row Address
_Colxxxxh	Column Address
CEx	Active CEx
_1, _2, _3	File Order

Ex:NF_DI_Row017821h_Col0000h_CE1_1.bin

NF_DO_Row017821h_Col0000h_CE1_2.bin

NF_DO_Row_Col_CE1_3.bin

Compare the content of file with the one of report.

D0	D1	D2	D3	D4	D5	D6	D7
5A	A6	6F	36	B2	38	B8	B7
06	8A	B7	0B	B1	19	C8	21
7E	CE	58	EF	BD	18	47	7C
5E	DD	9A	E3	A5	E4	02	11
E9	2D	96	14	86	32	CE	F4
53	10	60	79	EA	B6	D6	CE
5A	22	53	A5	F1	9E	DB	58
8A	73	B3	B1	82	19	B9	46
92	25	76	EA	E4	CE	74	A7
1C	E5	20	3D	9F	74	BB	E5
55	54	68	4C	69	86	AC	0F

```
000000  5A A6 6F 36 B2 38 B8 B7  06 8A B7 0B B1 19 C8 21
000010  7E CE 58 EF BD 18 47 7C  5E DD 9A E3 A5 E4 02 11
000020  E9 2D 96 14 86 32 CE F4  53 10 60 79 EA B6 D6 CE
000030  5A 22 53 A5 F1 9E DB 58  8A 73 B3 B1 82 19 B9 46
000040  92 25 76 EA E4 CE 74 A7  1C E5 20 3D 9F 74 BB E5
000050  55 54 68 4C 69 86 AC 0F  F1 A2 47 FA 37 4B 04 0D
```

Device information

Vendors: Select the NAND Flash Vendor. Please refer to the following details when select the **Custom** item.

Model: Select the NAND Flash device type.

Custom: Users create a **AqNFCustom.txt** file into the LA work directory when select the **Custom** vendor item and edit NAND Flash Command set.

```
Manufacturer=Samsung
PartNo=K9XXXXXXXX
#CE/RB=1
X16=N
SyncMode=Y
Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30
Cmd=Read Status, Read Stat., , , , , Y, N, Y, 70
Cmd=Two-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000, N, Y, N, 80, 11, 81, 10
```

Manufacturer, PartNo, #CE/RB, X16, SyncMode, Cmd are keywords.

Keyword	Description
Manufacturer	NAND Flash Vendor.
PartNo	NAND Flash IC Model.
#CE/RB	Number of targets, only 1/2/4 acceptable.
X16	8/16 bits device width, only Y/N acceptable.
SyncMode	Only Y/N acceptable, Y: Synchronous data interface supported; N:

	Not supported.
Cmd	Cmd is composed of several parts, it's divided with comma.
	1. Complete command name.
	2. Abbreviation of command.
	3. Name of first busy time check. Put a space and add a comma if unused.
	4. Value of first busy time check. Its unit is micro seconds. Put a space and add a comma if unused.
	5. Name of second busy time check. Put a space and add a comma if unused.
	6. Value of second busy time check. Its unit is micro mseconds. Put a space and add a comma if unused.
	7. First flag. It's acceptable command during busy.
	8. Second flag. It can be inserted by some command or not.
	9. Third flag. It can insert into some multi plane command or not.
	10. Command.

Ex: Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30

Cmd=Read Status, Read Stat., , , , , Y, N, Y ,70

Cmd=Two-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000,

N, Y, N, 80, 11, 81, 10

Read Status / Two-Plane Page Program : complete command.

Read Stat. / TPP Prog. : abbreviation of command.

Busy Time Check(tDBSY, 1, tPROG, 5000) : tDBSY is 1us; tPROG is

5000 us. It will show some information when violation of busy time.

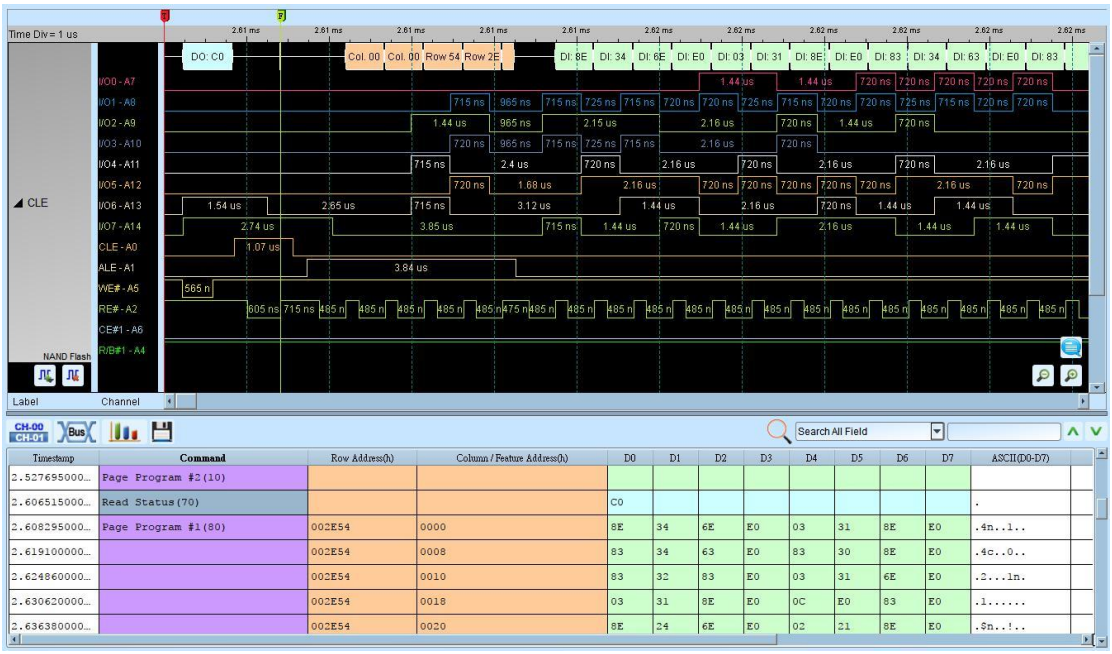
3 Flags: 1st flag of "Read Status" is Y means it's acceptable command

During busy; 2nd flag of "Two-Plane Page Program" and 3rd flag of "Read

Status" means any command between 11h and 81h is prohibited except

"Read Status (70h)".

Result

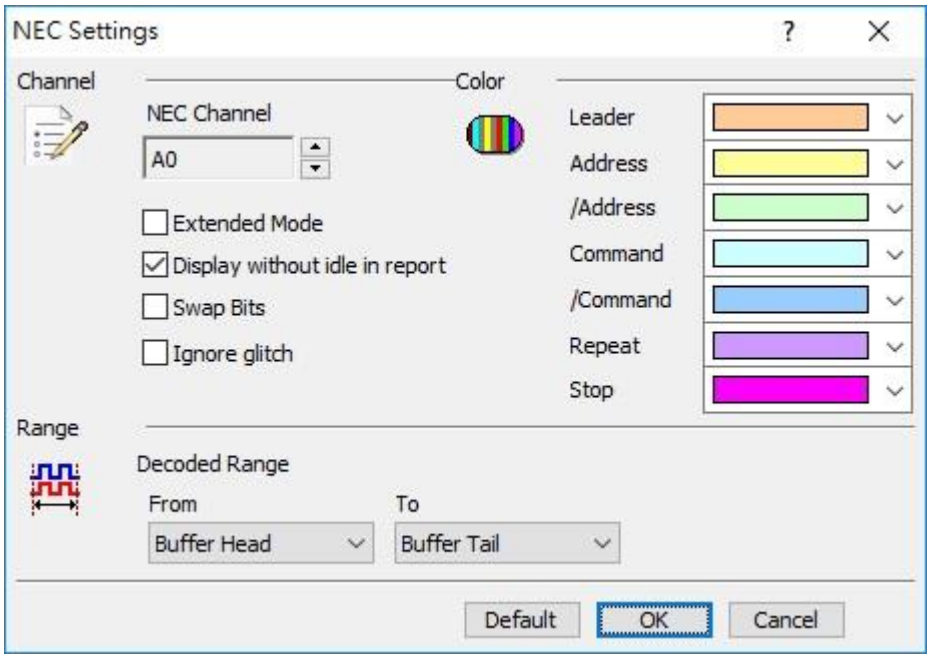


Timestamp	Command	Row Address(h)	Column / Feature Address(h)	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)
2.527695000...	Page Program #2(10)											
2.606515000...	Read Status(70)			C0								.
2.608295000...	Page Program #1(80)	002E54	0000	8E	34	6E	E0	03	31	8E	E0	.4n..1..
2.619100000...		002E54	0008	83	34	63	E0	83	30	8E	E0	.4c..0..
2.624860000...		002E54	0010	83	32	83	E0	03	31	6E	E0	.2...1n.
2.630620000...		002E54	0018	03	31	8E	E0	0C	E0	83	E0	.1......
2.636380000...		002E54	0020	8E	24	6E	E0	02	21	8E	E0	.$n..!..

NEC IR

It needs only one channel to analysis NEC signals.

Settings



Channel: Display the channel (CH 0).

Extended Mode: It integrates /Address and Address into 16 Bits Address, /Command and Command into 16 Bits Command.

Display without idle in report: It will not idle on the Report Window for the user to observe and analyze data.

Swap Bits: Switch LSB First to MSB First.

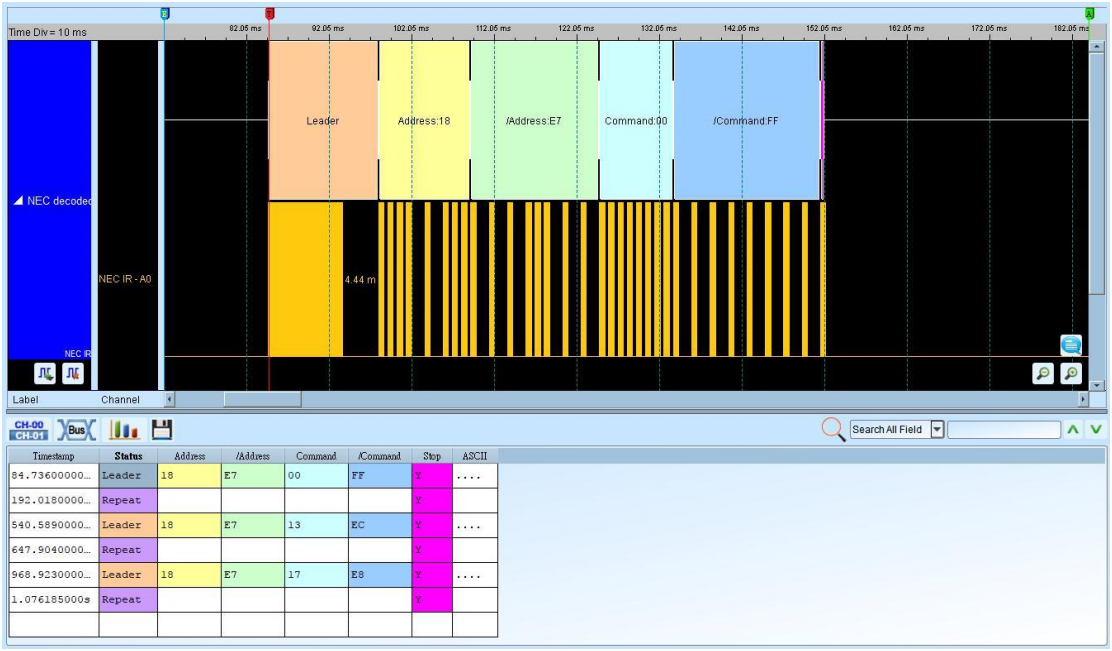
Auto: Shows High or Low when auto detection Idle.

Idle high: Idle condition shows High.

Idle low: Idle condition shows Low.

Result

Click **OK** to run the NEC IR decode and see the result on the Waveform Window below.

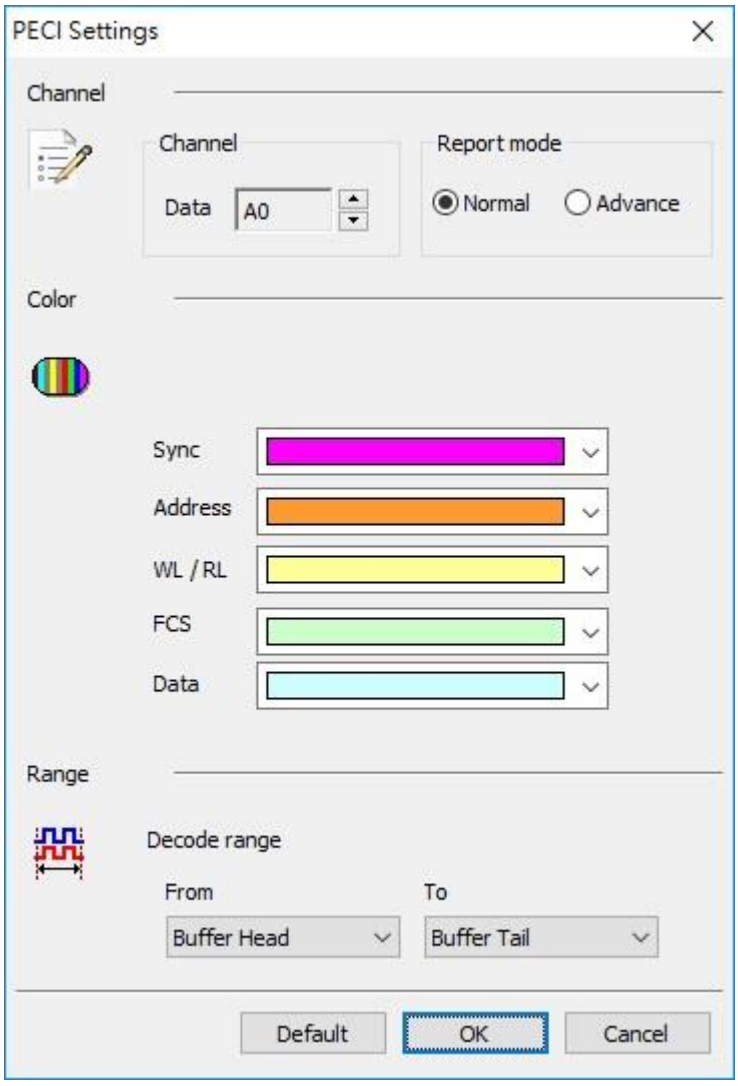


Timestamp	Status	Address	/Address	Command	/Command	Stop	ASCII
84.73600000...	Leader	18	E7	00	FF	Y	....
192.0180000...	Repeat					Y	
540.5890000...	Leader	18	E7	13	EC	Y	....
647.9040000...	Repeat					Y	
968.9230000...	Leader	18	E7	17	E8	Y	....
1.076185000s	Repeat					Y	

PECI

Platform Environment Control Interface, Platform management include thermal, power and electrical error monitoring.

Settings

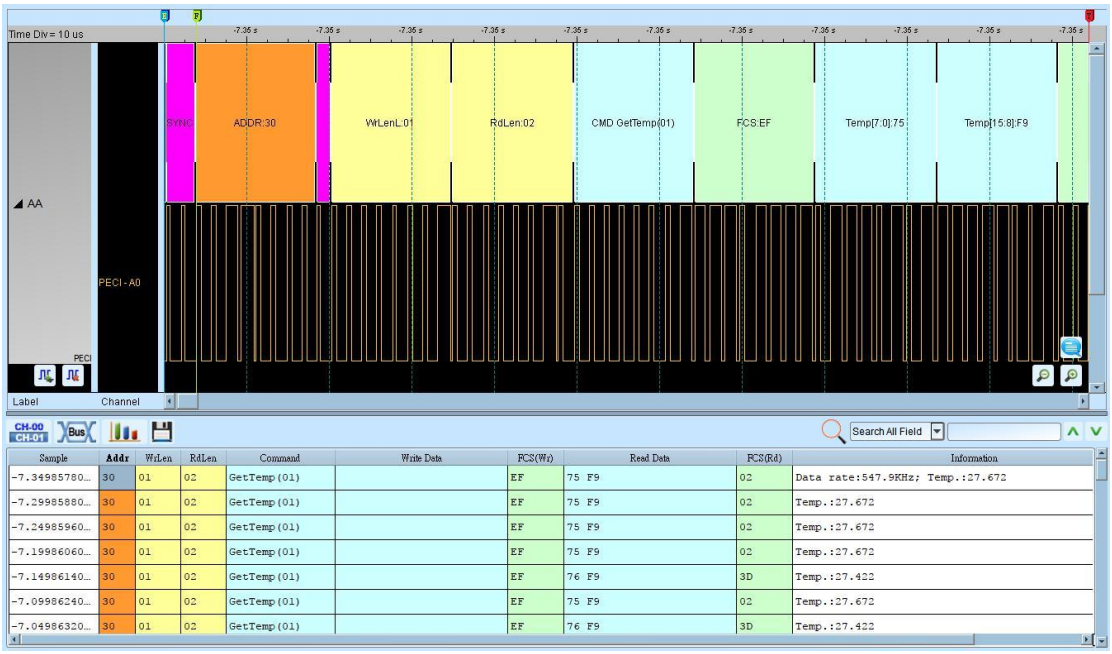


Channel: Show the selected channels.

Report mode: Normal or Advance

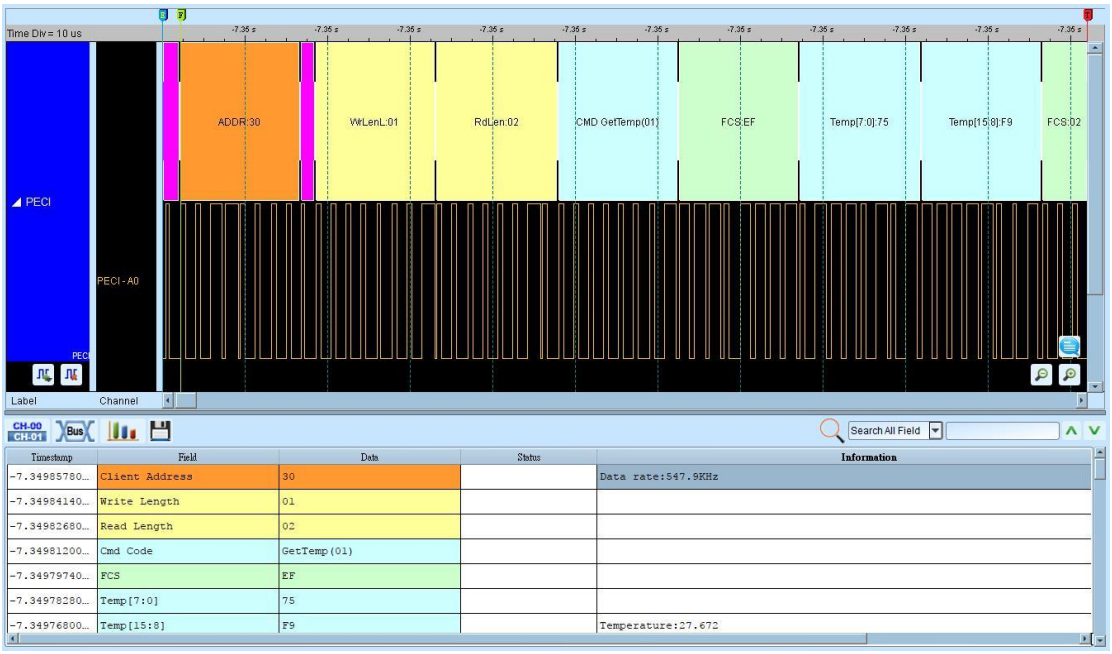
Result

Normal mode



Sample	Addr	WrLen	RdLen	Command	Write Data	FCS(Wr)	Read Data	FCS(Rd)	Information
-7.34985780...	30	01	02	GetTemp(01)		EF	75 F9	02	Data rate:547.9KHz; Temp.:27.672
-7.29985880...	30	01	02	GetTemp(01)		EF	75 F9	02	Temp.:27.672
-7.24985960...	30	01	02	GetTemp(01)		EF	75 F9	02	Temp.:27.672
-7.19986060...	30	01	02	GetTemp(01)		EF	75 F9	02	Temp.:27.672
-7.14986140...	30	01	02	GetTemp(01)		EF	76 F9	3D	Temp.:27.422
-7.09986240...	30	01	02	GetTemp(01)		EF	75 F9	02	Temp.:27.672
-7.04986320...	30	01	02	GetTemp(01)		EF	76 F9	3D	Temp.:27.422

Advance mode

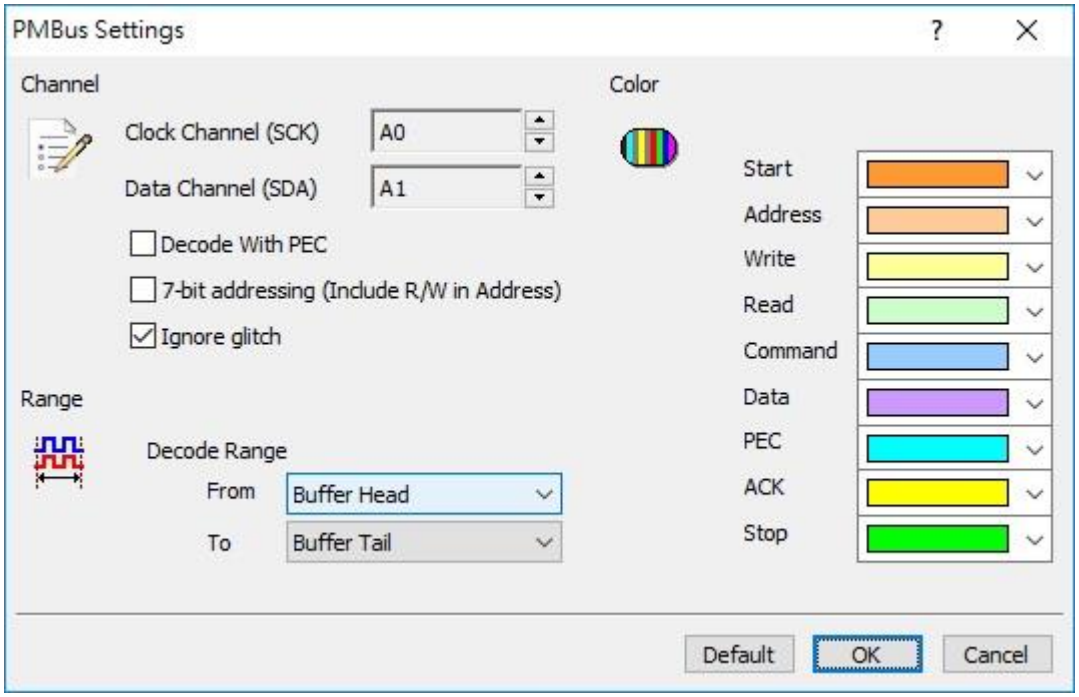


Timestamp	Field	Data	Status	Information
-7.34985780...	Client Address	30		Data rate:547.9KHz
-7.34984140...	Write Length	01		
-7.34982680...	Read Length	02		
-7.34981200...	Cmd Code	GetTemp(01)		
-7.34979740...	FCS	EF		
-7.34978280...	Temp[7:0]	75		
-7.34976800...	Temp[15:8]	F9		Temperature:27.672

PMBus

The Power Management Bus (“PMBus”) is an open standard protocol that defines a means of communicating with power conversion and other devices.

Settings



Channel: Show the selected channels.

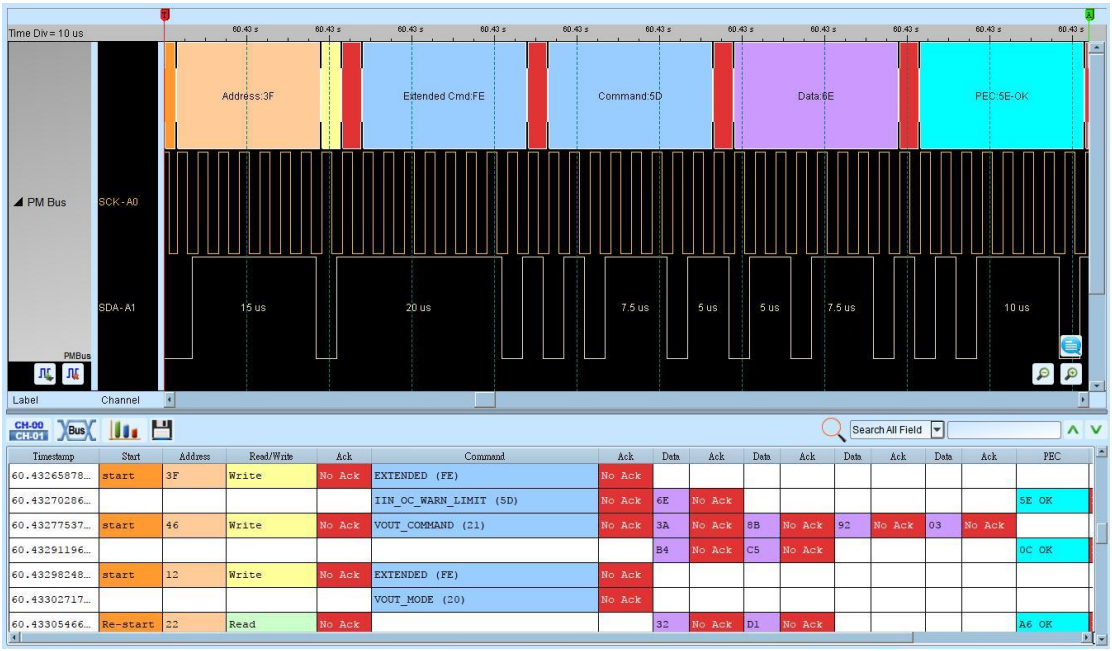
Decode With PEC: Group command protocol with PEC.

7-bit addressing (Include R/W in address): Show 8-bit addressing (include 7-bit addressing and 1-bit R/W).

Ignore glitch: Ignore the glitch when the slow transitions.

Result

Click **OK** to run the PMBus decode and see the result on the Waveform Window below.

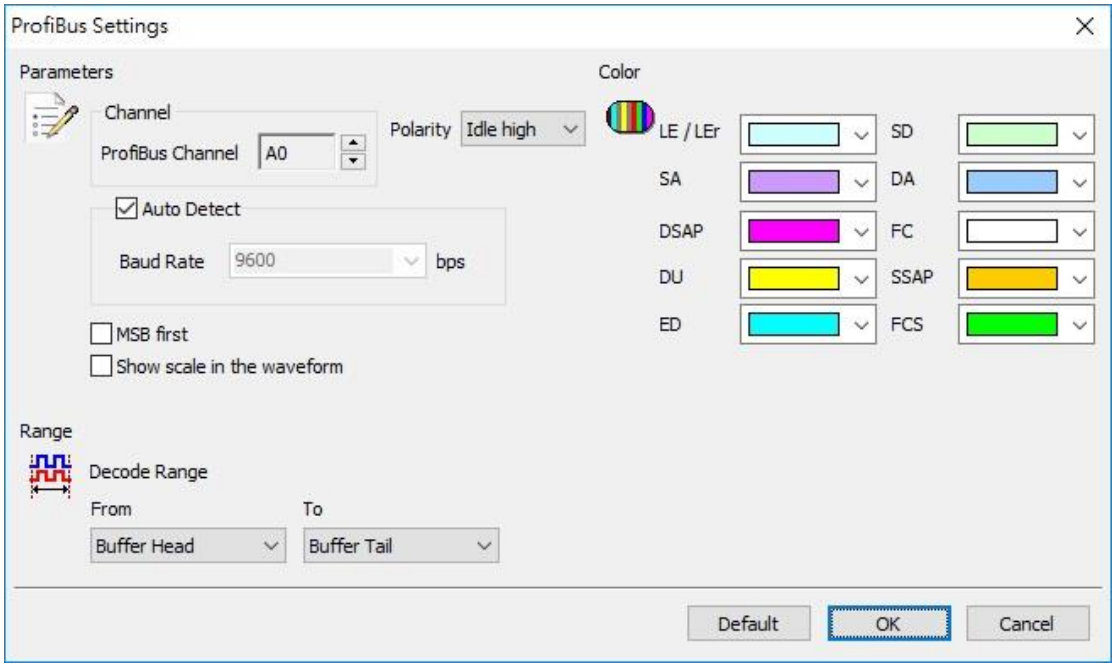


Timestamp	Start	Address	Read/Write	Ack	Command	Ack	Data	Ack	Data	Ack	Data	Ack	Data	Ack	PEC
60.43265878...	start	3F	Write	No Ack	EXTENDED (FE)	No Ack									
60.43270286...					IIN_OC_WARN_LIMIT (5D)	No Ack	6E	No Ack							5E OK
60.43277537...	start	46	Write	No Ack	VOUT_COMMAND (21)	No Ack	3A	No Ack	8B	No Ack	92	No Ack	03	No Ack	
60.43291196...							B4	No Ack	C5	No Ack					0C OK
60.43298248...	start	12	Write	No Ack	EXTENDED (FE)	No Ack									
60.43302717...					VOUT_MODE (20)	No Ack									
60.43305466...	Re-start	22	Read	No Ack			32	No Ack	D1	No Ack					A6 OK

ProfiBus

ProfiBus (PROcess Field Bus) is implemented by RS485. It includes PROFIBUS DP, PROFIBUS PA and PROFIBUS FMS.

Settings



Channel: Set the ProfiBus Channel

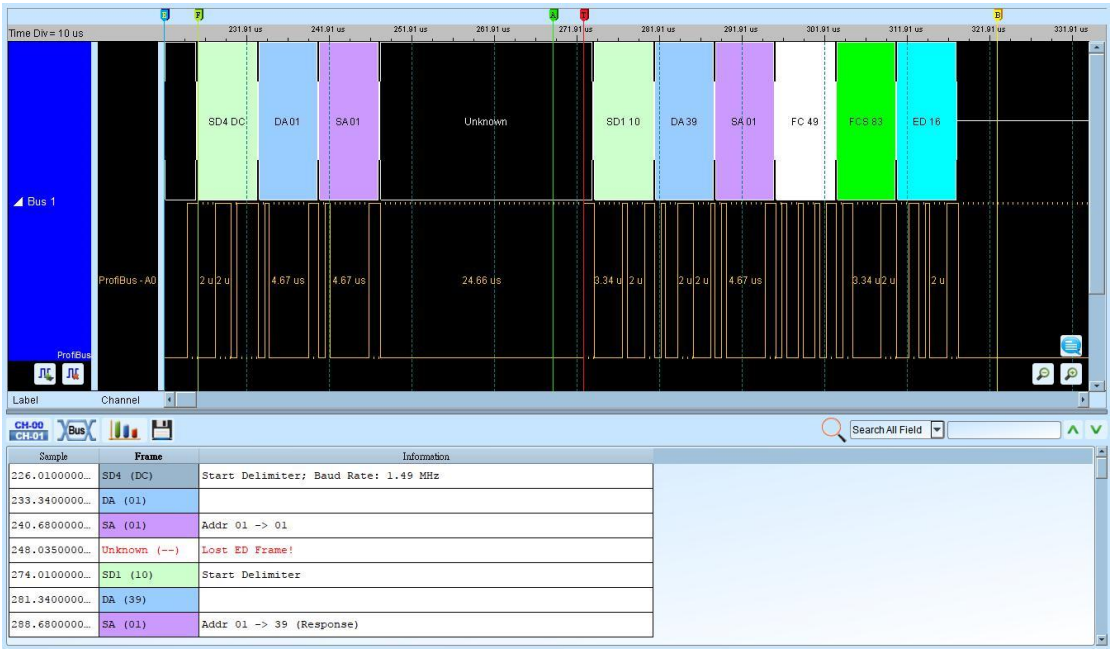
Polarity: Set the polarity Idle high / Idle low

Baud Rate/Auto Detect: Set the baud rate manually or auto detect

MSB First: The default is LSB first; click it to change to MSB first.

Show scale in the waveform: Show the scale in the waveform section

Result

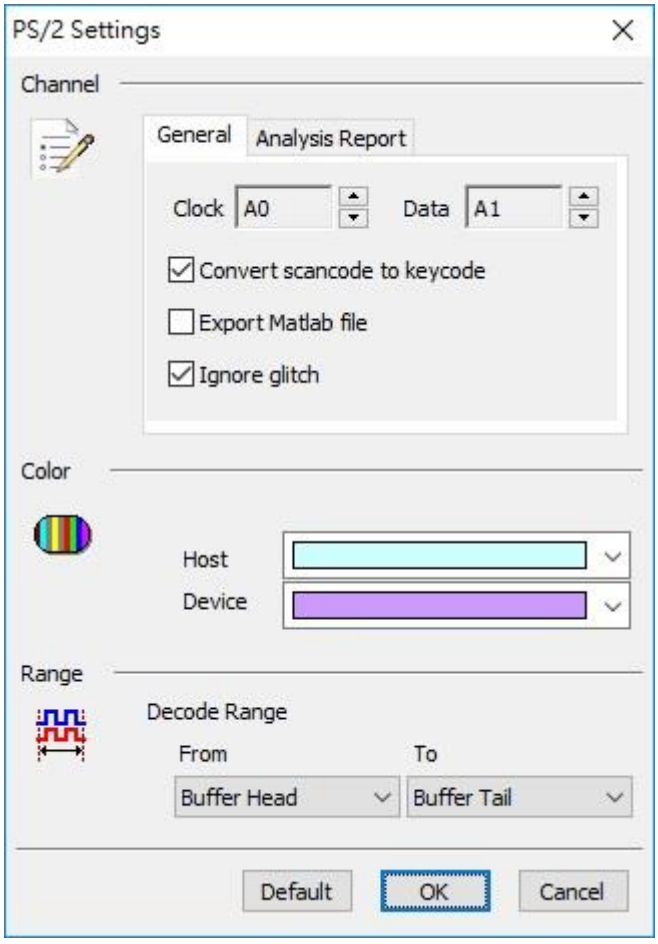


Sample	Frame	Information
226.0100000…	SD4 (DC)	Start Delimiter; Baud Rate: 1.49 MHz
233.3400000…	DA (01)	
240.6800000…	SA (01)	Addr 01 -> 01
248.0350000…	Unknown (--)	Lost ED Frame!
274.0100000…	SD1 (10)	Start Delimiter
281.3400000…	DA (39)	
288.6800000…	SA (01)	Addr 01 -> 39 (Response)

PS/2

The Personal System/2 (PS/2) protocol has 6 data bits, but only the first bit (Data) and the fifth bit (Clock) need to be analyzed.

PS/2 Settings



Channel: Show the selected channels.

Convert scan code to key code: Transform data into keyboard characters.

Export MATLAB file: Export the data with MATLAB format as the following:

Time = [25.78484 25.785985 …]

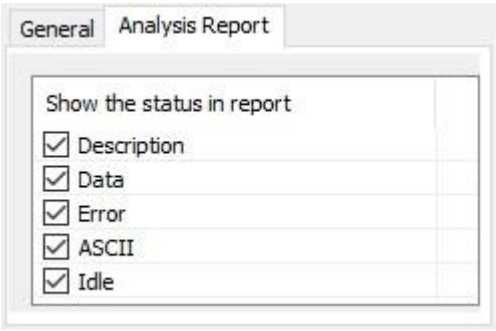
Description = [DH DH …] DH = Device to Host, HD = Host to Device

Data = [58 FA 02 FA C4 …]

The file (PS2_Matlab.m) will be saved at work directory

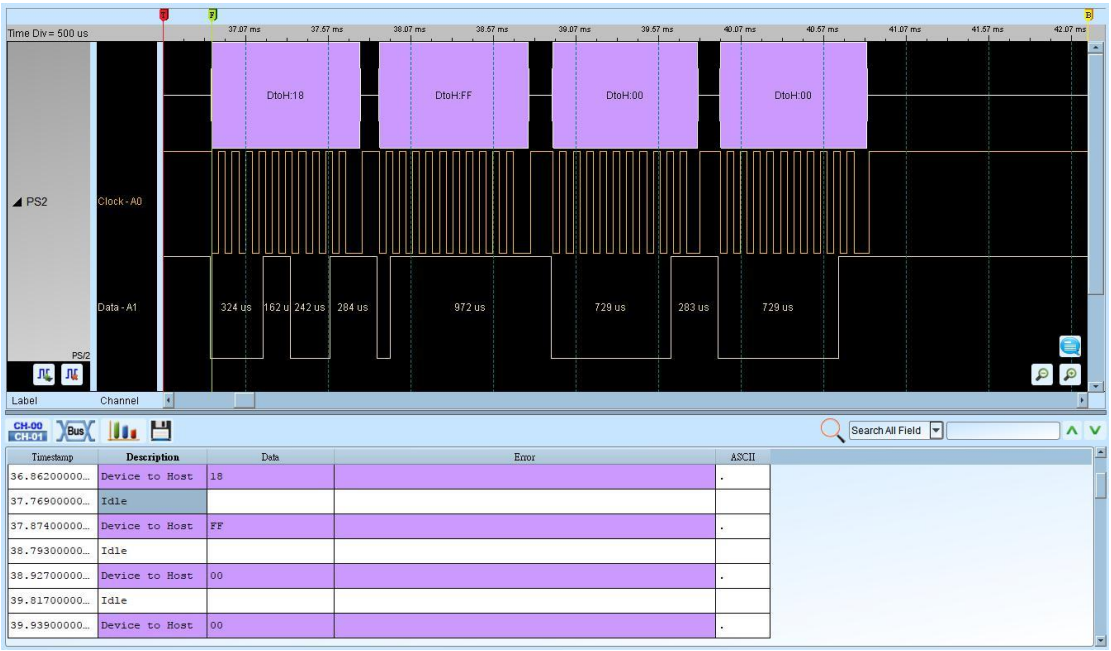
Ignore glitch: Ignore the glitch when the slow transitions.

Analysis Report: Show the selected status in report.



Result

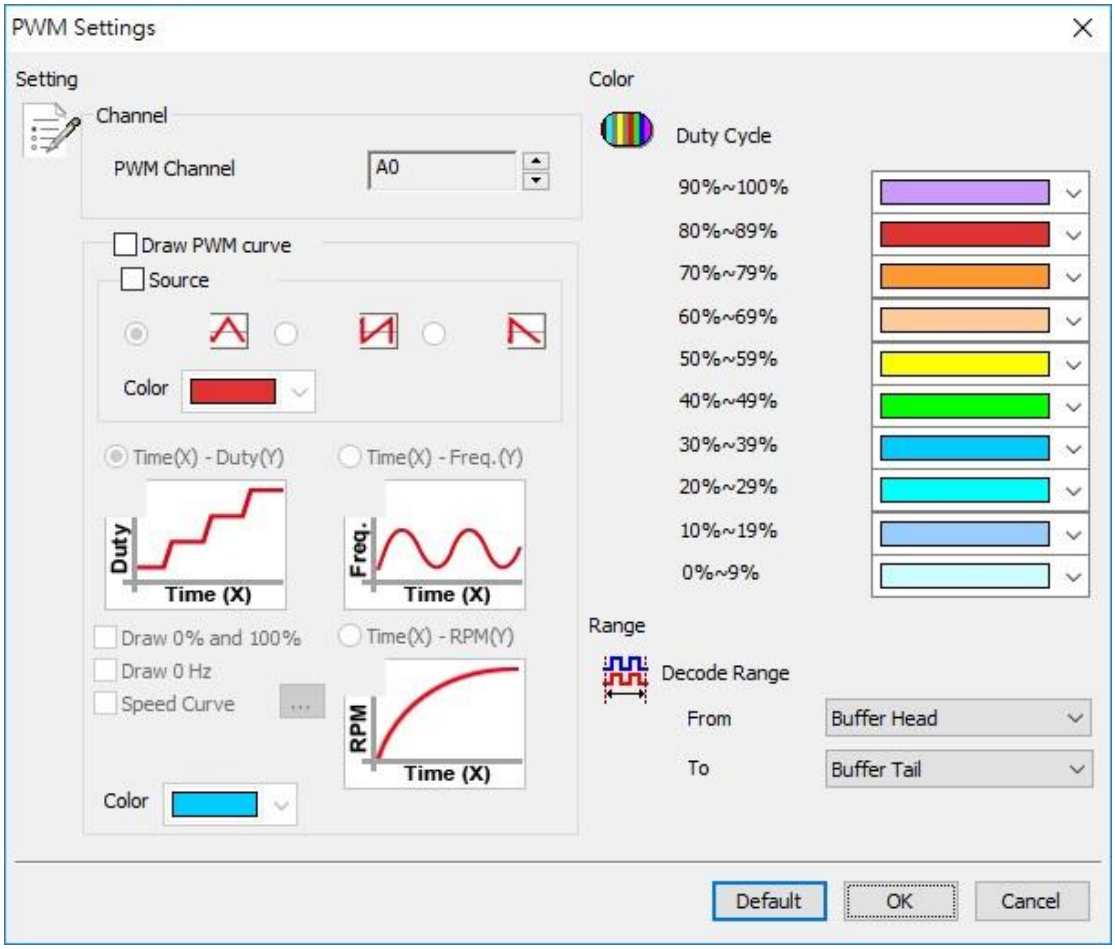
Click **OK** to run the PS/2 decode and see the result on the Waveform Window below.



PWM

Pulse-width modulation (PWM) is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches.

Settings



Channel: Show the selected channel.

Draw PWM curve:

Source: Show the source waveform of the PWM.

Time(X)-Duty(Y): Show the curve diagram with Time(X) and Duty(Y)

Time(X)-Freq.(Y): Show the curve diagram with Time(X) and Freq.(Y)

Time(X)-RPM(Y): Show the curve diagram with Time(X) and RPM(Y)

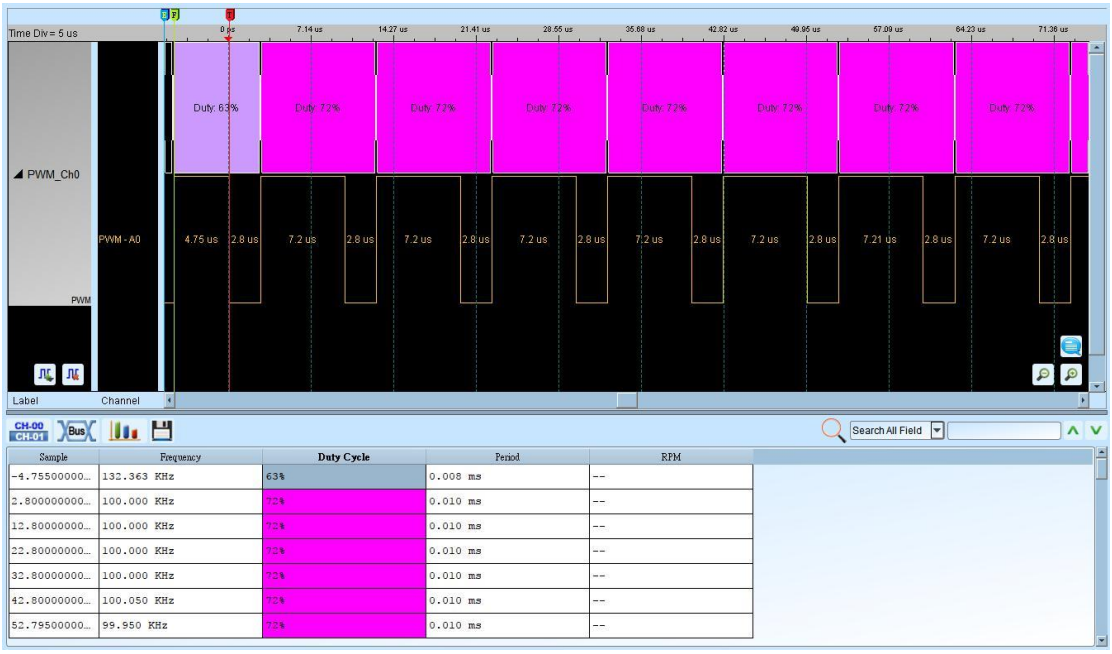
Draw 0% and 100%: When select the Time(X)-Duty(Y) drawing and check Draw 0% and 100%, the program will draw this duty curve of 0% or 100%; it will draw this duty curve of 0% or 100% when uncheck Draw 0% and 100%.

Draw 0 Hz: When select the Time(X)-Freq.(Y) drawing and check the item Draw 0 Hz, will show the Frequency from 0 Hz at Y axis.

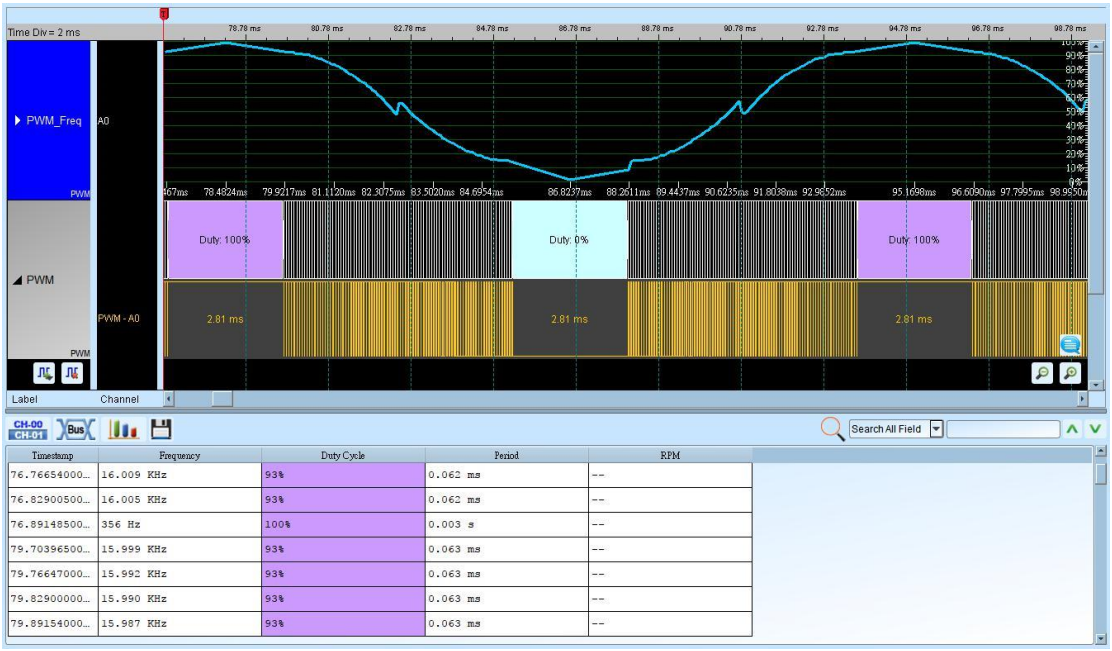
Result

Click **OK** to run the PWM decode and see the result on the Waveform Window below.

Select “Source”

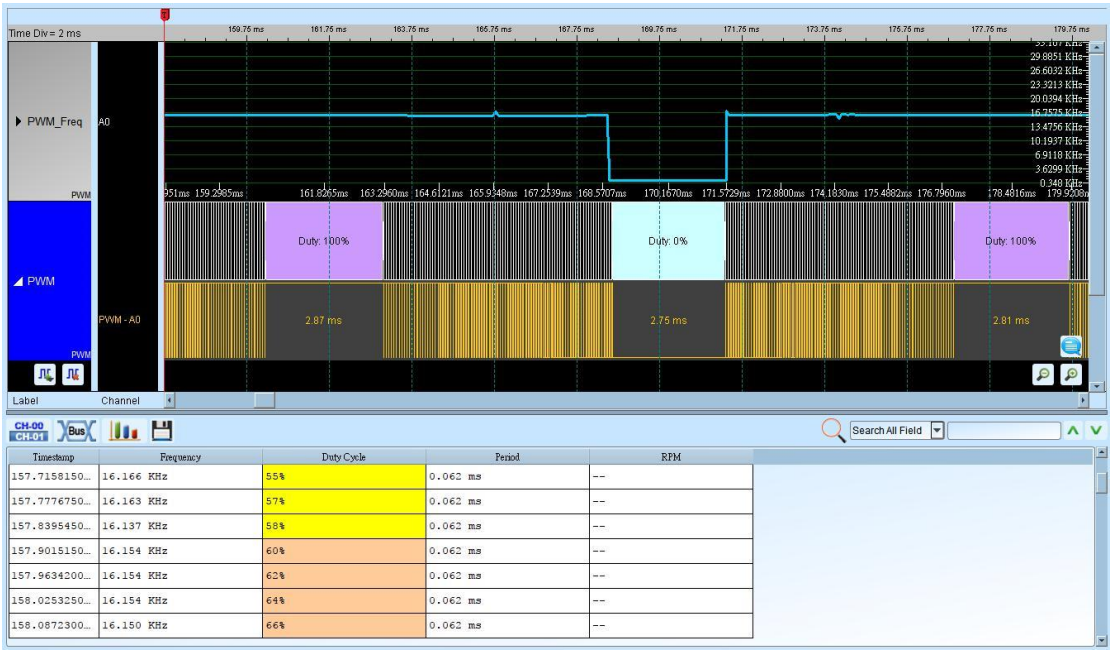


Select Time(X)-Duty(Y)



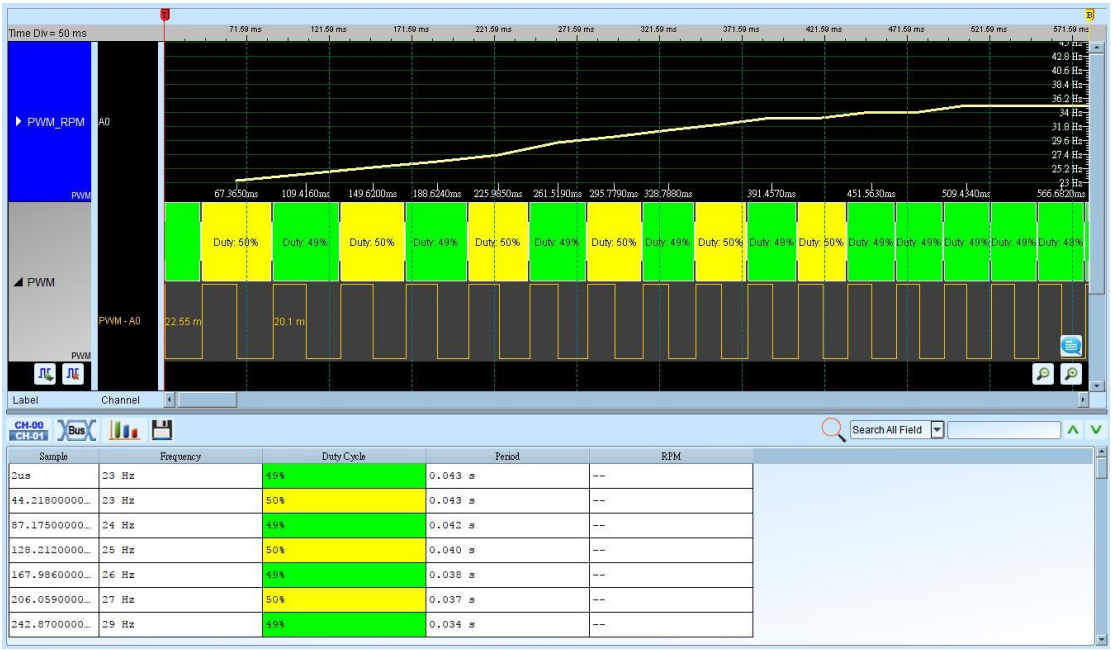
Timestamp	Frequency	Duty Cycle	Period	RPM
76.76654000...	16.009 KHz	93%	0.062 ms	--
76.82900500...	16.005 KHz	93%	0.062 ms	--
76.89148500...	356 Hz	100%	0.003 s	--
79.70396500...	15.999 KHz	93%	0.063 ms	--
79.76647000...	15.992 KHz	93%	0.063 ms	--
79.82900000...	15.990 KHz	93%	0.063 ms	--
79.89154000...	15.987 KHz	93%	0.063 ms	--

Select Time(X)-Freq.(Y)



Timestamp	Frequency	Duty Cycle	Period	RPM
157.7158150...	16.166 KHz	55%	0.062 ms	--
157.7776750...	16.163 KHz	57%	0.062 ms	--
157.8395450...	16.137 KHz	58%	0.062 ms	--
157.9015150...	16.154 KHz	60%	0.062 ms	--
157.9634200...	16.154 KHz	62%	0.062 ms	--
158.0253250...	16.154 KHz	64%	0.062 ms	--
158.0872300...	16.150 KHz	66%	0.062 ms	--

Select Time(X)-RPM(Y)

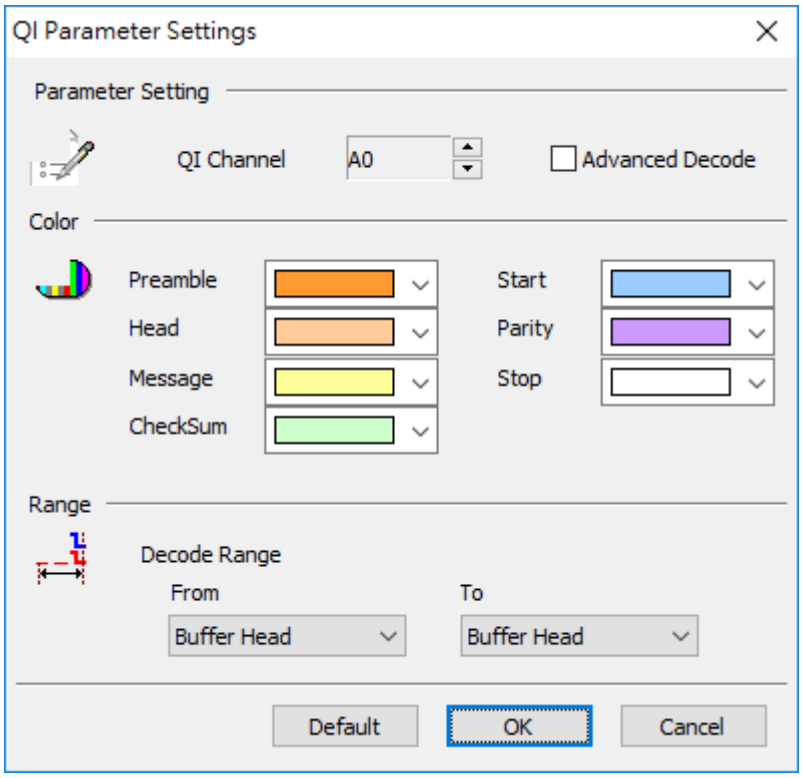


Sample	Frequency	Duty Cycle	Period	RPM
2us	23 Hz	49%	0.043 s	--
44.21800000...	23 Hz	50%	0.043 s	--
87.17500000...	24 Hz	49%	0.042 s	--
128.2120000...	25 Hz	50%	0.040 s	--
167.9860000...	26 Hz	49%	0.038 s	--
206.0590000...	27 Hz	50%	0.037 s	--
242.8700000...	29 Hz	49%	0.034 s	--

QI

QI is a contactless power transfer protocol published by Wireless Power Consortium (WPC). It is a method of contactless power transfer from a Base Station to a Mobile Device, which is based on near field magnetic induction between coils.

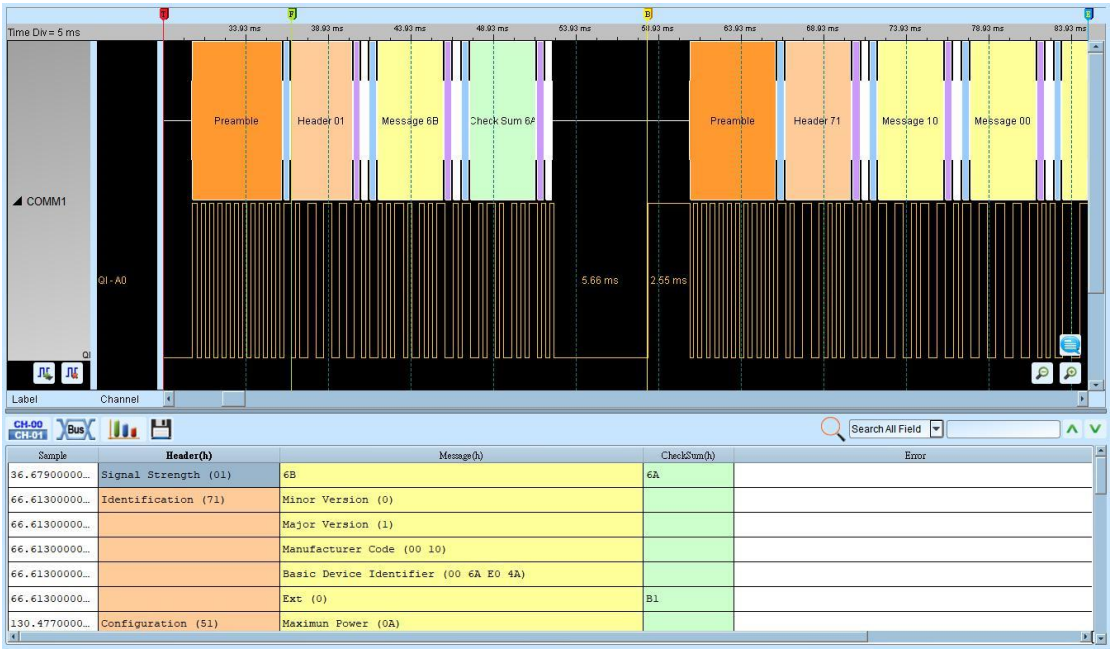
Settings



QI Channel: Show the selected channel.

Advance Decode: show detail message decode

Result

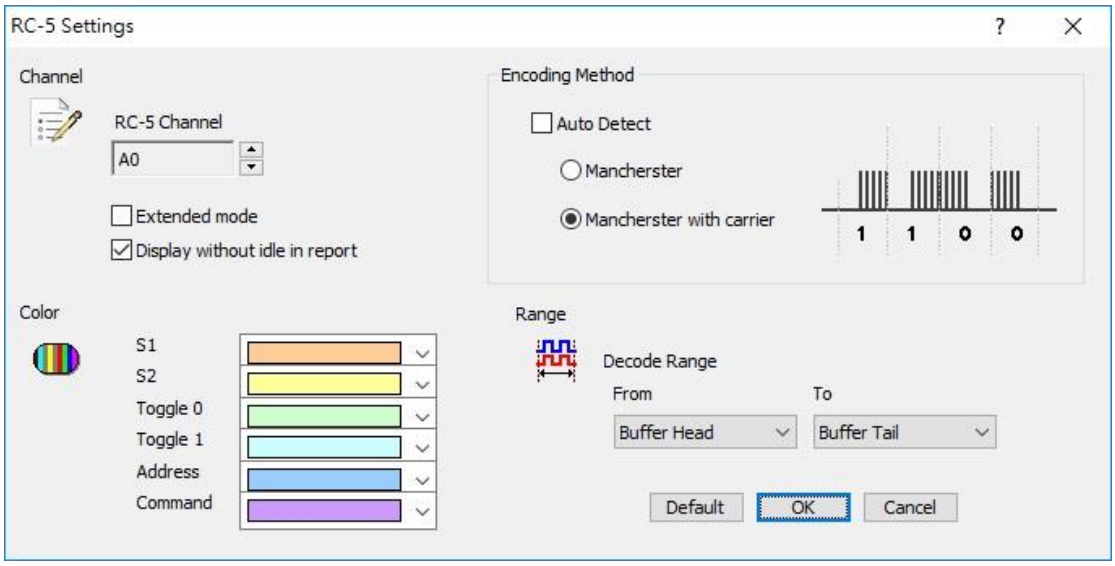


Sample	Header(h)	Message(h)	CheckSum(h)	Error
36.67900000...	Signal Strength (01)	6B	6A	
66.61300000...	Identification (71)	Minor Version (0)		
66.61300000...		Major Version (1)		
66.61300000...		Manufacturer Code (00 10)		
66.61300000...		Basic Device Identifier (00 6A E0 4A)		
66.61300000...		Ext (0)	B1	
130.4770000...	Configuration (51)	Maximun Power (0A)		

RC-5

The RC-5 code from Philips is possibly the most used protocol by hobbyists, probably because of the wide availability of cheap remote controls. The protocol is well defined for different device types ensuring compatibility with your whole entertainment system.

Settings



Channel: Show the selected channel (CH 0).

Extended mode: When the Extended enabled, the S2 will be converted into seventh bit of the Command. There is an Extend Command on the Waveform Window.

Display without idle in report: It will not idle on the Report Window for the user to observe and analyze data.

Encoding Method: Auto Detect mode, Mancherster mode and Mancherster with carrier mode.

S1/S2: Start bit.

Toggle 0/Toggle 1: The difference is that has been used while sending the message to

repeat, or send a new message.

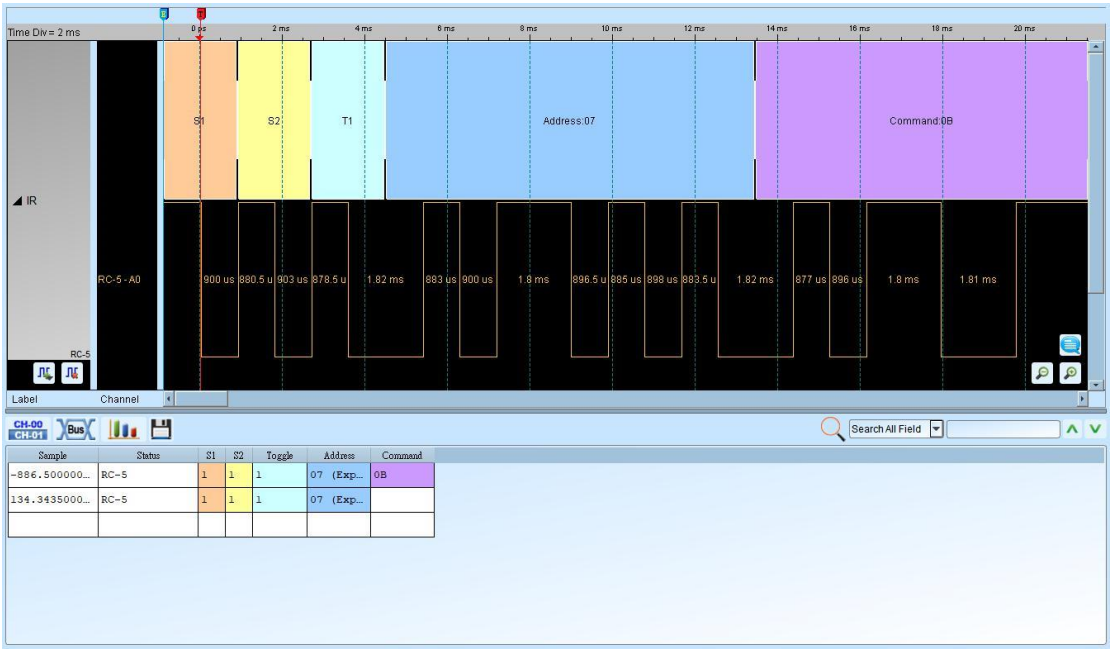
Address: To represent different device addresses.

Command: To represent the different button commands.

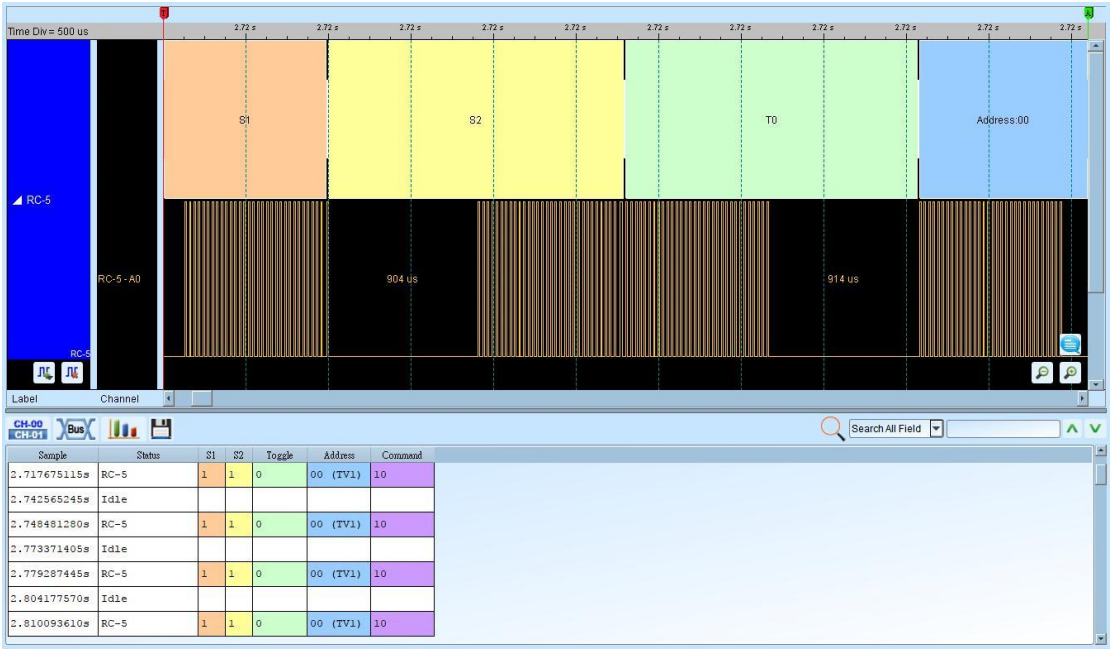
Result

Click **OK** to run the RC-5 decode and see the result on the Waveform Window below.

RC5 without carrier



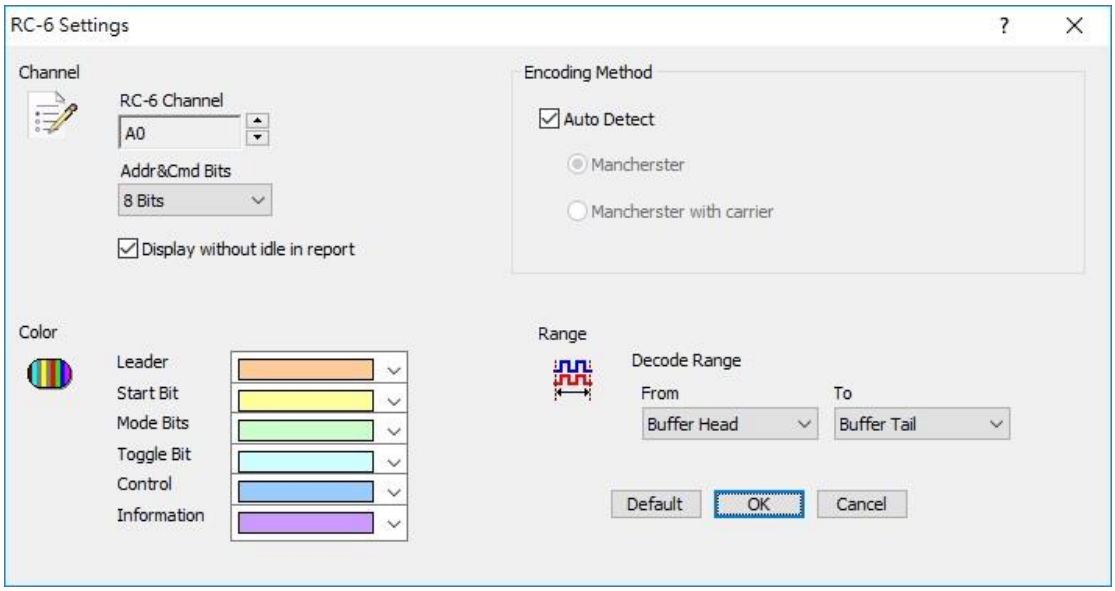
RC5 with carrier



RC-6

RC-6, like RC-5, is also developed by Philips. But, RC-6 has more features of remote controls than RC-5.

Settings



Channel: Show the selected channel (CH 0).

Add & Cmd Bits: Show commands in 8 bits or 16 bits of address and information in the control label.

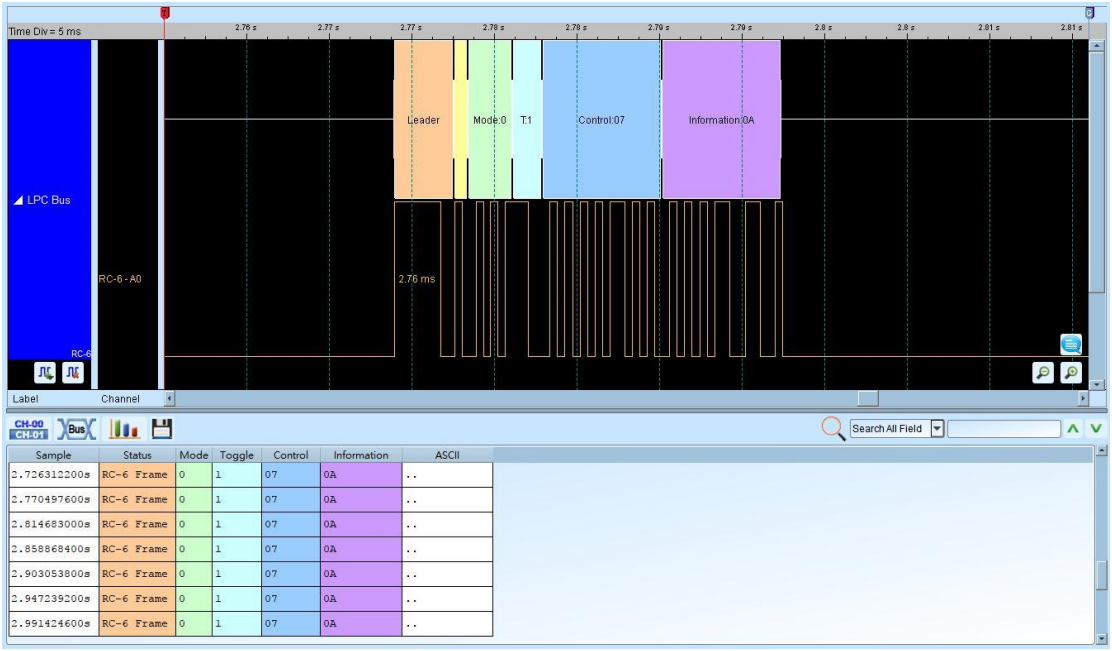
Display without idle in report: Do not display any idle in the Report Window.

Encoding Method: Auto detect mode, Mancherster mode, Mancherster with carrier mode.

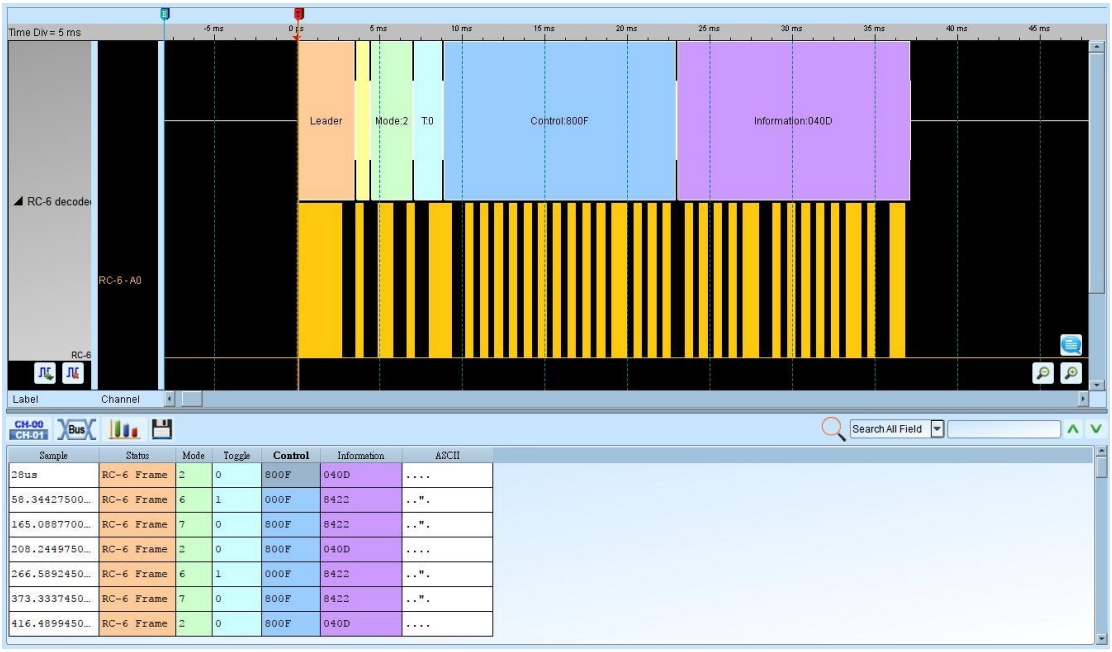
Result

Click **OK** to run the RC-6 decode and see the result on the Waveform Window below.

RC6 without carrier



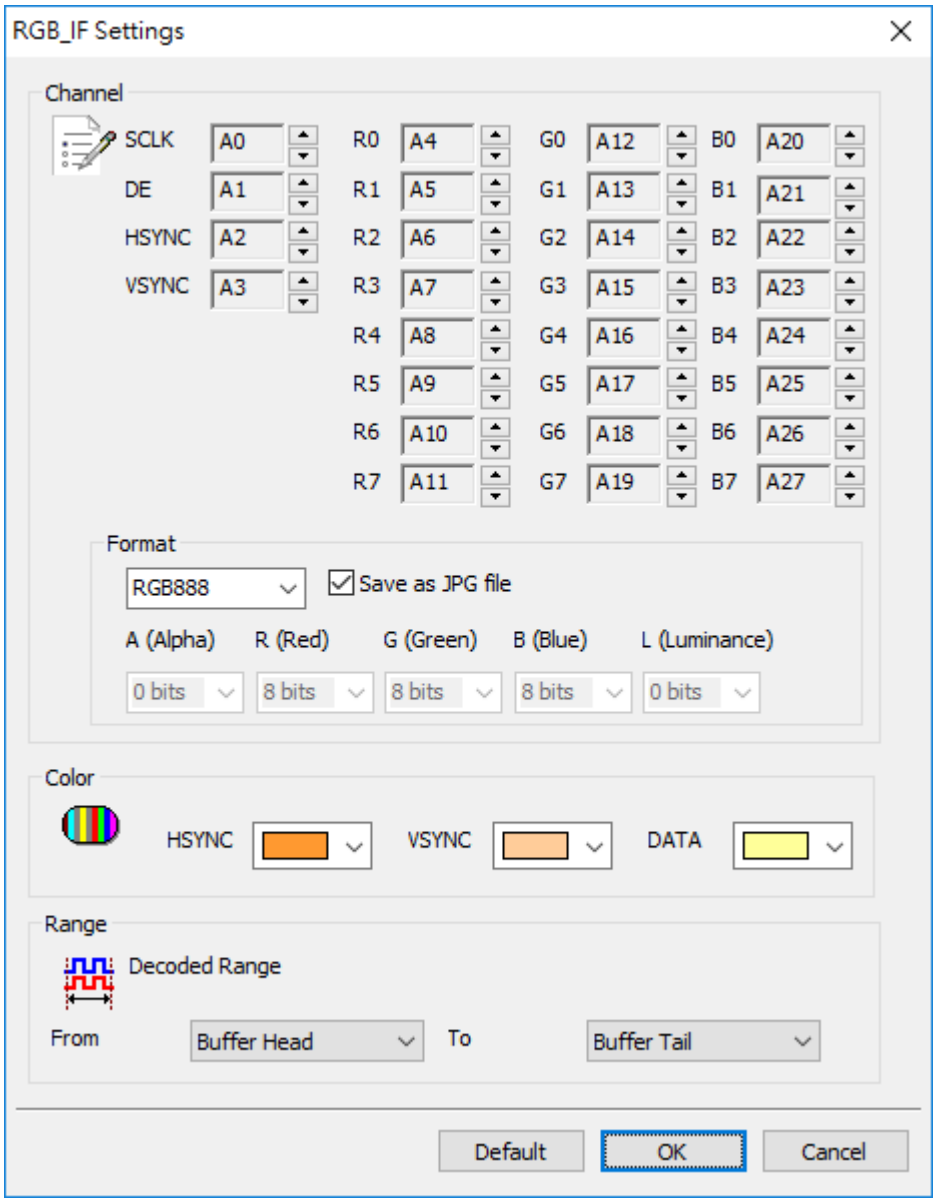
RC6 with carrier



RGB Interface

RGB Interface is for data transmission between MCU and LCD. LCD Panel can be driven by LCD controller. RGB data would be written in memory and can be transmitted to LCD controller. It is able to show the picture of LCD Panel by reading the data from the interface.

Settings



SCLK: The Clock pin.

DE: The Data Enable pin.

Hsync: The Horizontal synchronization pin.

Vsync: The Vertical synchronization pin.

R0 – 7, G0 – 7, B0 – 7: RGB data pins.

Format: Select one of RGB formats or User defined.

Save as JPG file: Generate the JPG file with RGB data in the work directory of LA.

Result

Timestamp	Field	D0 (RGB)	D1 (RGB)	D2 (RGB)	D3 (RGB)	D4 (RGB)	D5 (RGB)	D6 (RGB)	D7 (RGB)
73.57077000…	Ln36, D[16:23]	0C 0F 2A	0D 0E 2B	0A 16 28	0B 0F 27	0B 0F 27	0B 1A 2B	12 12 3B	13 13 3C
73.57210000…	Ln36, D[24:31]	13 13 3C	0F 0F 32	07 08 1B	13 13 3C	13 13 3C	08 09 1E	0A 09 24	07 08 1A
73.57343500…	Ln36, D[32:39]	11 11 37	13 11 36	07 08 1B	0B 0B 25	07 08 1C	13 13 3C	13 13 3C	13 1A 3D
73.57477000…	Ln36, D[40:47]	0D 0E 2E	06 08 19	02 01 38	0B 0C 26	08 09 1D	02 01 3C	08 09 1C	0B 0C 27
73.57610000…	Ln36, D[48:55]	05 07 18	09 0A 20	09 0A 20	05 07 18	0D 0E 2D	05 07 18	13 13 3C	11 13 3D
73.57743500…	Ln36, D[56:63]	06 08 1A	13 13 3C	13 1A 3C	13 13 3C	05 07 18	09 0A 20	09 0A 20	07 08 1B
73.57877000…	Ln36, D[64:71]	08 09 1F	06 08 1A	12 12 3B	13 13 3C	0D 0D 2B	07 08 1C	13 13 3C	13 13 3C

S/PDIF

The Sony/Philips Digital Interconnect Format (S/PDIF) is a digital audio transmission interface with the detailed specifications below:

Data format: Default is 16 bits, up to 24 bits.

Sampling frequency:

44.1Khz from CD → Bit Rate 2.8224 Mbit/s

48 Khz from DAT →Bit Rate 3.072 Mbit/s

32 Khz from DSR → Bit Rate 2.048 Mbit/s

Deliver method: One way.

V (Validity) bit: Audio samples to confirm effectiveness, if this bit is 0, the receiver should ignore this sub-frame.

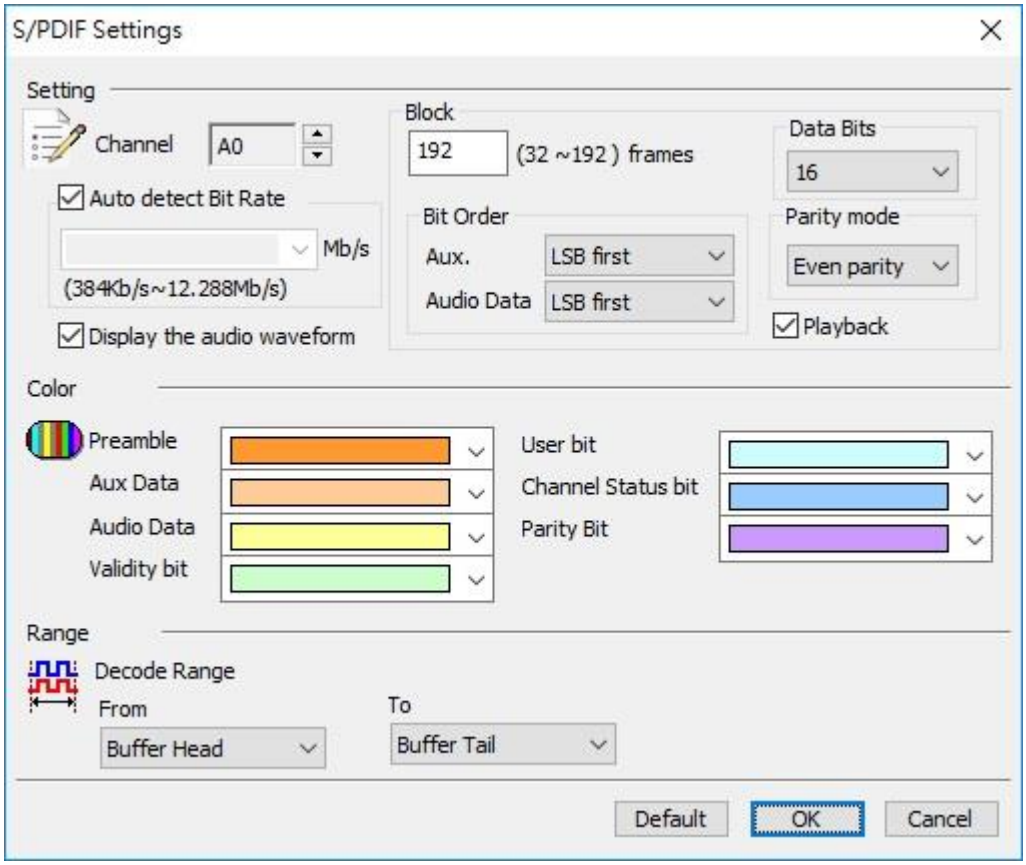
U (User) bit: User log information.

C (Channel status) bit: Channel state information.

P (Parity) bit: Parity bit check for the error.

The basic principle is to split the data bits into two parts. If the data is 1, split it into 01 or 10 or if the data is 0, split it into 00 or 11.

Settings



Channel: The default is Channel 0.

Auto detect Bit Rate: Turned on by default.

Num of frame: 192 frames within each block by default, used to analyze each sub-frame order User bit and Channel status bit.

Bit Order (Aux. Data): The default is the LSB first for the Aux. data.

Bit Order (Audio Data): The default is the LSB first for Audio data.

Data format: The default is 16 bits.

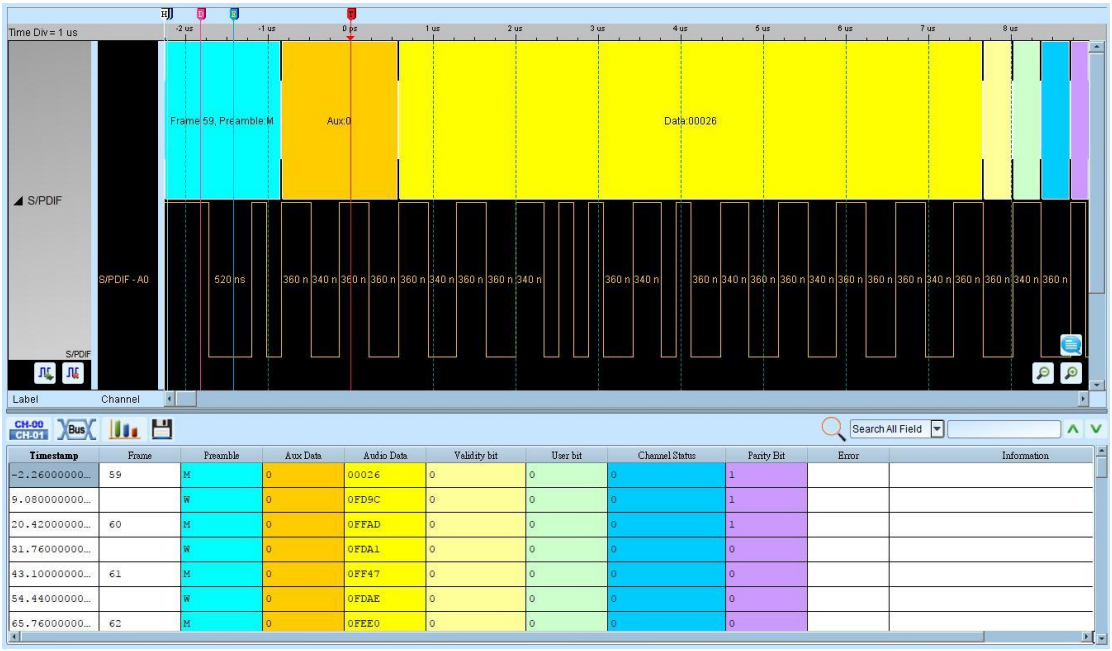
Parity mode: The default is even parity.

Display the audio waveform: Click to display the audio waveform in the Waveform Window.

Result

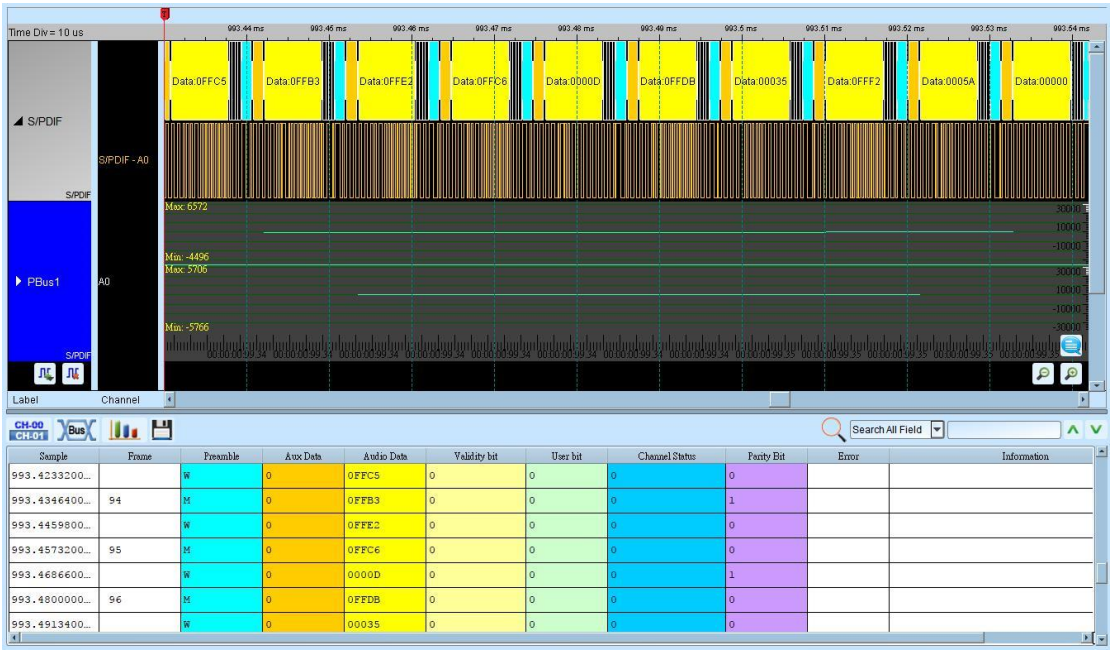
Click **OK** to run the S/PDIF Decode and see the result on the Waveform Window

below.



Timestamp	Frame	Preamble	Aux Data	Audio Data	Validity bit	User bit	Channel Status	Parity Bit	Error	Information
-2.26000000...	59	M	0	00026	0	0	0	1		
9.08000000...		W	0	0FD9C	0	0	0	1		
20.42000000...	60	M	0	0FFAD	0	0	0	1		
31.76000000...		W	0	0FDA1	0	0	0	0		
43.10000000...	61	M	0	0FF47	0	0	0	0		
54.44000000...		W	0	0FDAE	0	0	0	0		
65.76000000...	62	M	0	0FEE0	0	0	0	0		

Show wave:

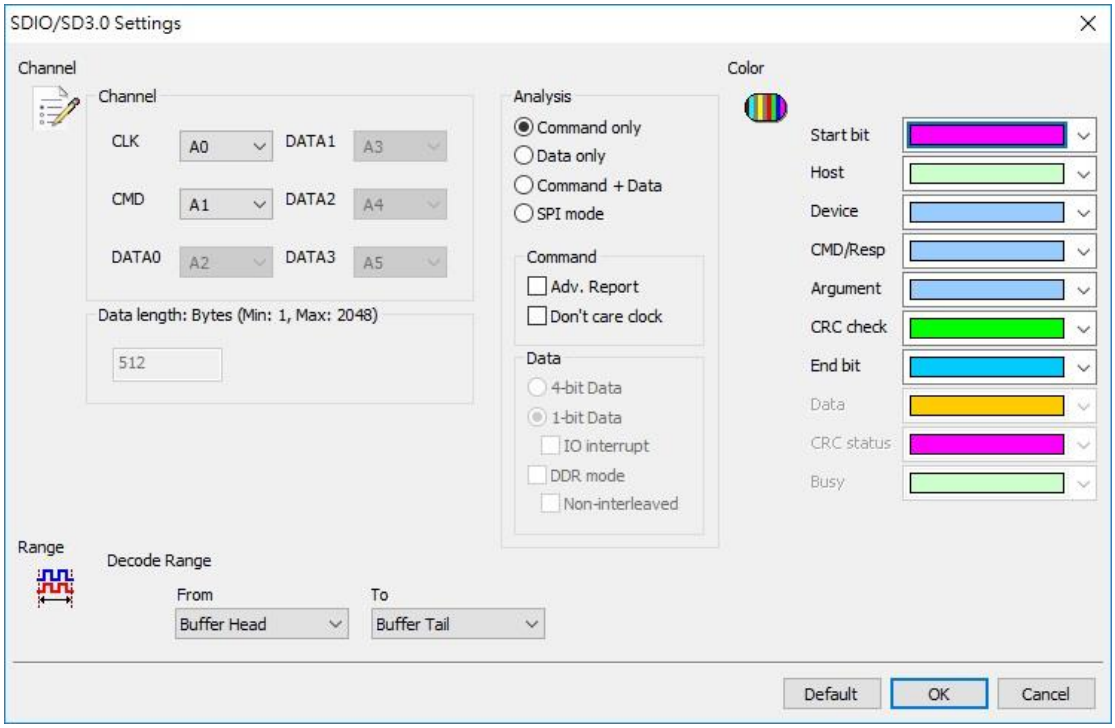


Sample	Frame	Preamble	Aux Data	Audio Data	Validity bit	User bit	Channel Status	Parity Bit	Error	Information
993.4233200...		W	0	0FFC5	0	0	0	0		
993.4346400...	94	M	0	0FFB3	0	0	0	1		
993.4459800...		W	0	0FFE2	0	0	0	0		
993.4573200...	95	M	0	0FFC6	0	0	0	0		
993.4686600...		W	0	0000D	0	0	0	1		
993.4800000...	96	M	0	0FFDB	0	0	0	0		
993.4913400...		W	0	00035	0	0	0	0		

SDIO

The SD3.0/SDIO3.0 Protocol is a high speed serial protocol used primarily for interfacing with SD (Secure Digital) Flash memory cards.

Settings



Channel: Show the selected channels.

Command only: Analyze the command.

Data only: Analyze the data.

Command + Data: Analyze Command and Data in the report window.

Adv. Report: Analyze the command argument

Don't care clock: decode only depend on the CMD channel.

Data: 1/4/8 bits or DDR mode, check "IO interrupt" when SDIO 1 bit mode and support the IO interrupt decode via DATA1 channel, check "DDR mode" and " "Non-interleaved" to analyze data without interleaved.

Data length: Set the length of data.

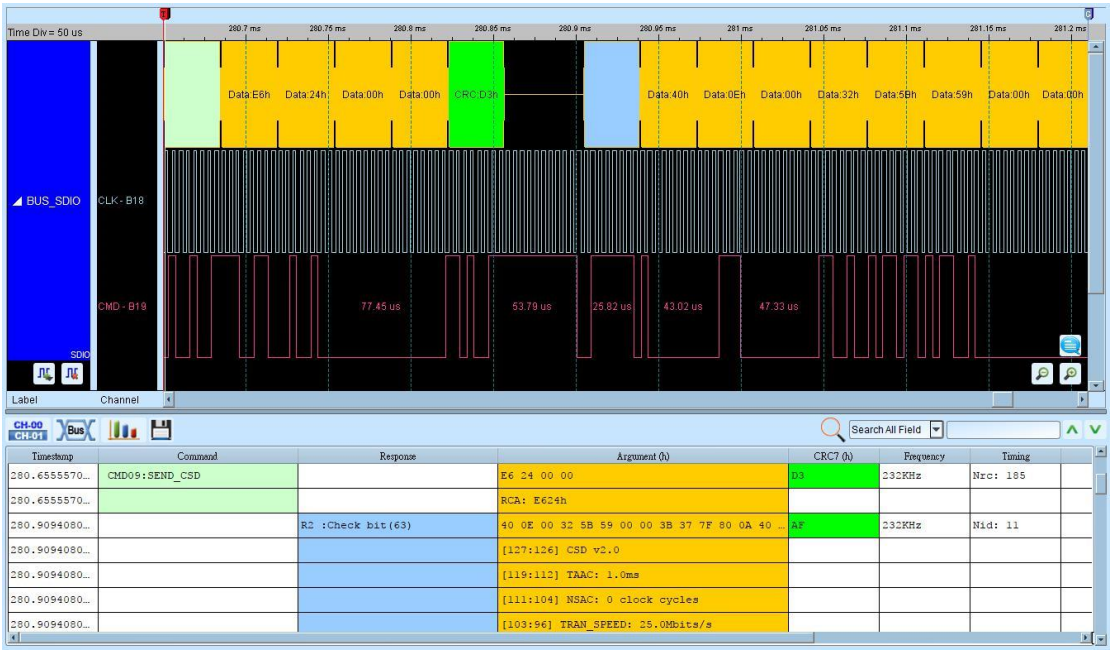
Result

Click **OK** to run the SDI/O decode and see the result on the Waveform Window below.

CMD mode

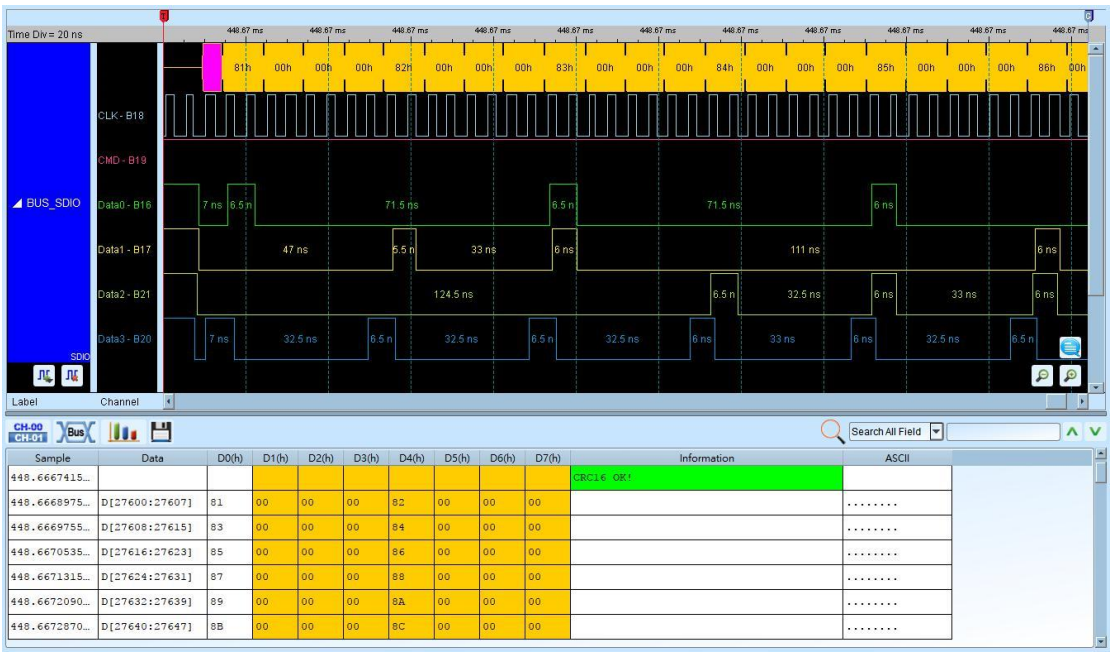
Sample	Command	Response	Argument (h)	CRC7 (h)	Frequency	Timing
3.327234924s		R1Bb:CMD12:STOP_TRANSMISSION	00 00 0B 00	7F	206MHz	Ncr: 13
3.328740484s	CMD18:READ_MULTIPLE_BLOCK		00 00 09 C8	9D	206MHz	Nrc: 311446
3.328740781s		R1 :CMD18:READ_MULTIPLE_BLOCK	00 00 09 00	D3	206MHz	Ncr: 13
3.334268240s	CMD12:STOP_TRANSMISSION		00 00 00 00	61	204MHz	Nrc: 1131372
3.334268540s		R1Bb:CMD12:STOP_TRANSMISSION	00 00 0B 00	7F	204MHz	Ncr: 13
3.337817406s	CMD18:READ_MULTIPLE_BLOCK		00 00 0D C8	C5	205MHz	Nrc: 729483
3.337817706s		R1 :CMD18:READ_MULTIPLE_BLOCK	00 00 09 00	D3	206MHz	Ncr: 13

Adv. Report



Timestamp	Command	Response	Argument (h)	CRC7 (h)	Frequency	Timing
280.6555570...	CMD09:SEND_CSD		E6 24 00 00	D3	232KHz	Nrc: 185
280.6555570...			RCA: E624h			
280.9094080...		R2 :Check bit(63)	40 0E 00 32 5B 59 00 00 3B 37 7F 80 0A 40 ...	AF	232KHz	Nid: 11
280.9094080...			[127:126] CSD v2.0			
280.9094080...			[119:112] TAAC: 1.0ms			
280.9094080...			[111:104] NSAC: 0 clock cycles			
280.9094080...			[103:96] TRAN_SPEED: 25.0Mbits/s			

Data mode

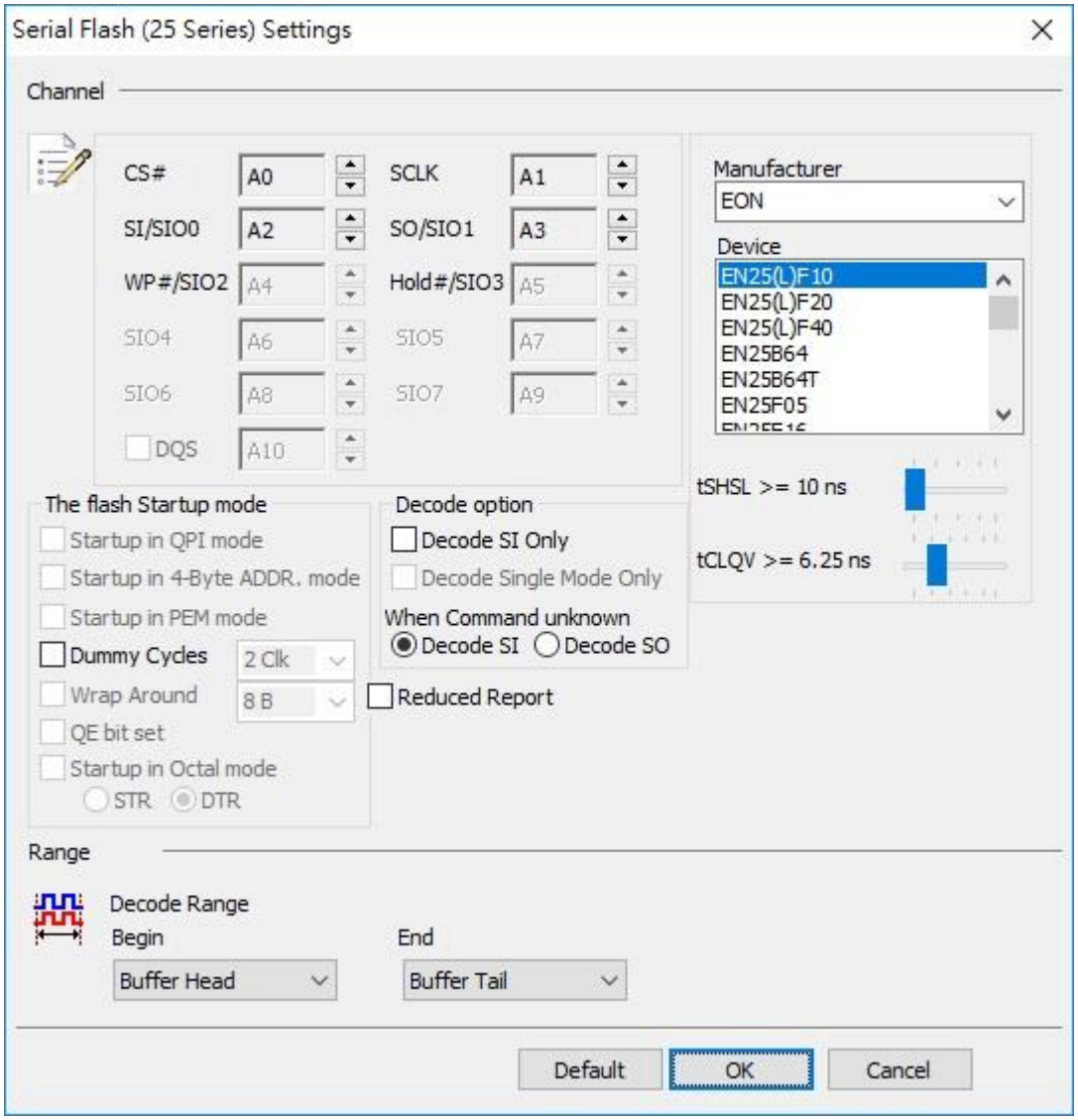


Sample	Data	D0(h)	D1(h)	D2(h)	D3(h)	D4(h)	D5(h)	D6(h)	D7(h)	Information	ASCII
448.6667415...										CRC16 OK!	
448.6668975...	D[27600:27607]	81	00	00	00	82	00	00	00		....
448.6669755...	D[27608:27615]	83	00	00	00	84	00	00	00		....
448.6670535...	D[27616:27623]	85	00	00	00	86	00	00	00		....
448.6671315...	D[27624:27631]	87	00	00	00	88	00	00	00		....
448.6672090...	D[27632:27639]	89	00	00	00	8A	00	00	00		....
448.6672870...	D[27640:27647]	8B	00	00	00	8C	00	00	00		....

Serial Flash

SPI Serial Flash is small, low-power flash memory that features Serial Peripheral Interface (SPI) and pin-for-pin compatibility with industry-standard SPI EEPROM devices.

Settings



Channel: Show the selected channels (CH0 – CH5).

Manufacturer/Device: Select the Serial Flash device type, tCLQV and tSHSL.

QPI mode: Quad Peripheral Interface Mode/Quad SPI Mode

4-Byte mode: 4-Byte Address Mode

PEM mode: Performance Enhance Mode

Dummy Cycles: Clock buffers between read command and data.

Wrap Around: Wrap number

QE bit: Enable or disable the QPI mode.

Decode SI Only: Single mode, 3-wire → CS#, SCLK, SI.

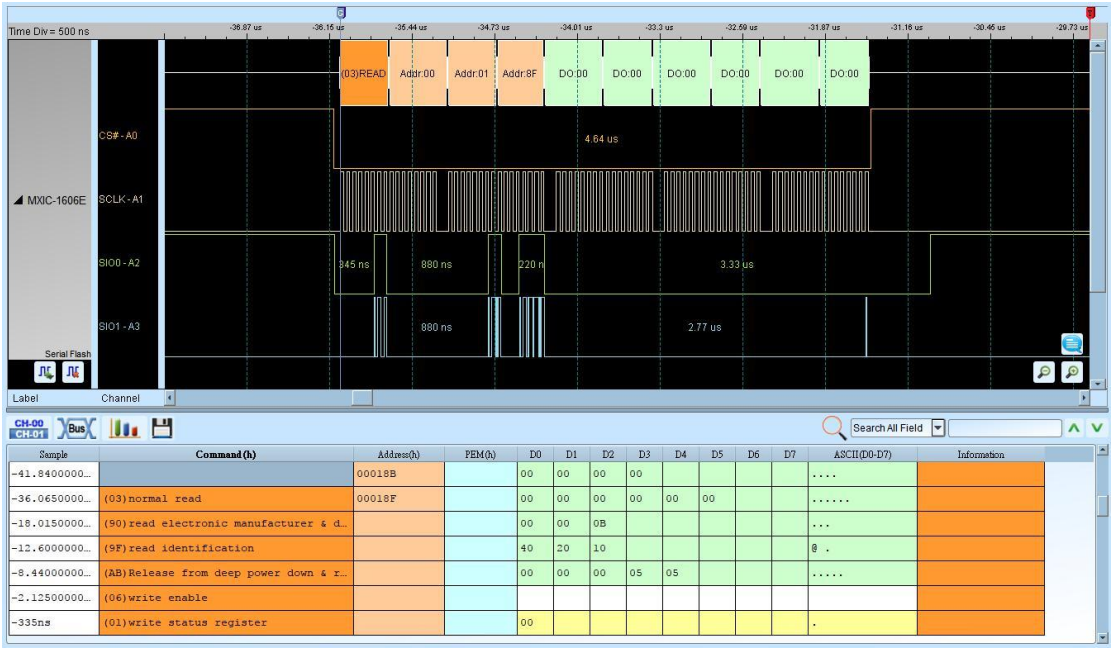
Decode Single Mode Only: Single mode, 4-wire → CS, Clock, SI, SO.

The LA viewer will choose 4-wire or 6-wire to analyze according to the Serial Flash device type.

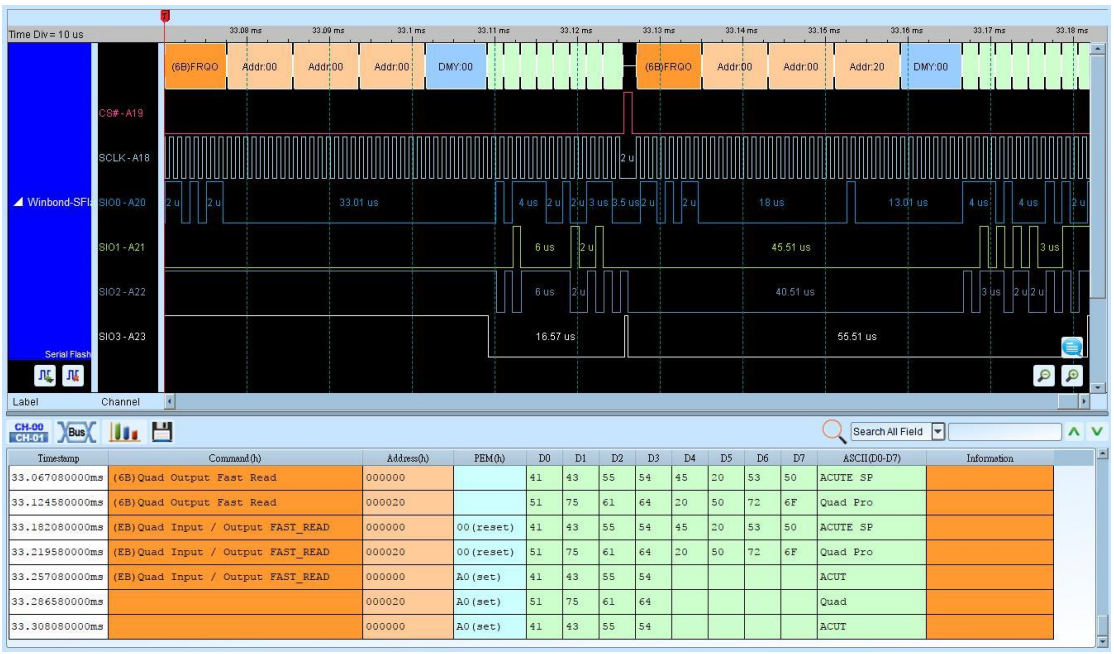
Result

Click **OK** to run the Serial Flash decode and see the result on the Waveform Window below.

Serial Flash decode within SPI mode.



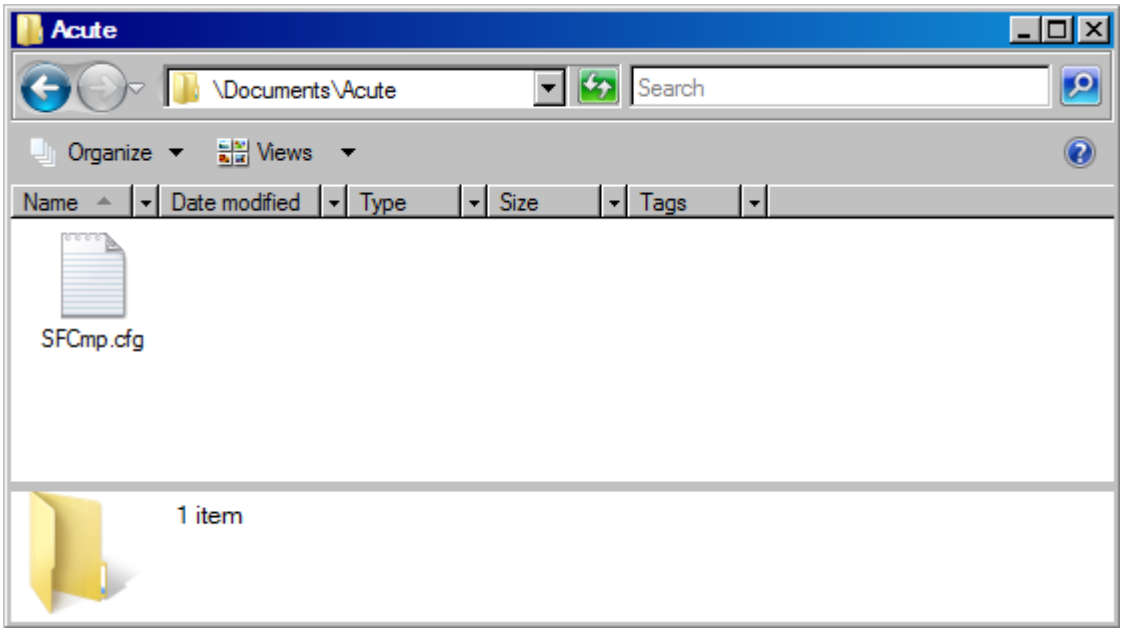
Serial Flash decode within QPI mode.



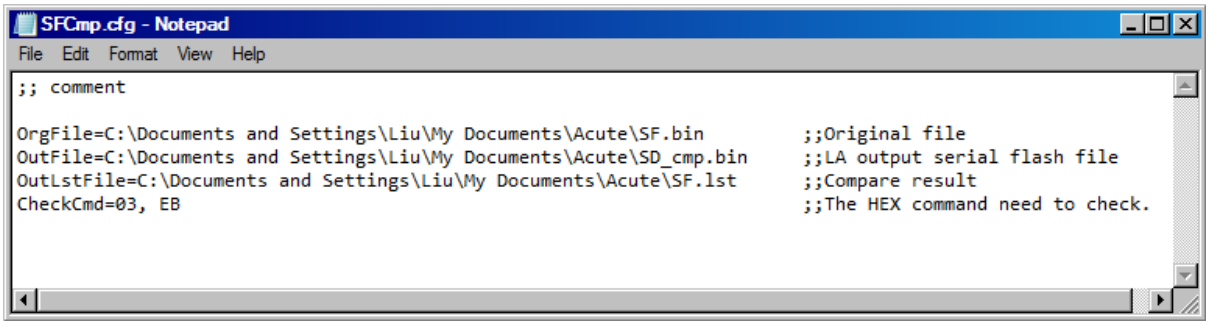
Timestamp	Command (h)	Address(h)	PEM(h)	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Information
33.067080000ms	(6B)Quad Output Fast Read	000000		41	43	55	54	45	20	53	50	ACUTE SP	
33.124580000ms	(6B)Quad Output Fast Read	000020		51	75	61	64	20	50	72	6F	Quad Pro	
33.182080000ms	(EB)Quad Input / Output FAST_READ	000000	00(reset)	41	43	55	54	45	20	53	50	ACUTE SP	
33.219580000ms	(EB)Quad Input / Output FAST_READ	000020	00(reset)	51	75	61	64	20	50	72	6F	Quad Pro	
33.257080000ms	(EB)Quad Input / Output FAST_READ	000000	A0(set)	41	43	55	54					ACUT	
33.286580000ms		000020	A0(set)	51	75	61	64					Quad	
33.308080000ms		000000	A0(set)	41	43	55	54					ACUT	

Serial Flash data Comparison : Compare the Serial Flash data by the waveform files.

Method: Create a file by text editor and save it as SFCmp.cfg in order to compare with the real Serial Flash waveform to find the bug, the default path is “My Documents\Acute”



SFCmp.cfg information:



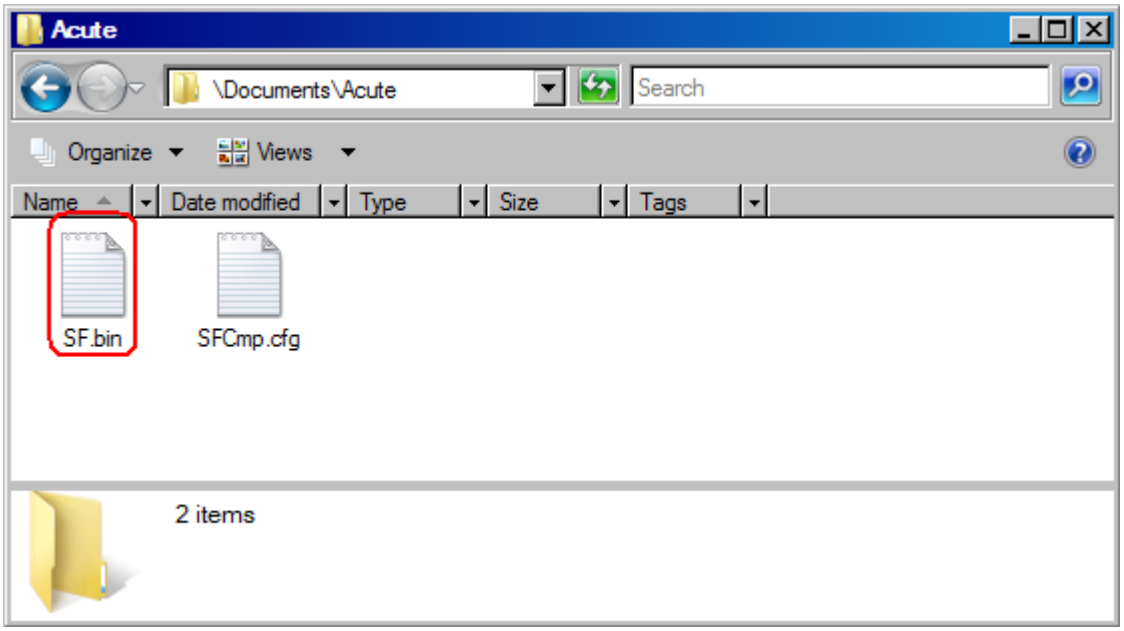
OrgFile=File_Path: Key in the file path of the original Serial Flash data file (.bin).

OutFile=File_Path: Key in the file path of the Serial Flash output file.

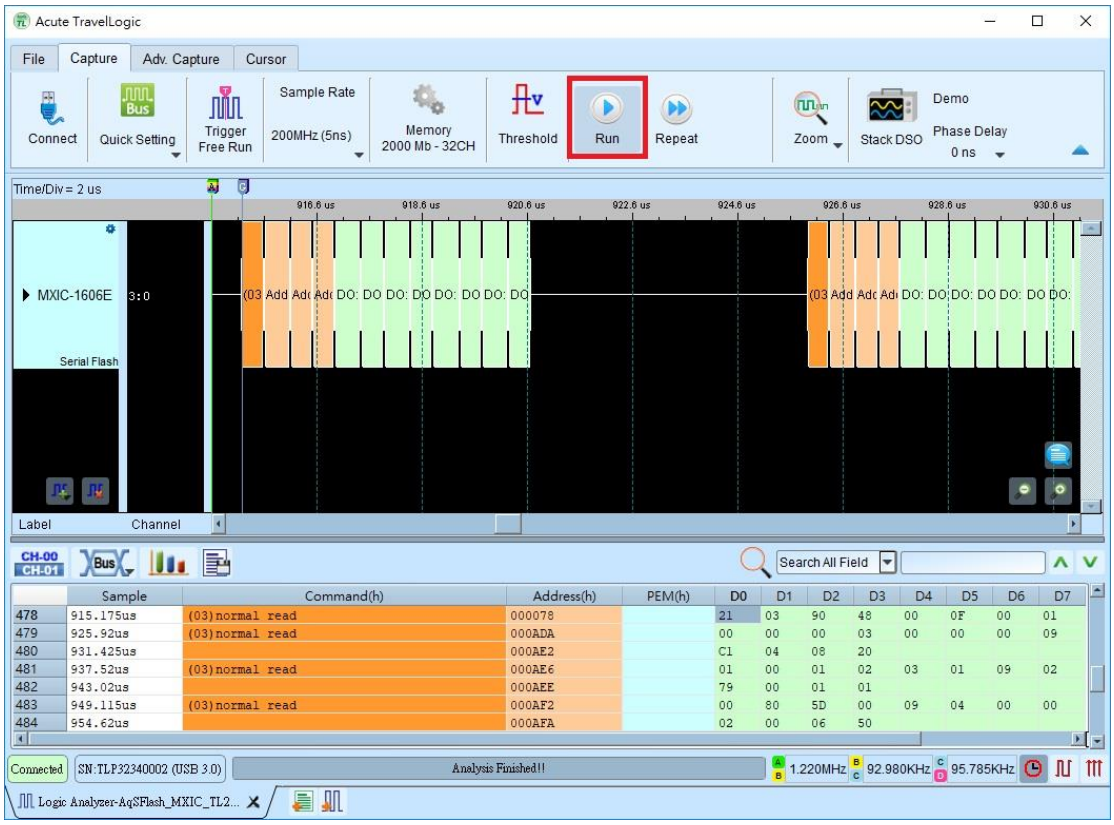
OutLstFile=File_Path: Key in the file path of the comparison result. The file name will has extension ".lst".

CheckCmd=Serial Flash command: Key in the command in Hex that are separated by commas.

Save the OrgFile to the OrgFile file path.

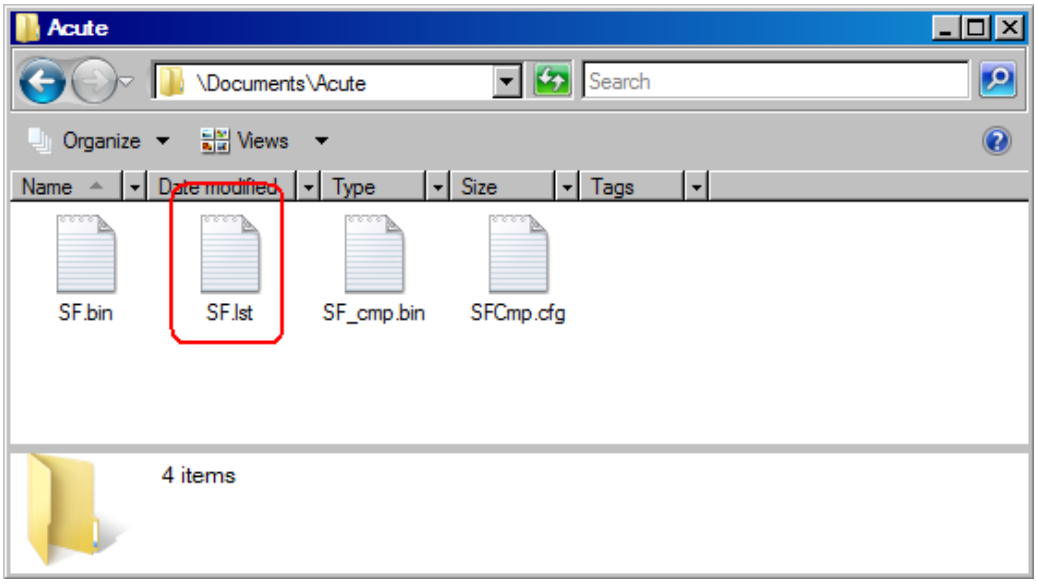


Run the Serial Flash Bus Decode to capture the Serial Flash signal.

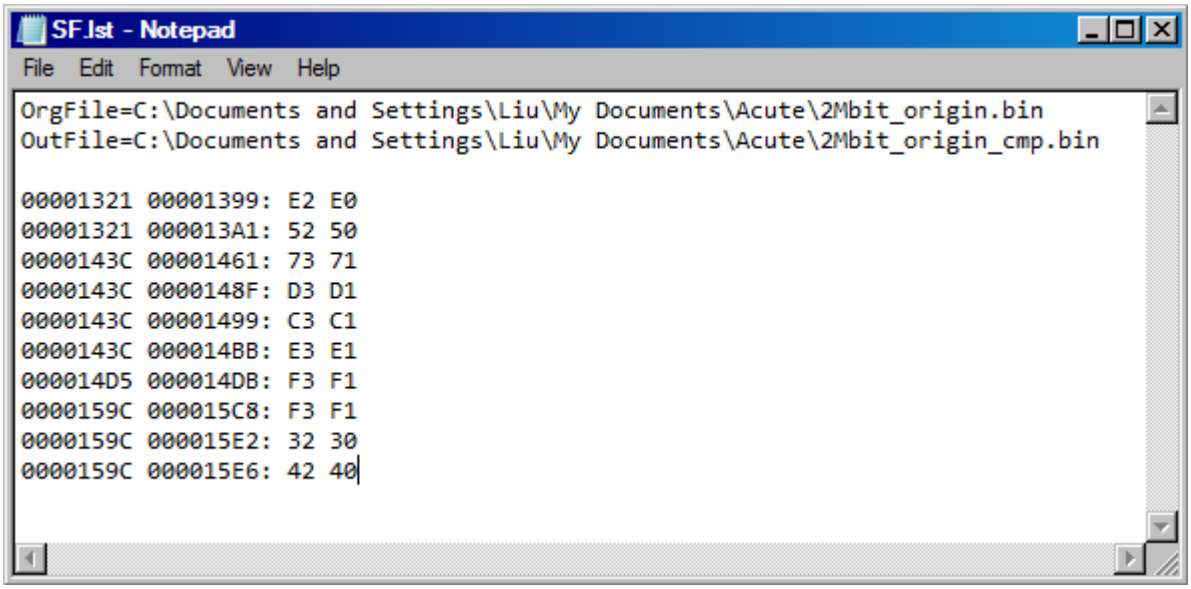


If the OutFile does not exit, it will copy the OrgFile to the OutFile and write the data to it according to the CheckCmd.

Compare result:



The OutLstFile:

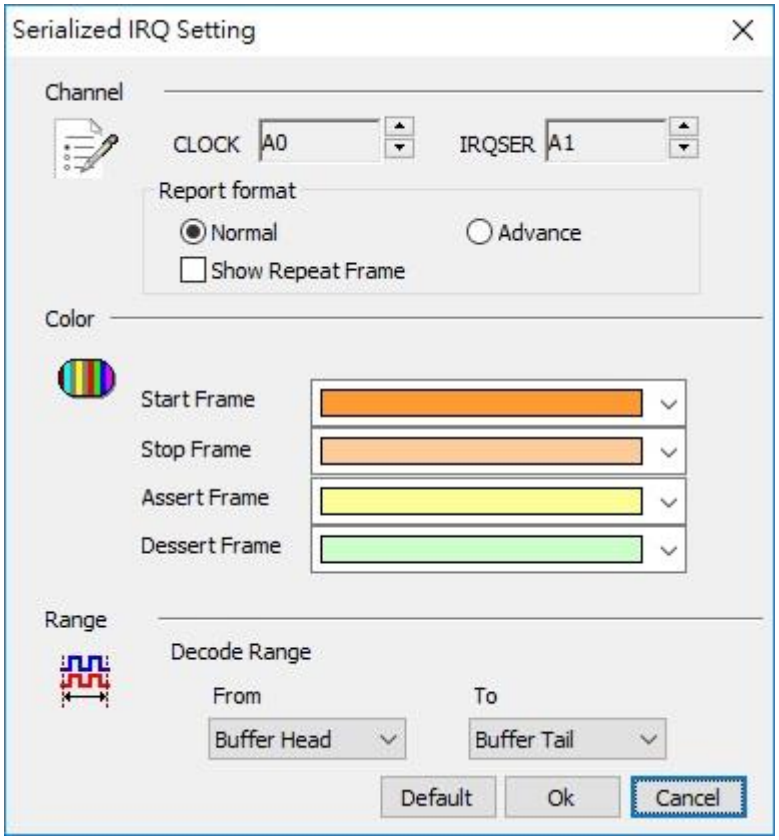


The first column is the compared address from OrgFile, the second column is the different address from OutFile.

Serial IRQ

The IRQ/Data serializer is a Wired-OR structure that simply passes the state of one or more device's IRQ(s) and/or Data to the host controller. The transfer can be initiated by either a device or the host controller. A transfer, called an IRQSER Cycle, consists of three frame types: one Start Frame, several IRQ/Data Frames, and one Stop Frame. This protocol uses the PCI Clock as its clock source and conforms to the PCI bus electrical specification.

Settings



CLOCK: PCI Clock channel

IRQSER; IRQSER channel

Normal: Not show repeat frame

Clock	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IRQ
10286946	22830	Continue mode		A					A						A				
10291906	22841	Continue mode		A											A				
10404663	23091	Continue mode		A					A						A				
10415039	23114	Continue mode		A											A				
10459240	23212	Continue mode		A					A						A				
10461943	23218	Continue mode		A											A				
10580112	23480	Continue mode		A					A						A				
10590037	23502	Continue mode		A											A				
10634238	23600	Continue mode		A					A						A				
10636941	23606	Continue mode		A											A				

Show repeat frame

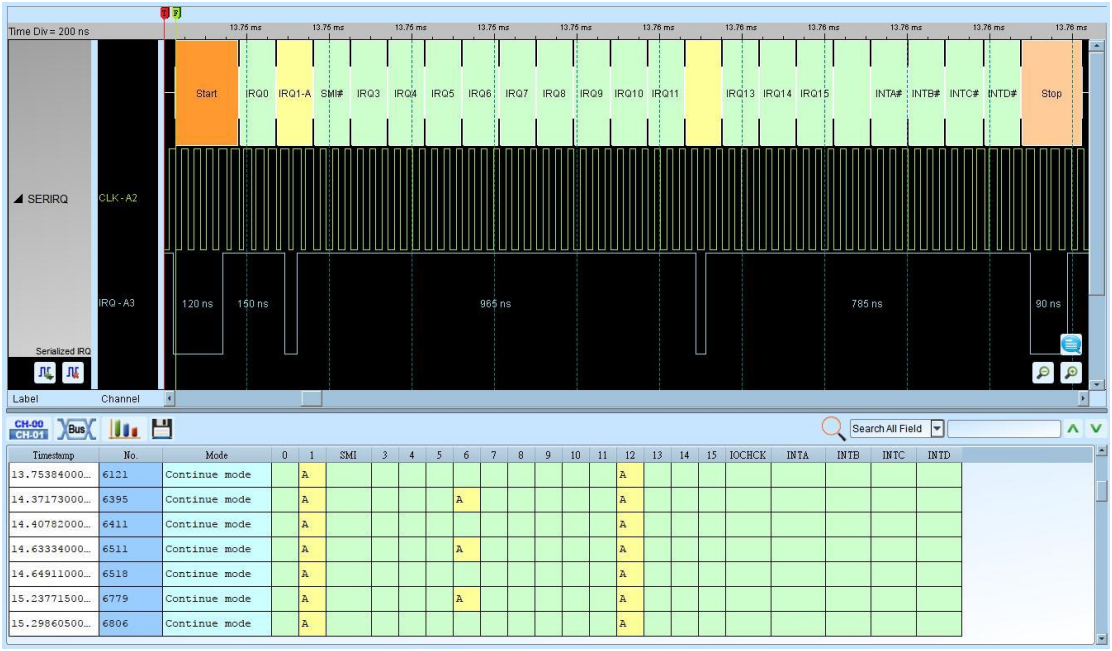
Clock	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IRQ
10457887	23209	Continue mode		A											A				
10458338	23210	Continue mode		A											A				
10458789	23211	Continue mode		A											A				
10459240	23212	Continue mode		A					A						A				
10459690	23213	Continue mode		A					A						A				
10460140	23214	Continue mode		A					A						A				
10460590	23215	Continue mode		A					A						A				
10461041	23216	Continue mode		A					A						A				
10461492	23217	Continue mode		A					A						A				
10461943	23218	Continue mode		A											A				
10462394	23219	Continue mode		A											A				
10462846	23220	Continue mode		A											A				
10463298	23221	Continue mode		A											A				

Advance:

Clock	IRQ/Data Frame	Signal Sampled	# of clocks past Start
-9470	1	IRQ0	2
-9452	2	IRQ1	5
-9434	3	SMI#	8
-9416	4	IRQ3	11
-9398	5	IRQ4	14
-9380	6	IRQ5	17
-9362	7	IRQ6	20
-9344	8	IRQ7	23
-9326	9	IRQ8	26
-9308	10	IRQ9	29
-9290	11	IRQ10	32
-9272	12	IRQ11	35
-9254	13	IRQ12	38
-9236	14	IRQ13	41
-9217	15	IRQ14	44
-9199	16	IRQ15	47
-9181	17	IOCHCK#	50
-9163	18	INTA#	53
-9145	19	INTB#	56
-9127	20	INTC#	59
-9109	21	INTD#	62
-9019	1	IRQ0	2
-9001	2	IRQ1	5

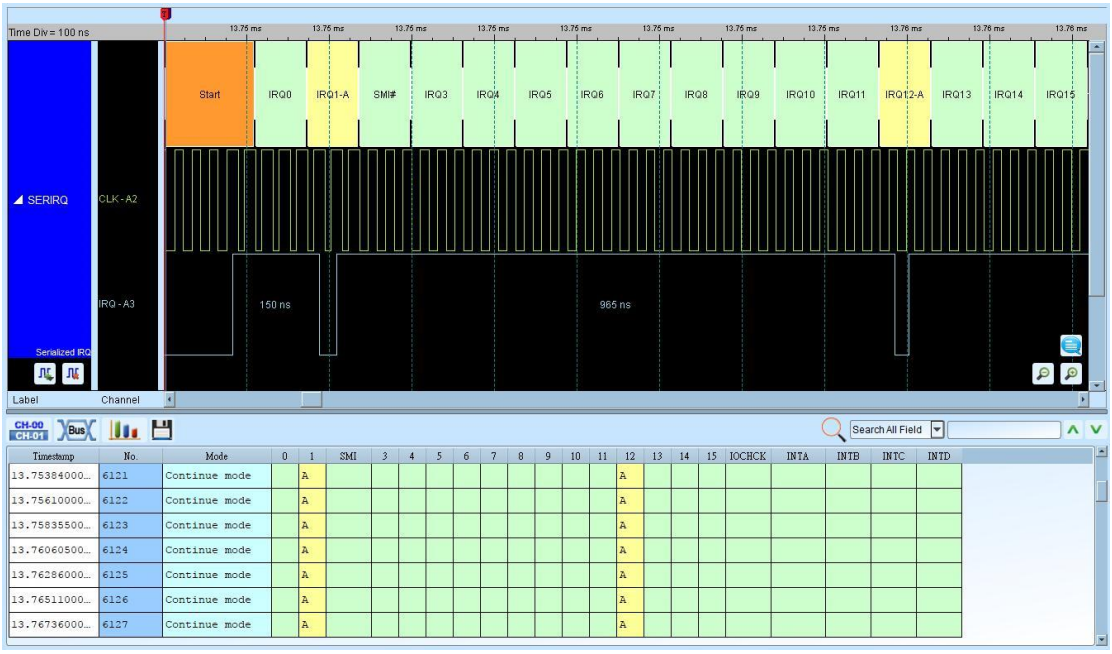
Result

Normal mode



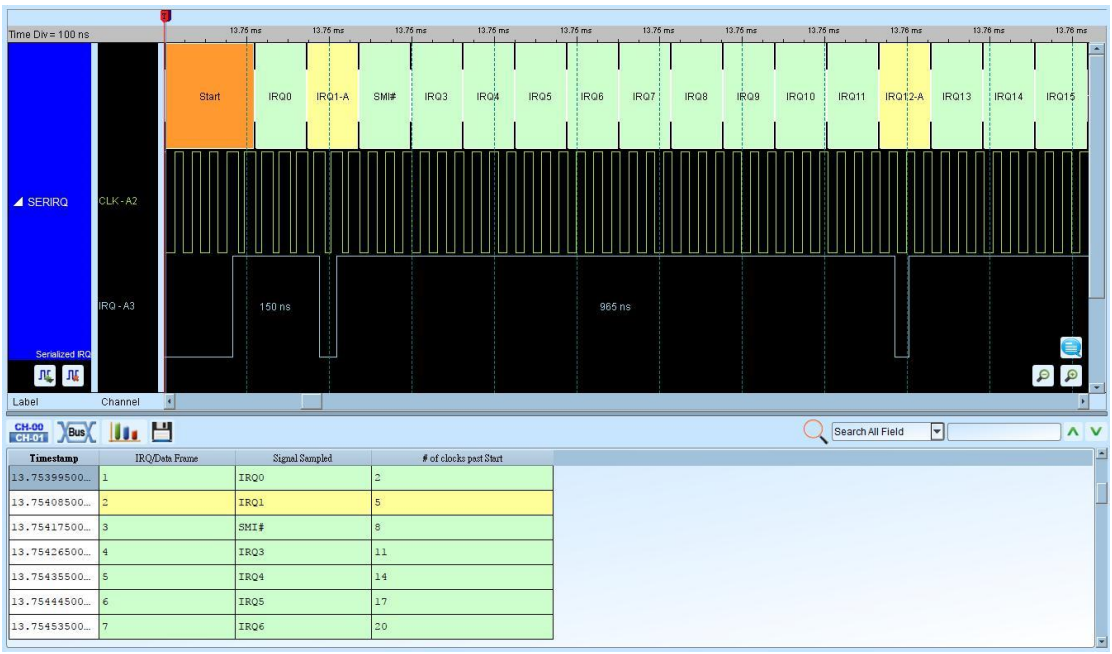
Timestamp	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IOCHCK	INTA	INTB	INTC	INTD
13.75384000...	6121	Continue mode		A											A								
14.37173000...	6395	Continue mode		A					A						A								
14.40782000...	6411	Continue mode		A											A								
14.63334000...	6511	Continue mode		A					A						A								
14.64911000...	6518	Continue mode		A											A								
15.23771500...	6779	Continue mode		A					A						A								
15.29860500...	6806	Continue mode		A											A								

Normal mode(Show repeat frame)



Timestamp	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IOCHCK	INTA	INTB	INTC	INTD
13.75384000...	6121	Continue mode		A											A								
13.75610000...	6122	Continue mode		A											A								
13.75835500...	6123	Continue mode		A											A								
13.76060500...	6124	Continue mode		A											A								
13.76286000...	6125	Continue mode		A											A								
13.76511000...	6126	Continue mode		A											A								
13.76736000...	6127	Continue mode		A											A								

Advance mode

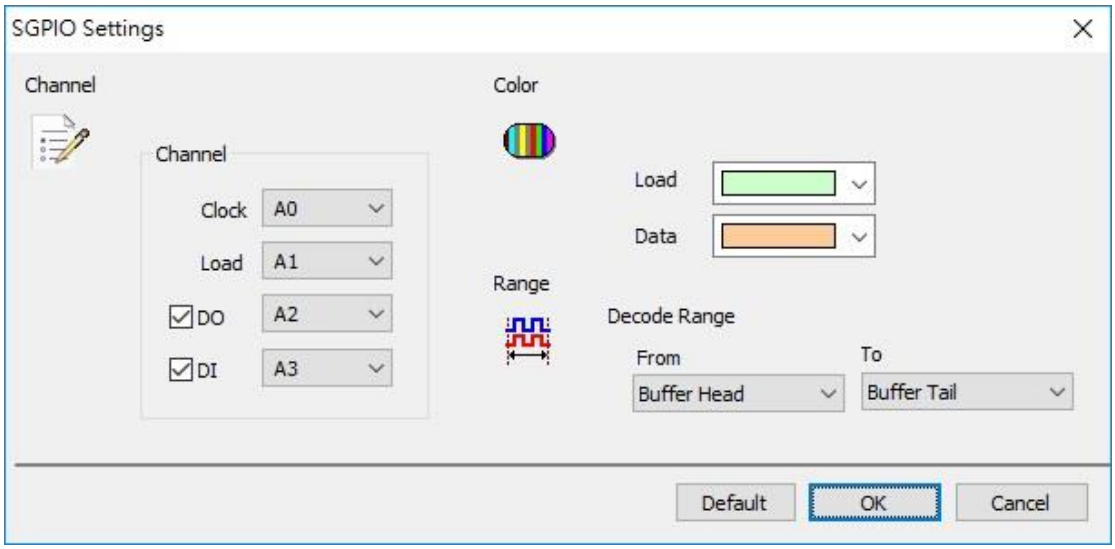


Timestamp	IRQ/Data Frame	Signal Sampled	# of clocks past Start
13.75399500...	1	IRQ0	2
13.75408500...	2	IRQ1	5
13.75417500...	3	SMI#	8
13.75426500...	4	IRQ3	11
13.75435500...	5	IRQ4	14
13.75444500...	6	IRQ5	17
13.75453500...	7	IRQ6	20

Serial General Purpose Input Output (SGPIO)

The SGPIO is a method to serialize general purpose IO signals. SGPIO defines the communication between an initiator and a target.

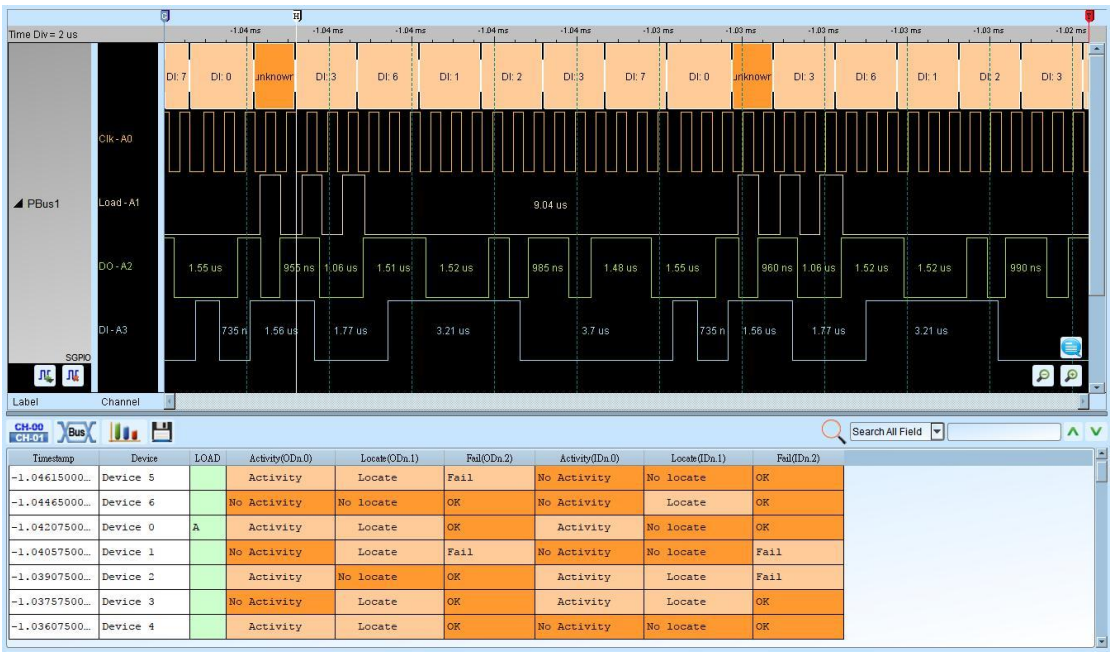
Settings



Channel: Show the selected channels (Clock, Load and Data), it can only use data out or date in or both.

Result:

Click OK to run the Smart Card decode and see the result on the Waveform Window below.

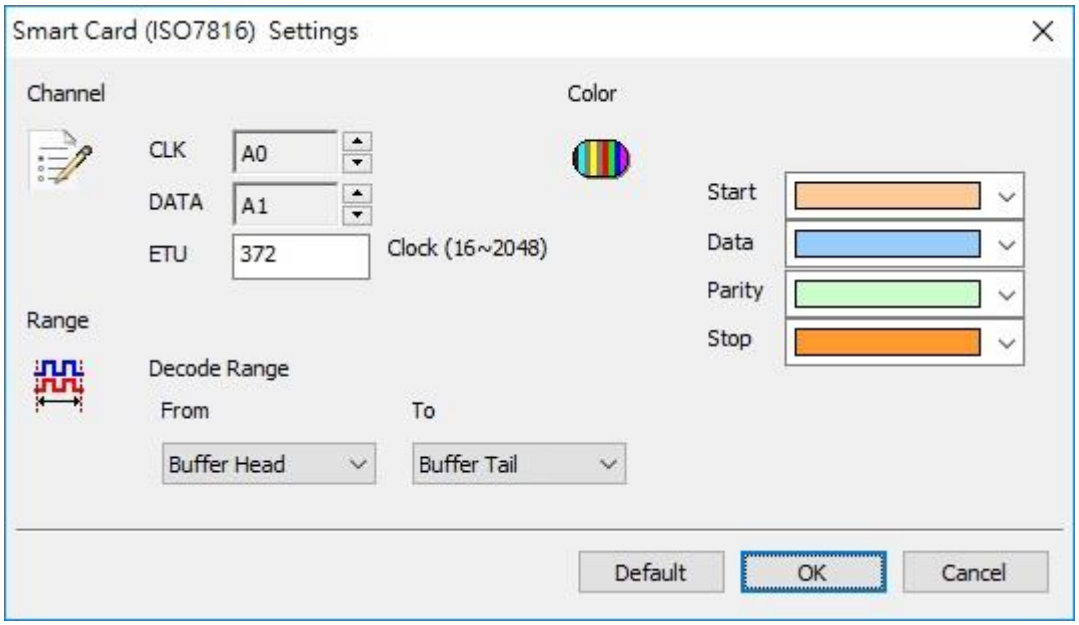


Timestamp	Device	LOAD	Activity(ODn.0)	Locate(ODn.1)	Fail(ODn.2)	Activity(IDn.0)	Locate(IDn.1)	Fail(IDn.2)
-1.04615000...	Device 5		Activity	Locate	Fail	No Activity	No locate	OK
-1.04465000...	Device 6		No Activity	No locate	OK	No Activity	Locate	OK
-1.04207500...	Device 0	A	Activity	Locate	OK	Activity	No locate	OK
-1.04057500...	Device 1		No Activity	Locate	Fail	No Activity	No locate	Fail
-1.03907500...	Device 2		Activity	No locate	OK	Activity	Locate	Fail
-1.03757500...	Device 3		No Activity	Locate	OK	Activity	Locate	OK
-1.03607500...	Device 4		Activity	Locate	OK	No Activity	No locate	OK

Smart Card (ISO7816)

The card is made of plastic and provides strong security authentication for single sign-on within large organizations.

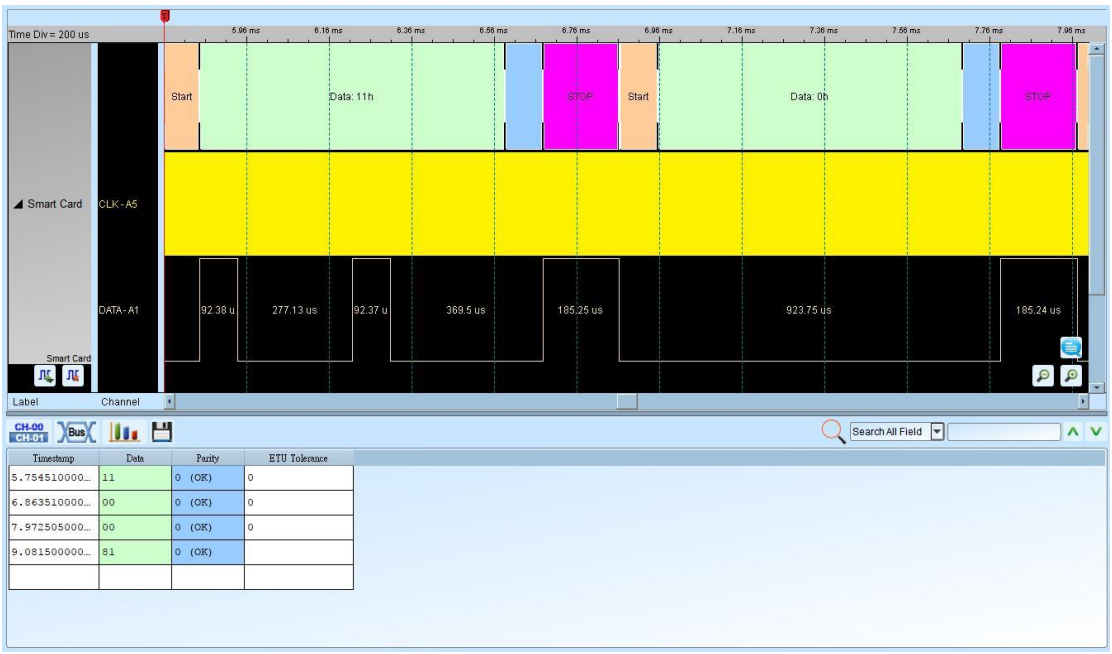
Settings



Channel: Show the selected channels (CLK and DATA) and the number of clocks within the bit (ETU).

Result

Click **OK** to run the Smart Card decode and see the result on the Waveform Window below.

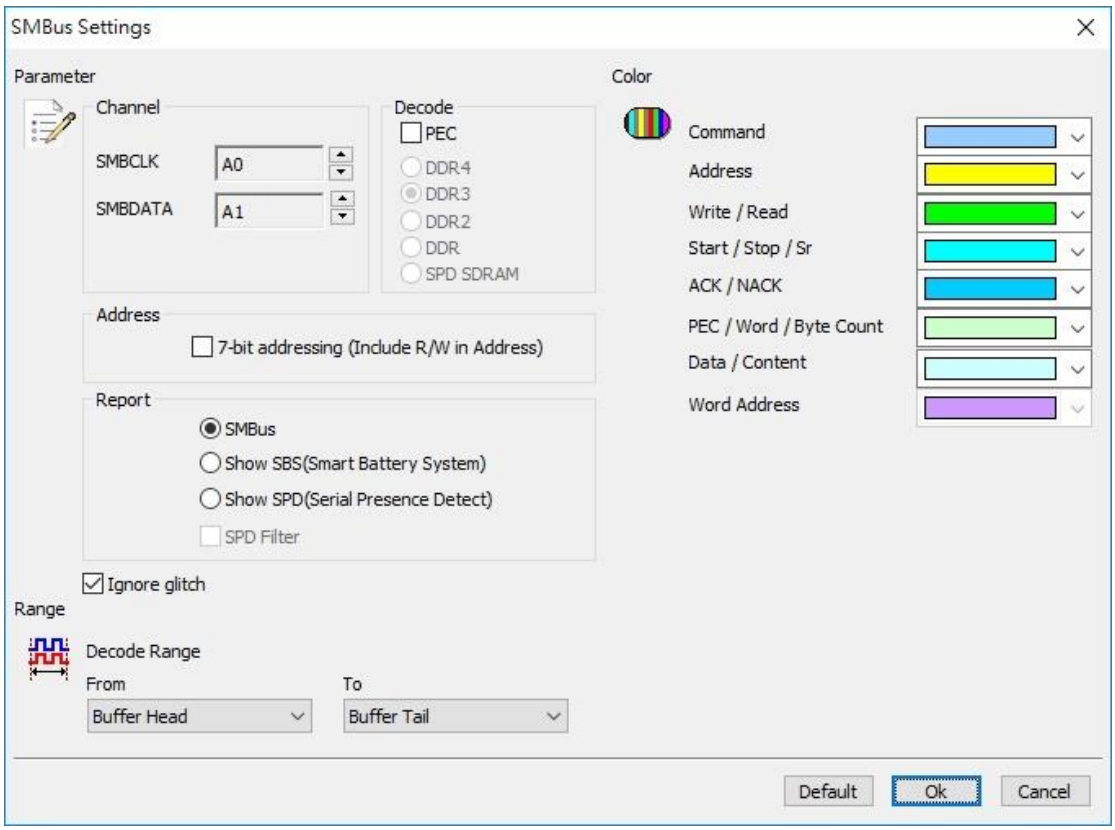


Timestamp	Data	Parity	ETU Tolerance
5.754510000...	11	0 (OK)	0
6.863510000...	00	0 (OK)	0
7.972505000...	00	0 (OK)	0
9.081500000...	81	0 (OK)	

System Management Bus (SMBus)

The SMBus (SMB) is a two-wire bus.

Settings



Clock: Show the selected channels (SMBCLK CH0 and SMBDATA CH1).

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit R/W).

Show SBS (Smart Battery System): Show the Smart Battery System: voltage, electric current and the manufacturer.

Show SPD(Serial Presence Detect)：Report window show the configuration of memory module(DDR3, DDR2, DDR, SPD SDRAM) in EEPROM.

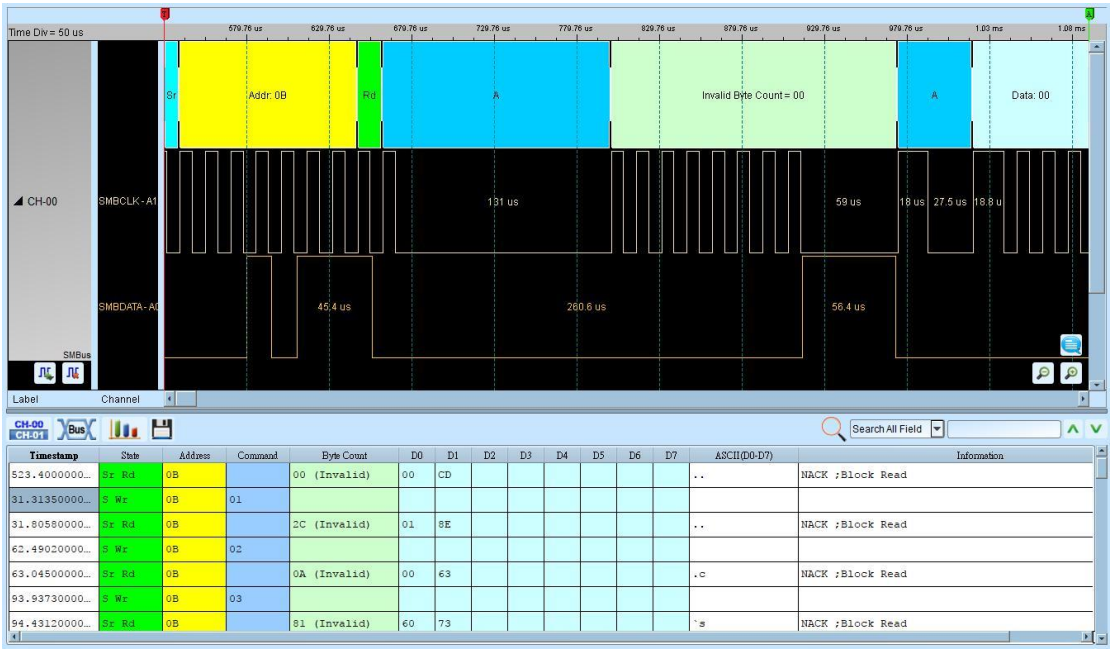
SBS/SPD Filter: Report window only show SBS/SPD packet.

Ignore glitch: Ignore the glitch when the slow transitions.

Result

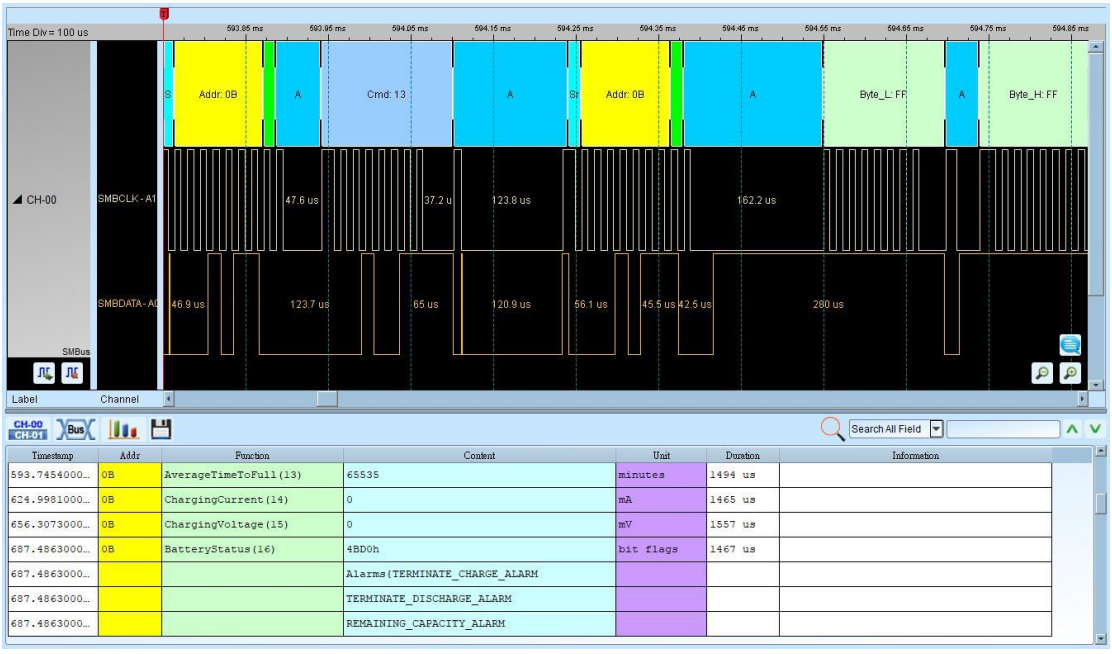
Click **OK** to run the SMBus Decode and see the result on the Waveform Window below.

SMBus



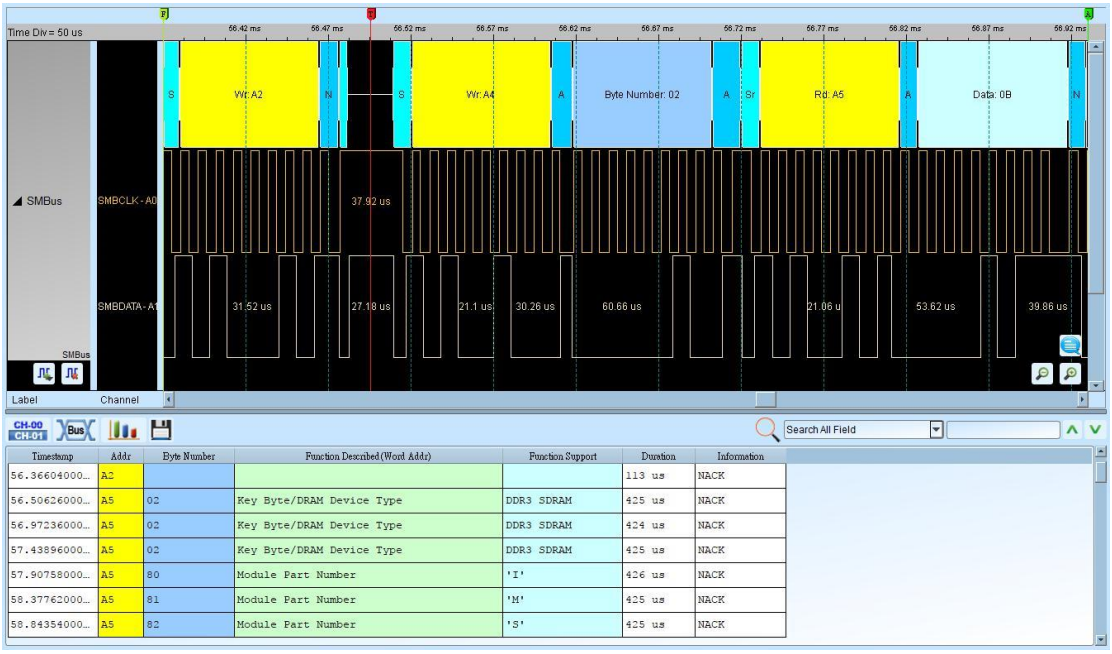
Timestamp	State	Address	Command	Byte Count	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Information
523.4000000...	Sr Rd	0B		00 (Invalid)	00	CD							..	NACK ;Block Read
31.31350000...	S Wr	0B	01											
31.80580000...	Sr Rd	0B		2C (Invalid)	01	8E							..	NACK ;Block Read
62.49020000...	S Wr	0B	02											
63.04500000...	Sr Rd	0B		0A (Invalid)	00	63							.c	NACK ;Block Read
93.93730000...	S Wr	0B	03											
94.43120000...	Sr Rd	0B		81 (Invalid)	60	73							`s	NACK ;Block Read

Show SBS (Smart Battery System)



Timestamp	Addr	Function	Content	Unit	Duration	Information
593.7454000...	0B	AverageTimeToFull(13)	65535	minutes	1494 us	
624.9981000...	0B	ChargingCurrent(14)	0	mA	1465 us	
656.3073000...	0B	ChargingVoltage(15)	0	mV	1557 us	
687.4863000...	0B	BatteryStatus(16)	4BD0h	bit flags	1467 us	
687.4863000...			Alarms(TERMINATE_CHARGE_ALARM			
687.4863000...			TERMINATE_DISCHARGE_ALARM			
687.4863000...			REMAINING_CAPACITY_ALARM			

Show SPD (Serial Presence Detect)

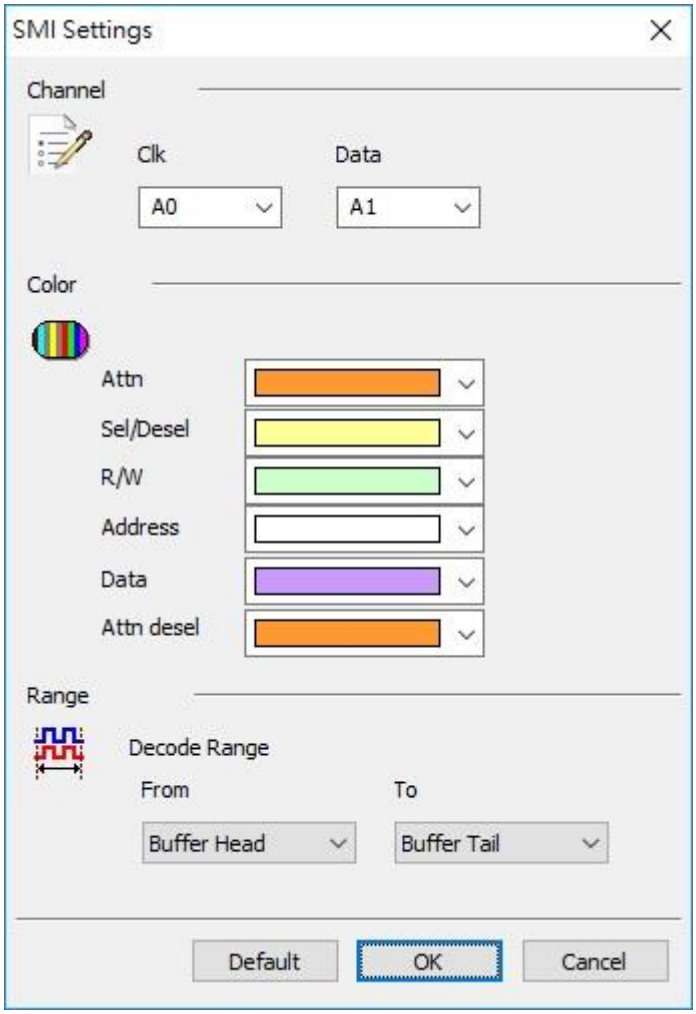


Timestamp	Addr	Byte Number	Function Described (Word Addr)	Function Support	Duration	Information
56.36604000...	A2				113 us	NACK
56.50626000...	A5	02	Key Byte/DRAM Device Type	DDR3 SDRAM	425 us	NACK
56.97236000...	A5	02	Key Byte/DRAM Device Type	DDR3 SDRAM	424 us	NACK
57.43896000...	A5	02	Key Byte/DRAM Device Type	DDR3 SDRAM	425 us	NACK
57.90758000...	A5	80	Module Part Number	'I'	426 us	NACK
58.37762000...	A5	81	Module Part Number	'M'	425 us	NACK
58.84354000...	A5	82	Module Part Number	'S'	425 us	NACK

Serial Microprocessor Interface (SMI)

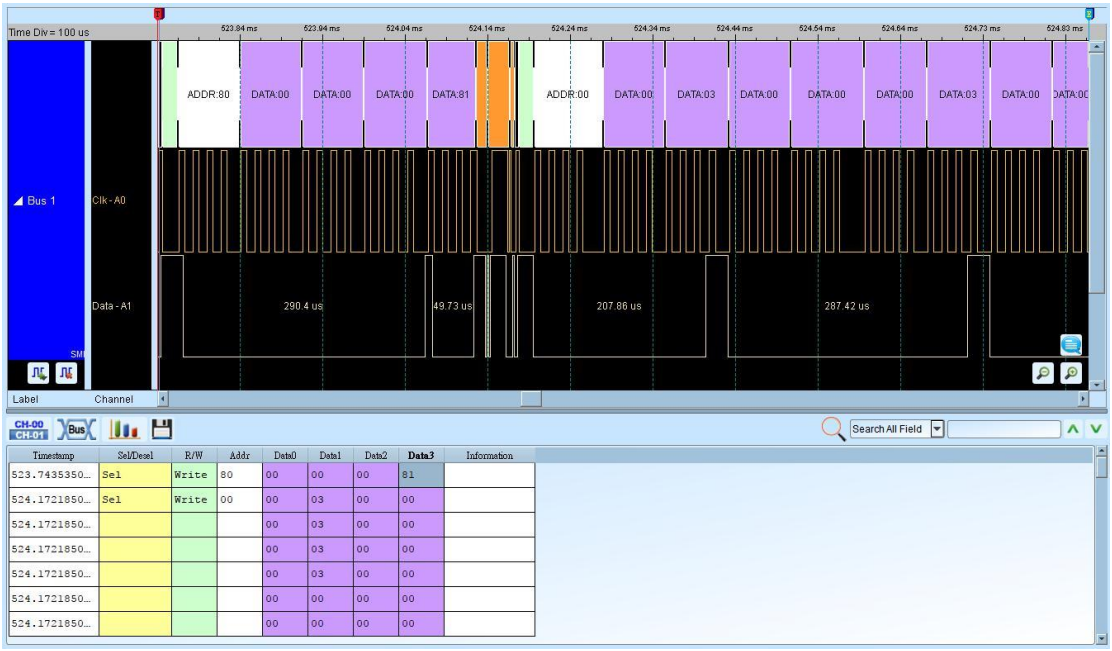
The SMI is a two-wire bus.

Settings



Channel: Show the selected channels (Clk and Data)

Result



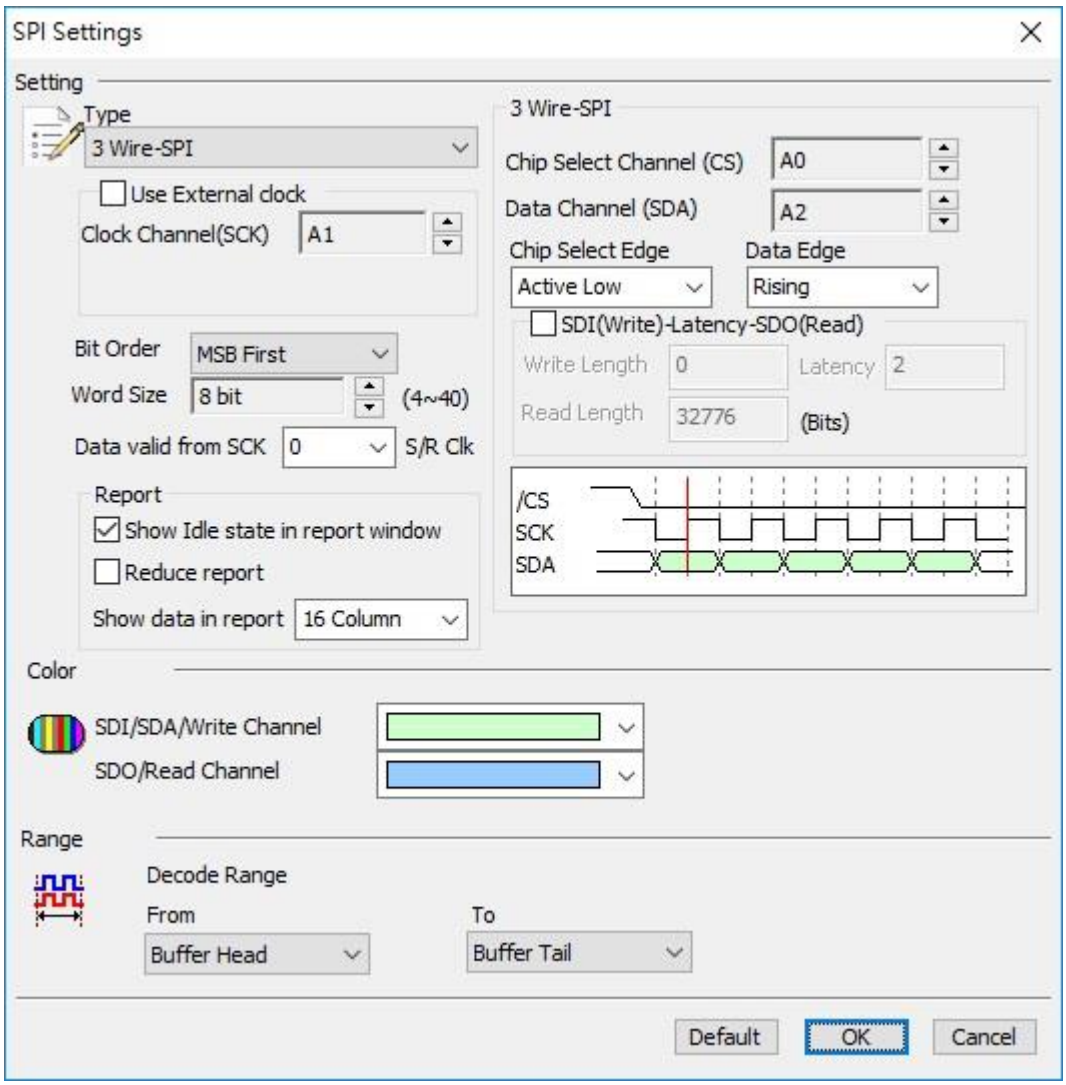
Timestamp	Sel/Desel	R/W	Addr	Data0	Data1	Data2	Data3	Information
523.7435350...	Sel	Write	80	00	00	00	81	
524.1721850...	Sel	Write	00	00	03	00	00	
524.1721850...				00	03	00	00	
524.1721850...				00	03	00	00	
524.1721850...				00	03	00	00	
524.1721850...				00	00	00	00	
524.1721850...				00	00	00	00	

Serial Peripheral Interface (SPI)

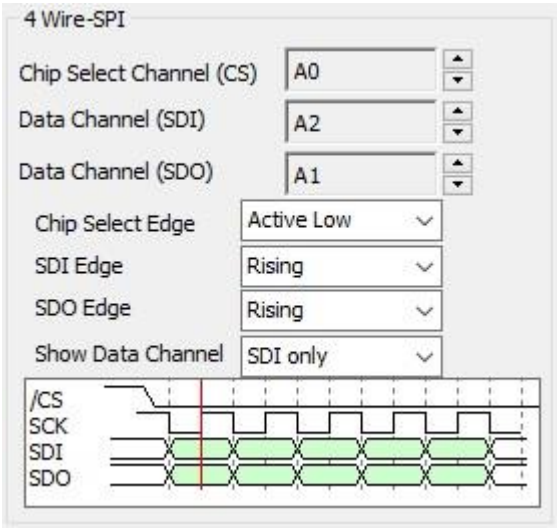
The SPI, is one kind of 4-wires synchronous serial data link. The SPI bus can be 4 wires, 3 wires, or 2 wires.

Settings

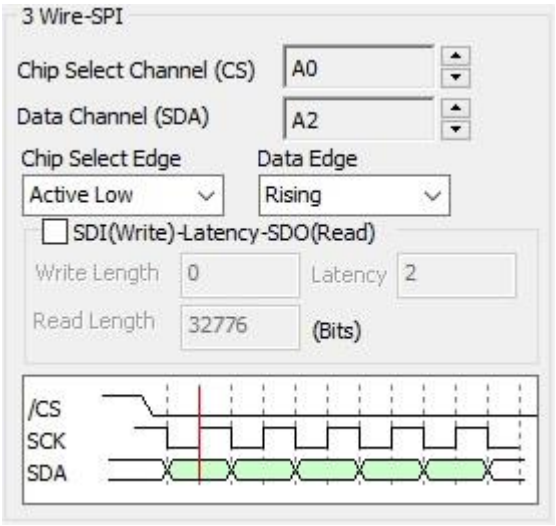
Type: The default is 3 Wire-SPI.



4 Wire-SPI dialog box ➔CS, SCK, SDI, SDO

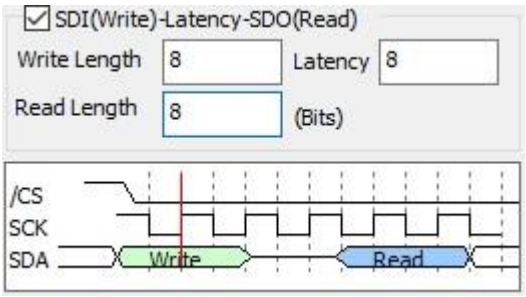


3 Wire-SPI dialog box ➔ CS, SCK, SDA

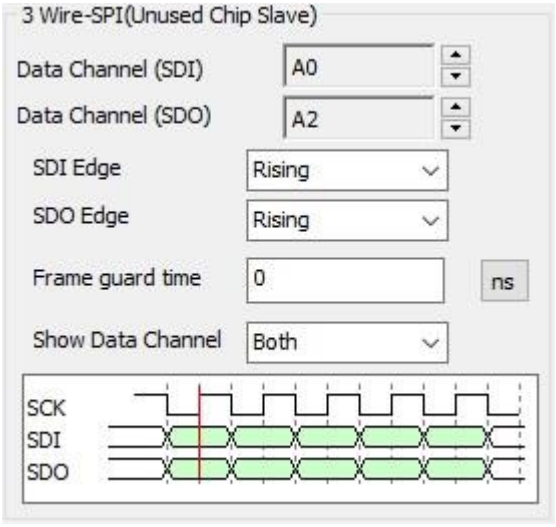


Click the SDI(Write)-Latency-SDO(Read) to show the dialog below.

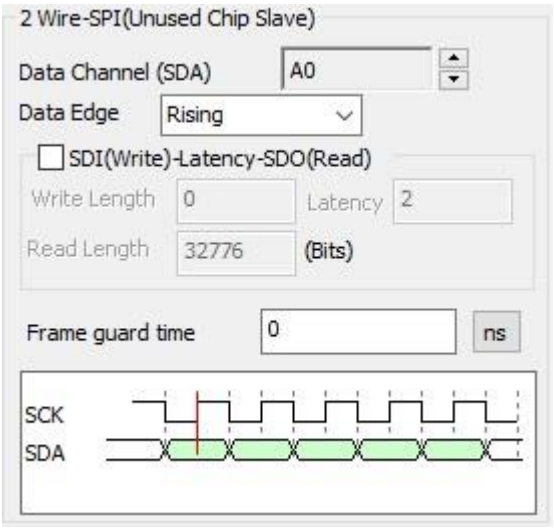
The maximum length is 65535 (Bits)



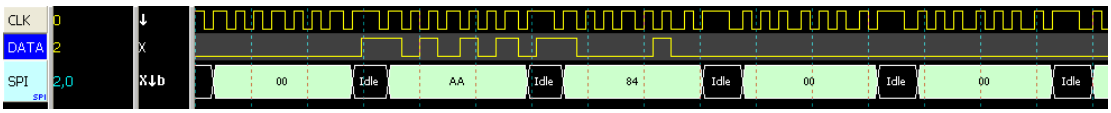
3 Wire-SPI (Unused Chip Slave) dialog box ➔ SCK, SDI, SDO

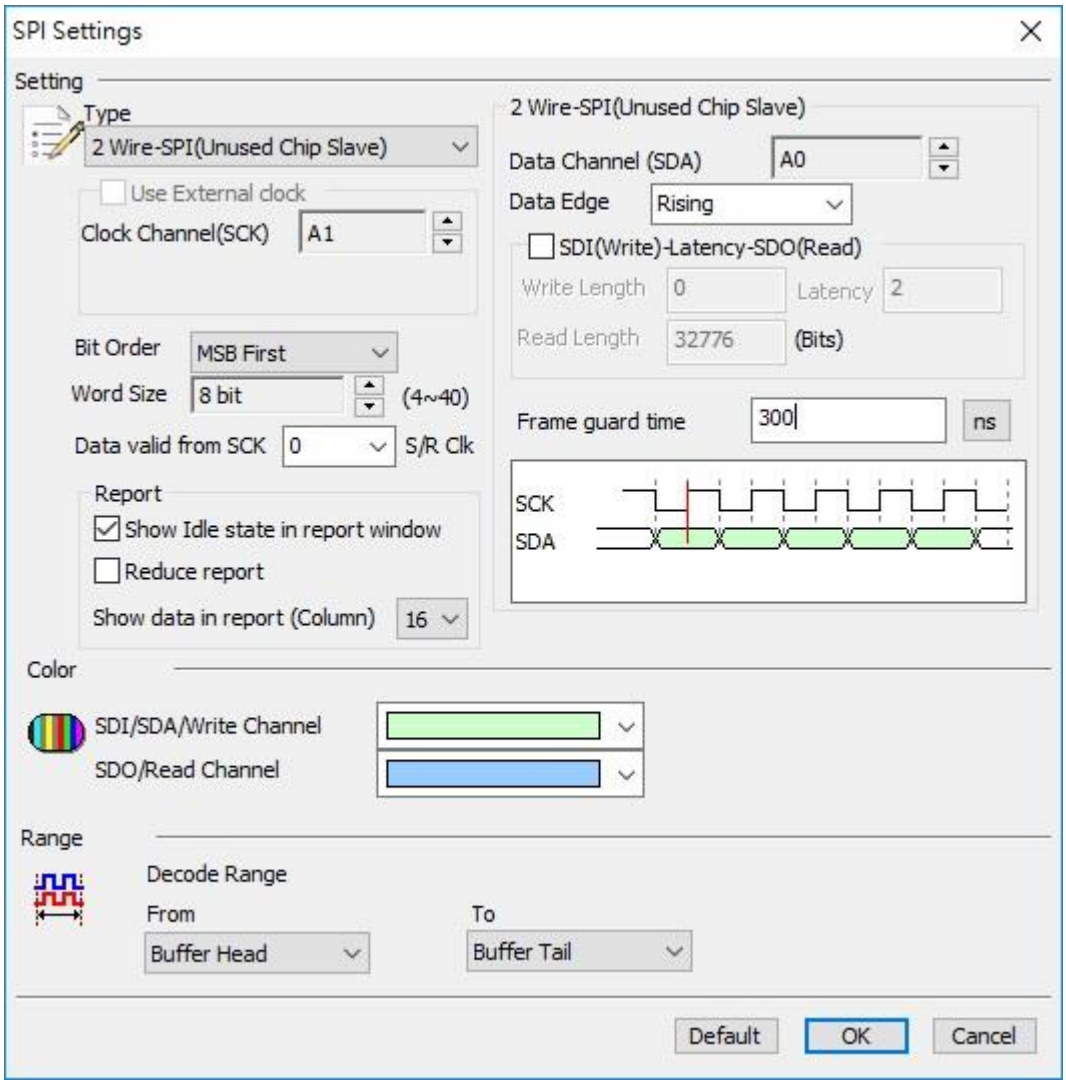


2 Wire-SPI (Unused Chip Slave) dialog box ➔ SCK, SDA

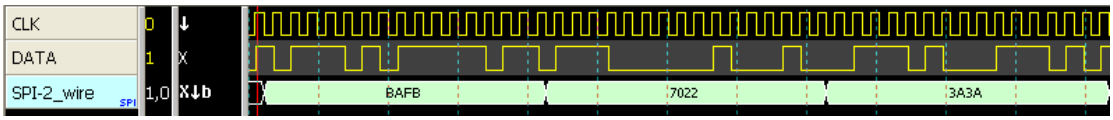


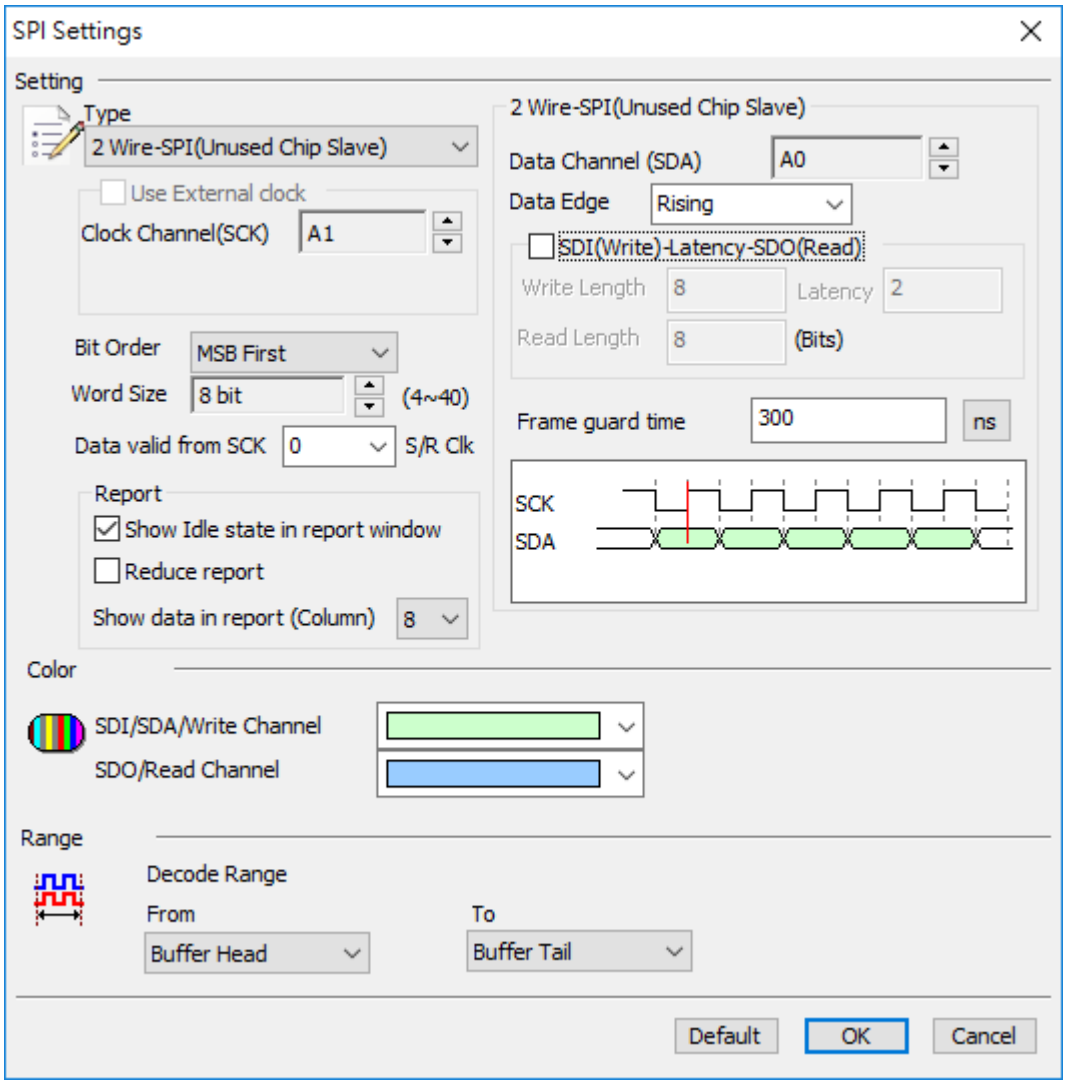
If the chip slave is not used and the interval between frames is not 0. You can set the interval as 6us, any data bit higher than 6us will be seen as Idle.



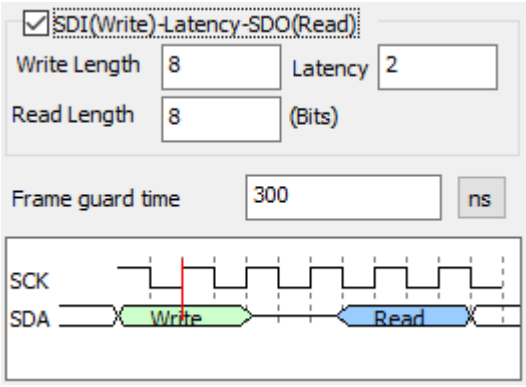


If the chip slave is not used and the interval between frames is 0. You can see the data continuous as the dialog below.





We also offer bi-direction mode as the dialog below.



C heck the SDI(Write)-Latency-SDO(Read)to set the bit numbers for the 3 columns;

Write and Read (1~65535), Latency (0~65535).

Bit Order: MSB first or LSB first.

Word size: Default is 8 bits, minimum is 4 and maximum is 32.

Report: Show Idle state in report window, You can disable this default for not to display the idle state on the Report Window.

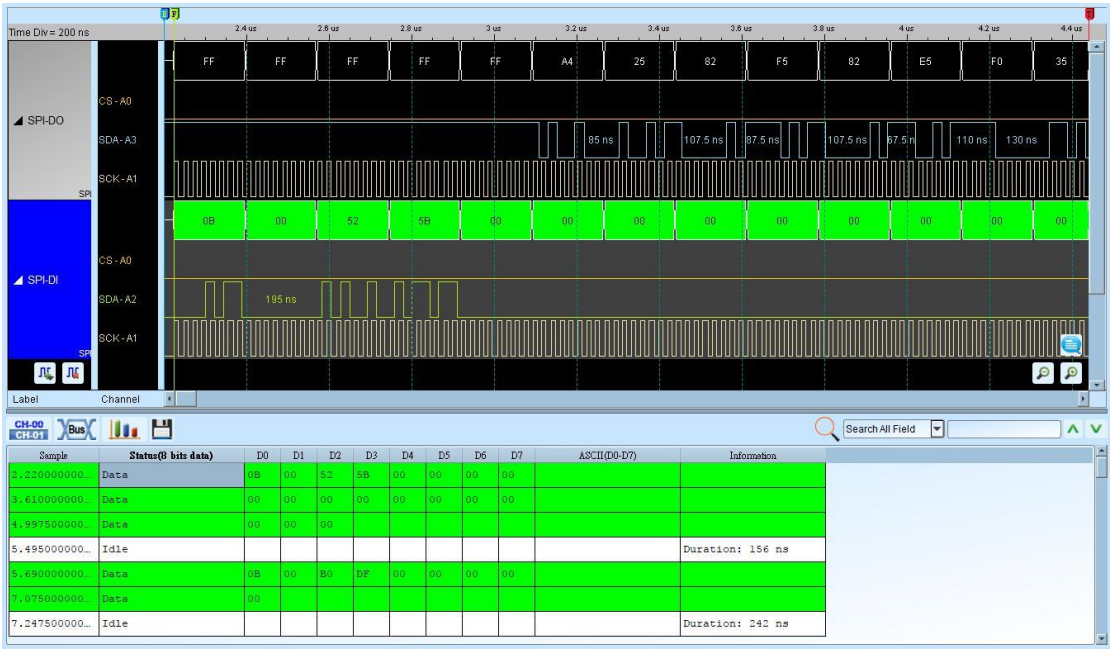
Show data in report: Display the ASCII code with default 16 columns on the Report Window.

Data Valid from SCK: In some SPI devices, the data is not valid right after the data output or the clock edge. You can set the data valid after 0-3 units of the sampling rate in Data valid from SCK; if the unit is 1 and the sampling rate is 200MHz, the delay time is 5 ns.

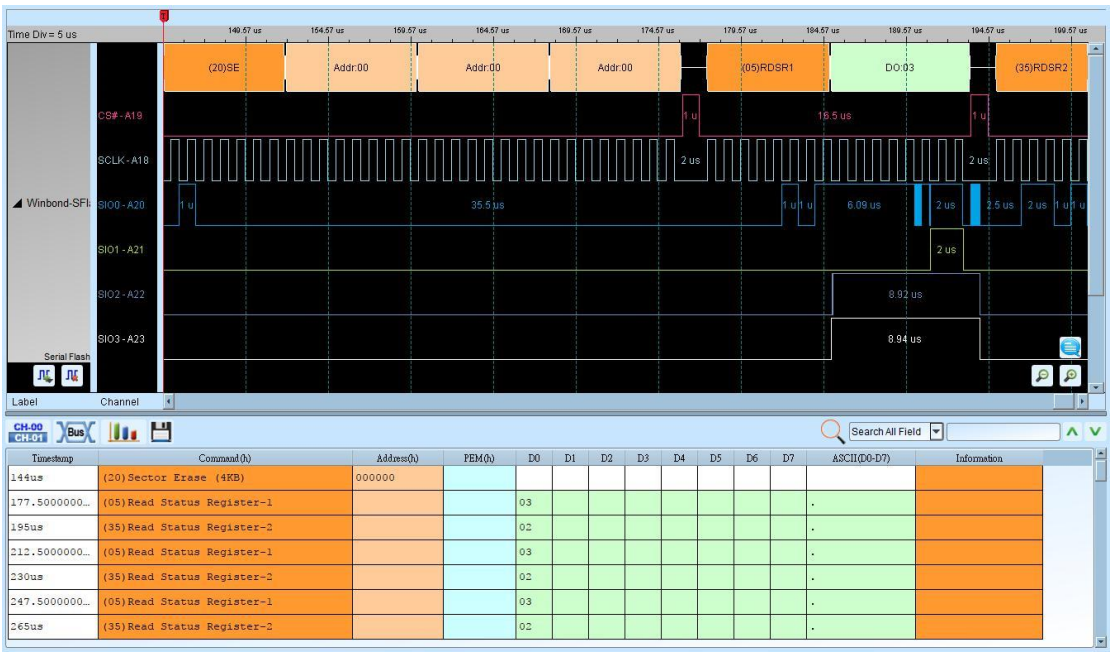
Result

Click **OK** to run the SPI decode and see the result on the Waveform Window below.

3-Wire SPI, Internal clock mode



3-Wire SPI, External clock mode

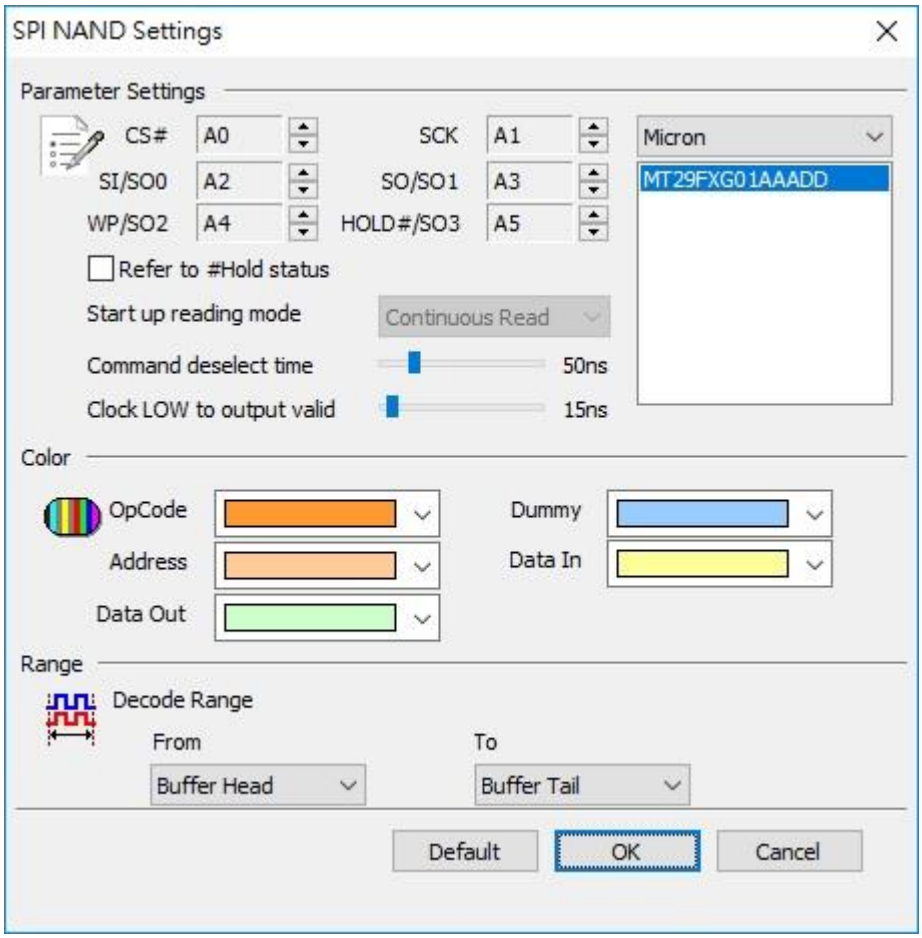


Timestamp	Command(h)	Address(h)	PEM(h)	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Information
144us	(20)Sector Erase (4KB)	000000											
177.5000000...	(05)Read Status Register-1			03								.	
195us	(35)Read Status Register-2			02								.	
212.5000000...	(05)Read Status Register-1			03								.	
230us	(35)Read Status Register-2			02								.	
247.5000000...	(05)Read Status Register-1			03								.	
265us	(35)Read Status Register-2			02								.	

Serial Peripheral Interface NAND (SPI NAND)

SPI NAND Flash is a SPI/QPI interfaced NAND flash memory. The decoder translates the bus signal to command/address/data field to provide an easier way to exam the SPI NAND waveform.

Settings



CS#: Chip select

SCLK: Clock

SIO0 – SIO3: Data

Start up reading mode: The initial setting of the reading mode for the decoder.

Command deselect time: The minimum required time for #CS deselecting. Clock

LOW to output valid: The data probe time after clock falling.

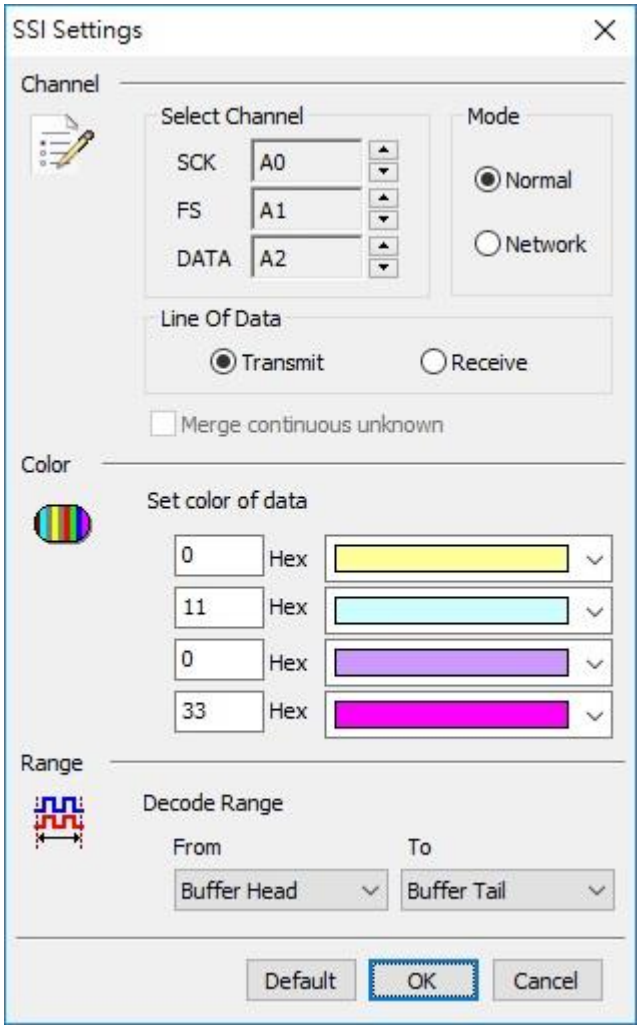
Result

Sample	Op Code	Address	D0	D1	D2	D3	D4	D5	D6	D7	ASCII	Memo
337.3600000…	READ FROM CACHE x4(6B)	0800	33								3	
342.6000000…	PAGE READ(13)	000040										
350us	GET FEATURE(0F)	C0	01								.	Duration: 163.159 …
678.4800000…			00								.	
681.0200000…	READ FROM CACHE x4(6B)	1800	33								3	
686.2400000…	PAGE READ(13)	000080										
693.6400000…	GET FEATURE(0F)	C0	01								.	Duration: 163.159 …

SSI

The Synchronous Serial Interface (SSI) protocol has four kinds of signals: Serial Clock (SCK), Transmit Data, Receive Data and Transmit/Receive Frame Synchronous (FS). The SSI protocol supports either the Normal or Network mode that is independent of whether the transmitter and the receiver are synchronous or asynchronous.

Settings



Select Channel: Show the selected channels.

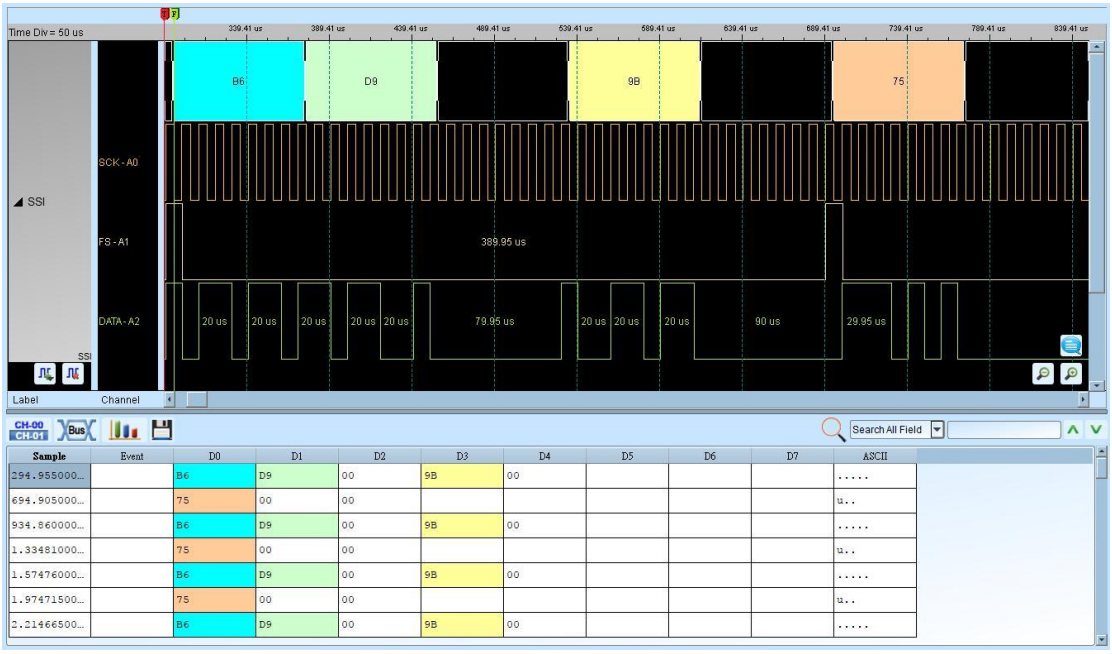
Mode: Normal or Network.

Line Of Data: Transmit or Receive.

Merge continuous unknown: Combine the unknown data only in Network mode.

Result

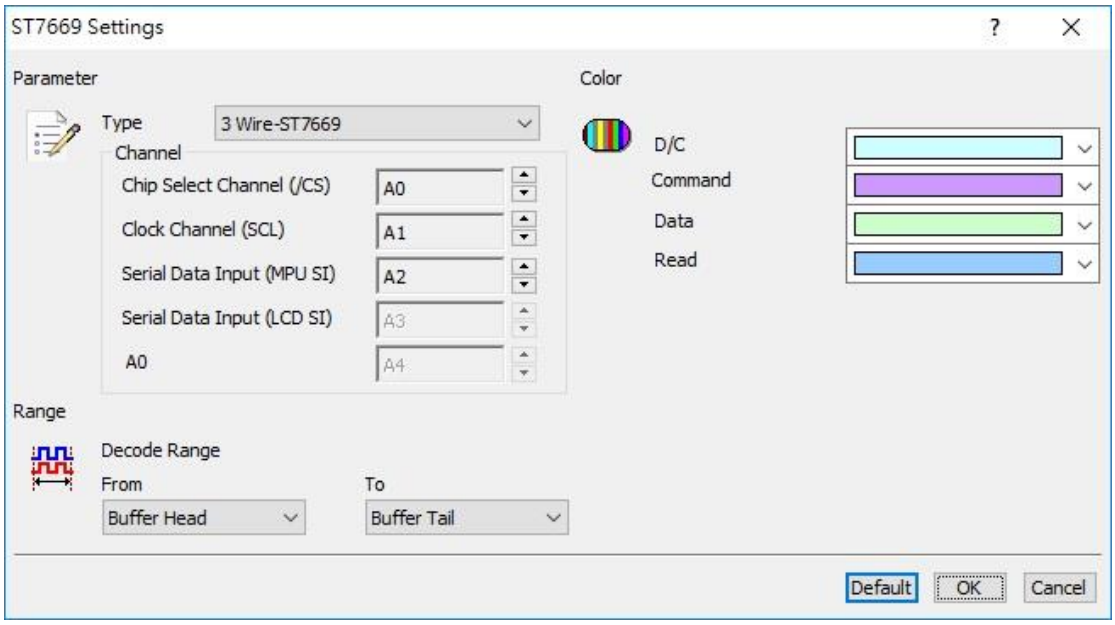
Click **OK** to run SSI decode and see the result on the Report Window below.



ST7669

ST76669 was developed by Sitronix to interface with the LCD module.

Settings



Channel: Show the selected channels.

Result

Click **OK** to run the LCD1602 decode and see the result on the Waveform Window below.

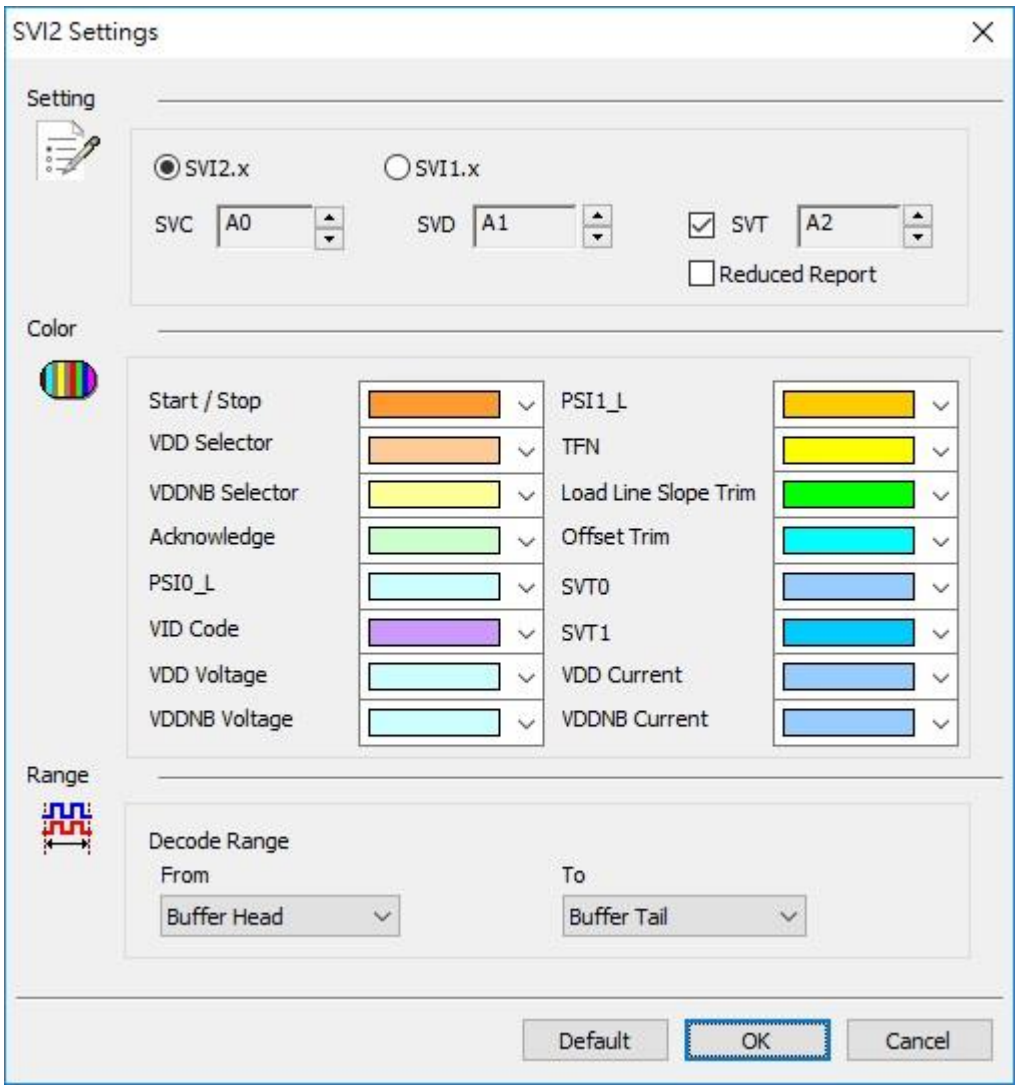
Timestamp	D/C	Data or Parameter/Command	ID Data(Read)	ASCII
83.47000000...	0x01 (Data or Paramete...	03		.
101.4600000...	0x00 (Command)	44		D
119.4600000...	0x01 (Data or Paramete...	05		.
217.4900000...	0x00 (Command)	21		!
233.4800000...	0x00 (Command)	23		#
251.4850000...	0x01 (Data or Paramete...	03		.
269.4800000...	0x00 (Command)	44		D

Serial VID Interface 2.0 (SVI2)

The SVI2 protocol is an interface for power management and developed by AMD.

The SVI2 working voltage is between 1V to 1.6V and its maximum frequency is at 20MHz with 3 bits： SVC/ SVD/ SVT.

Settings



SVC: SVI2 clock.

SVD: SVI2 data.

SVT: SVI2 telemetry data line. Telemetry will not be decoded if the SVT is not

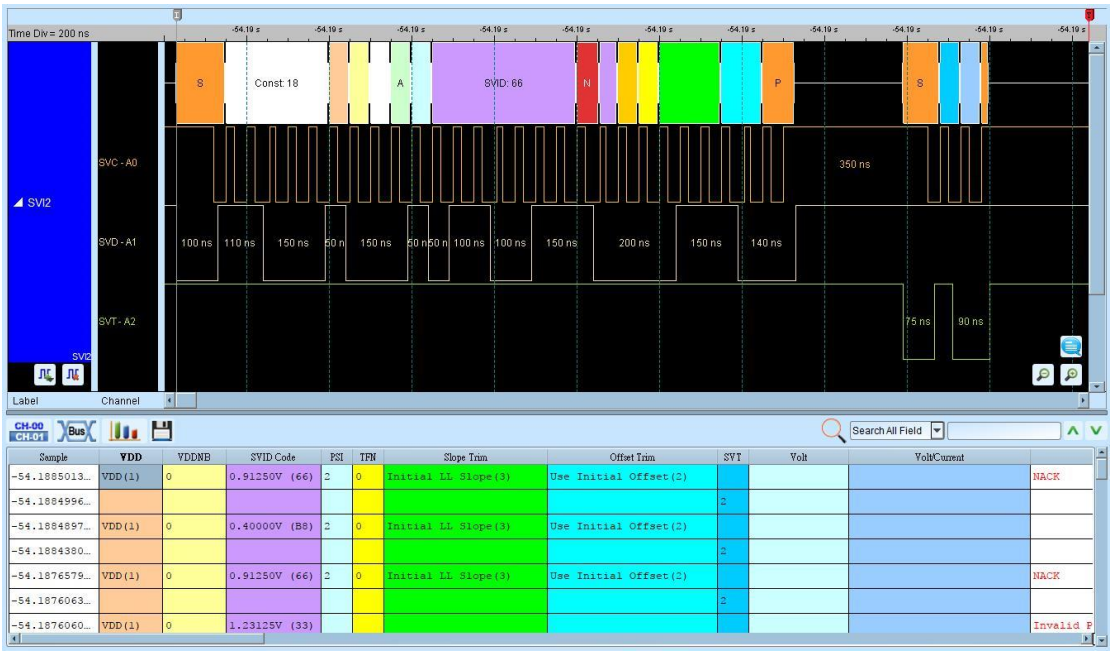
checked.

SVI2.x / SVI1.x: Select SVI2 / SVI protocol to decode.

Reduced Report: Only show SVD / VOTFC packet in the report window.

Result

Click **OK** to run the SVI2 decode and see the result on the Waveform Window below.



Serial VID (SVID) (Upon Request)

Serial VID (SVID) protocol is for power management and developed by Intel. SVID voltage is between 1.0V to 1.1V, maximum frequency at 26.25MHz and is 3 wires：SCLK/ SDATA/ ALERT.

Supported version:

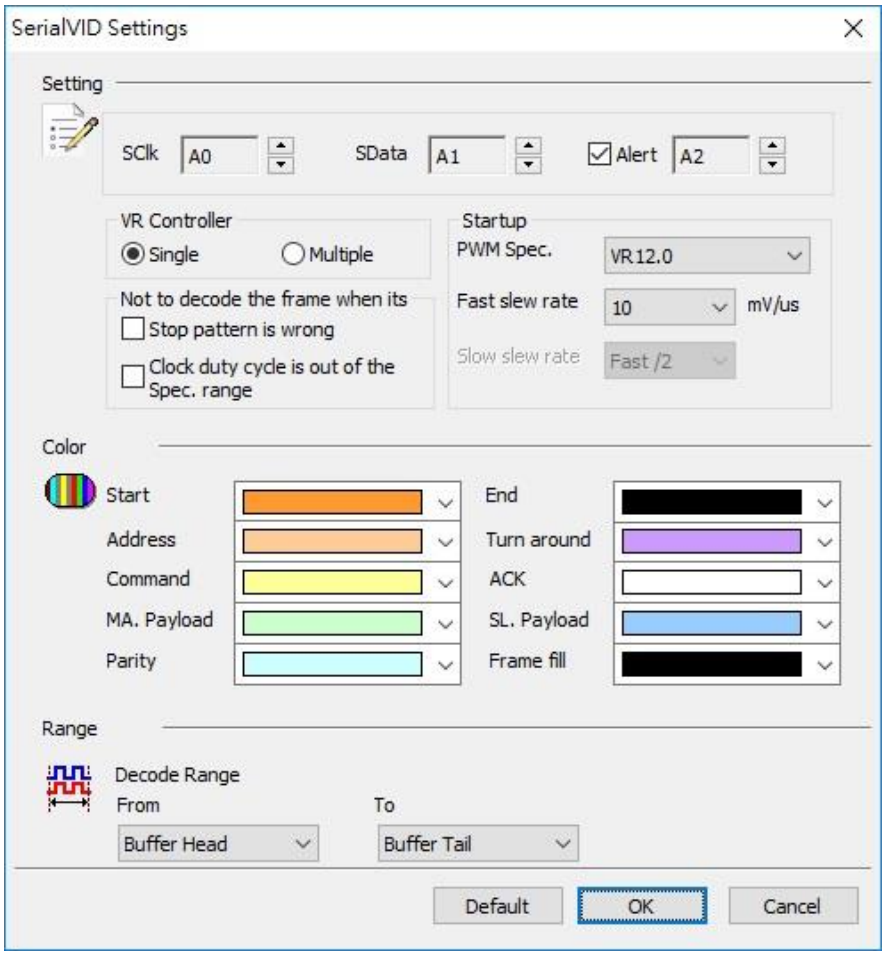
IMVP7/VR12, VR12.1, VR12.5, VR12.6

IMVP8/VR13

IMVP9/VR14

If you have any issues with SVID protocol features, please contact your Intel Field Representative.

Settings



SClk: SVID clock.

SData: SVID data.

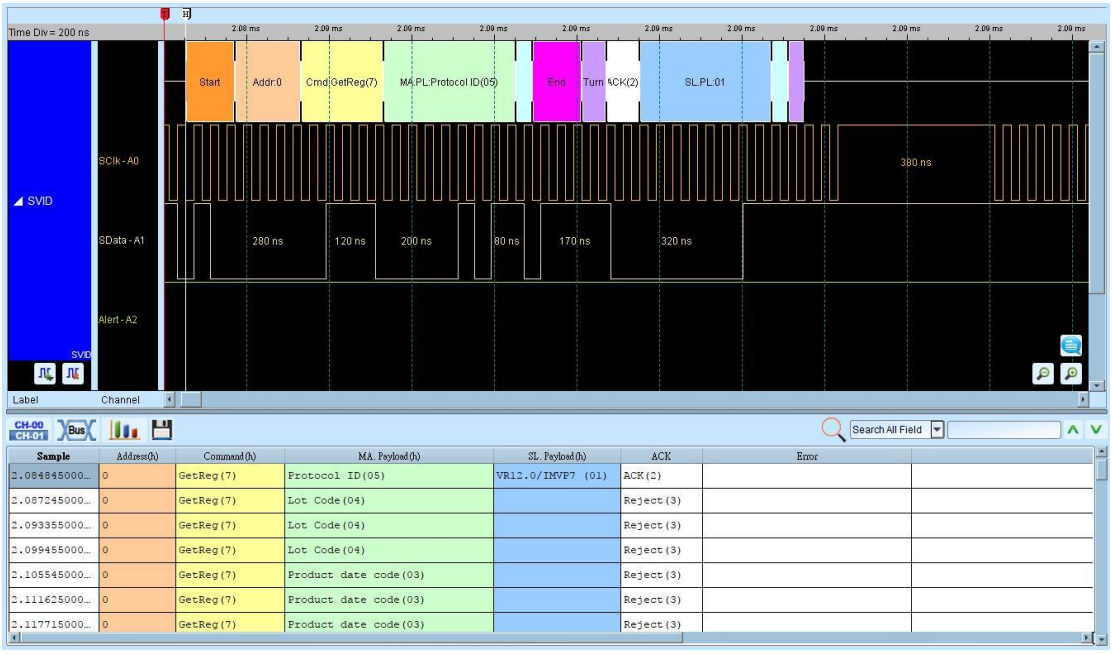
Alert: Alert, optional reminder.

VR Controller: Set single or multiple controllers in current VR. Set different address.

Not to decode the frame when its stop pattern wrong or clock duty cycle is out of range.

Result

Click OK to run the SVID decode and see the result on the Waveform Window below.

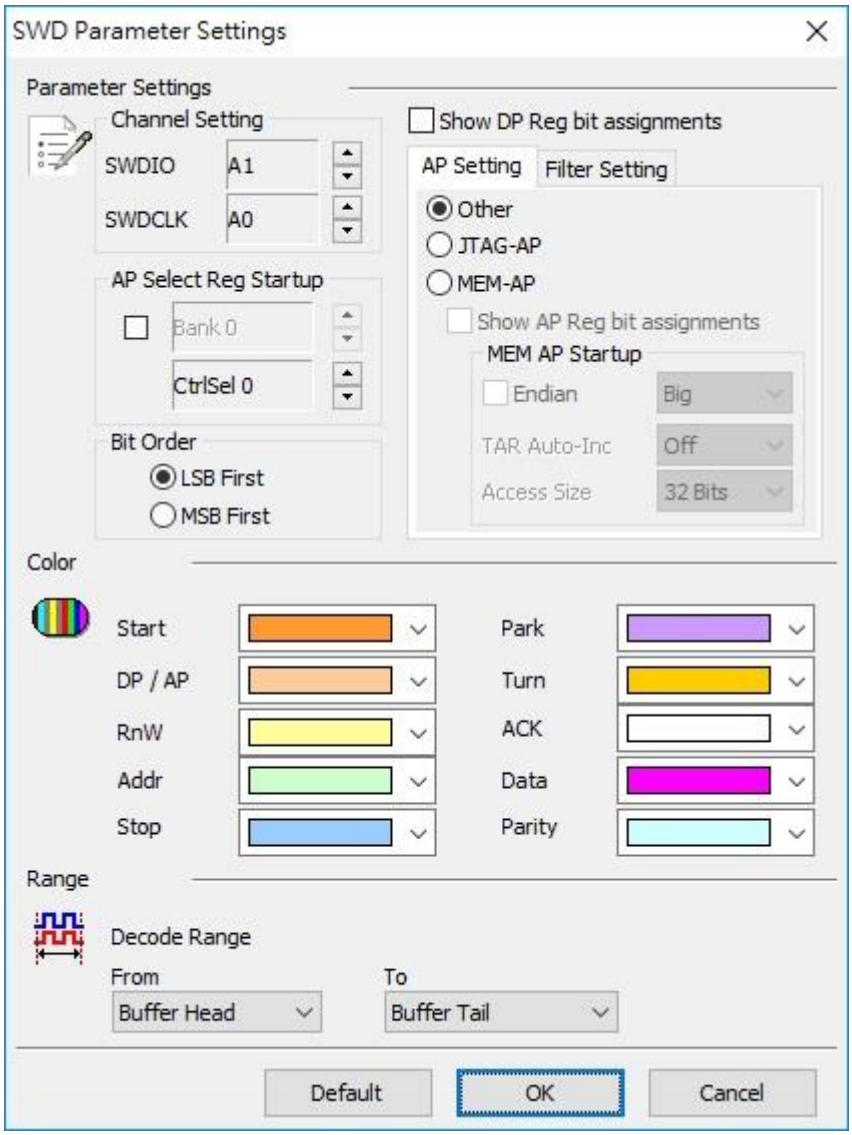


Sample	Address(h)	Command(h)	MA. Payload(h)	SL. Payload(h)	ACK	Error
2.084845000…	0	GetReg(7)	Protocol ID(05)	VR12.0/IMVP7 (01)	ACK(2)	
2.087245000…	0	GetReg(7)	Lot Code(04)		Reject(3)	
2.093355000…	0	GetReg(7)	Lot Code(04)		Reject(3)	
2.099455000…	0	GetReg(7)	Lot Code(04)		Reject(3)	
2.105545000…	0	GetReg(7)	Product date code(03)		Reject(3)	
2.111625000…	0	GetReg(7)	Product date code(03)		Reject(3)	
2.117715000…	0	GetReg(7)	Product date code(03)		Reject(3)	

Serial Wire Debug (SWD)

The SWD is a 2-pin electrical alternative JTAG interface that has the same JTAG protocol on top. It uses the existing GND connection. SWD uses an ARM CPU standard bi-directional wire protocol, defined in the ARM Debug Interface v5.

Settings

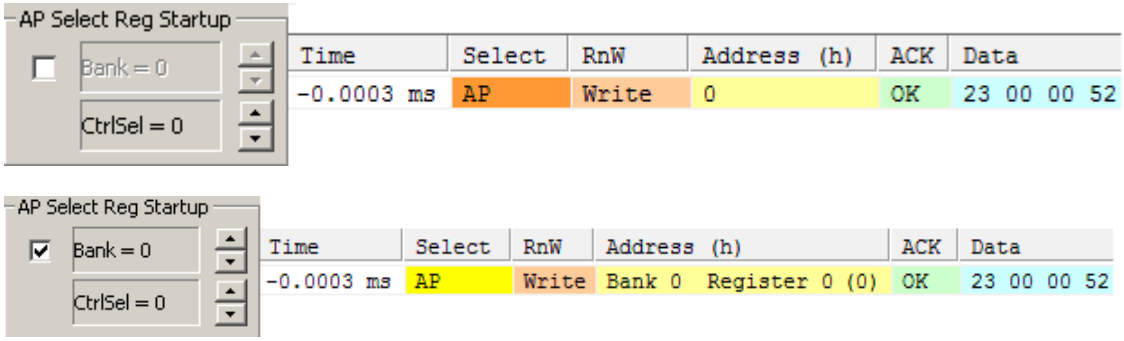


SWDIO: I/O data.

SWDCLK: Clock.

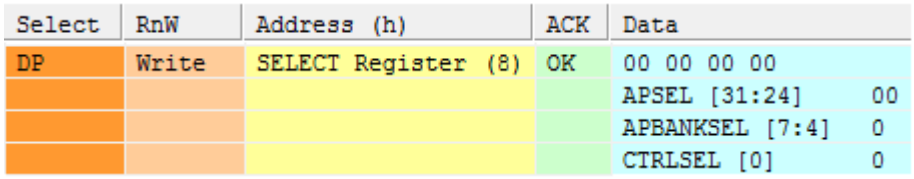
AP Select Reg Startup: When the AP Select Reg Startup is not assigned, only the

address information will be shown. You may input the Bank and Ctrl/Select initial values manually.



Bit Order: LSB or MSB.

Show DP Reg bit assignments: Show the DP register information.

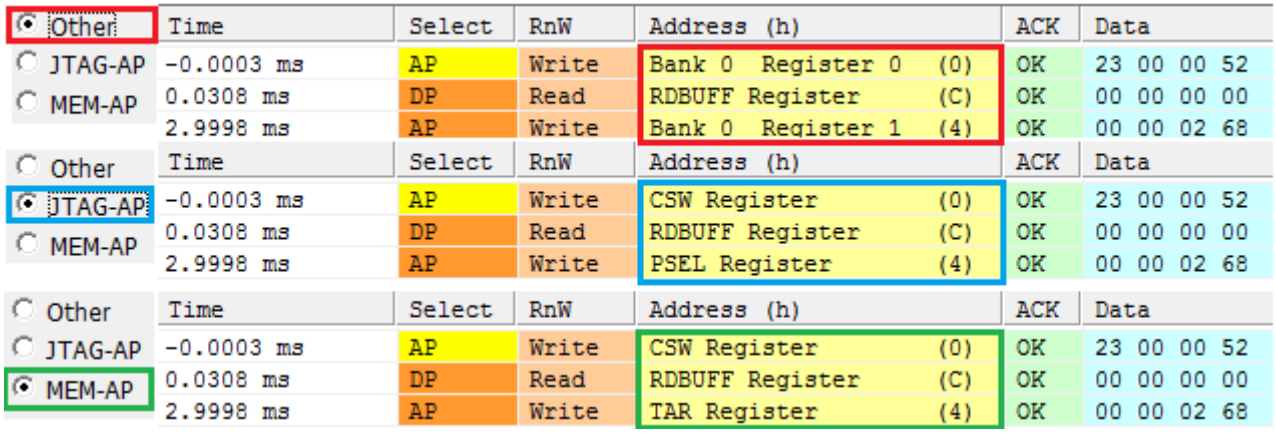


AP Setting:

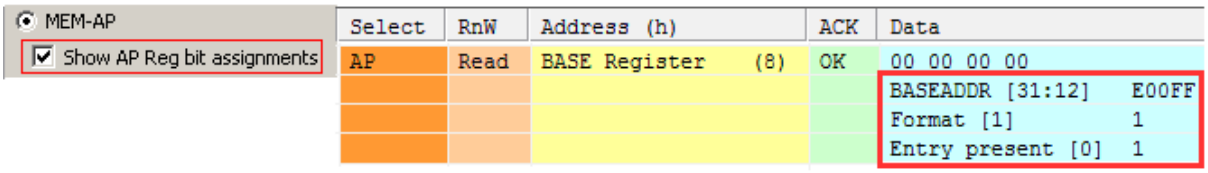
JTAG-AP: Show the JTAG AP decode.

MEM-AP: Show the MEM AP decode.

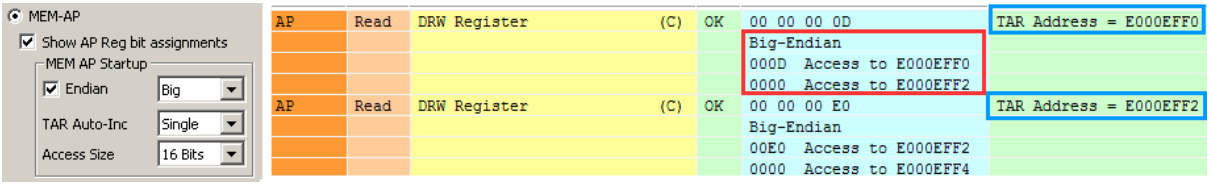
Other: Show Bank X Register X.



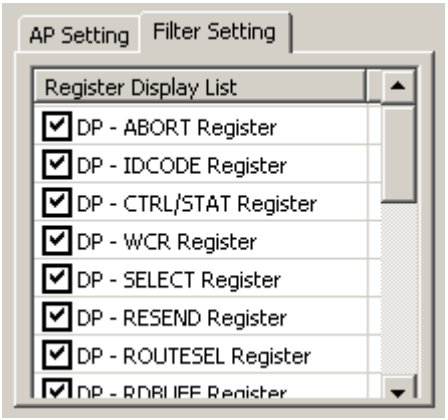
Show AP Reg bit assignments: Display the AP register information if JTAG-AP or MEM-AP checked.



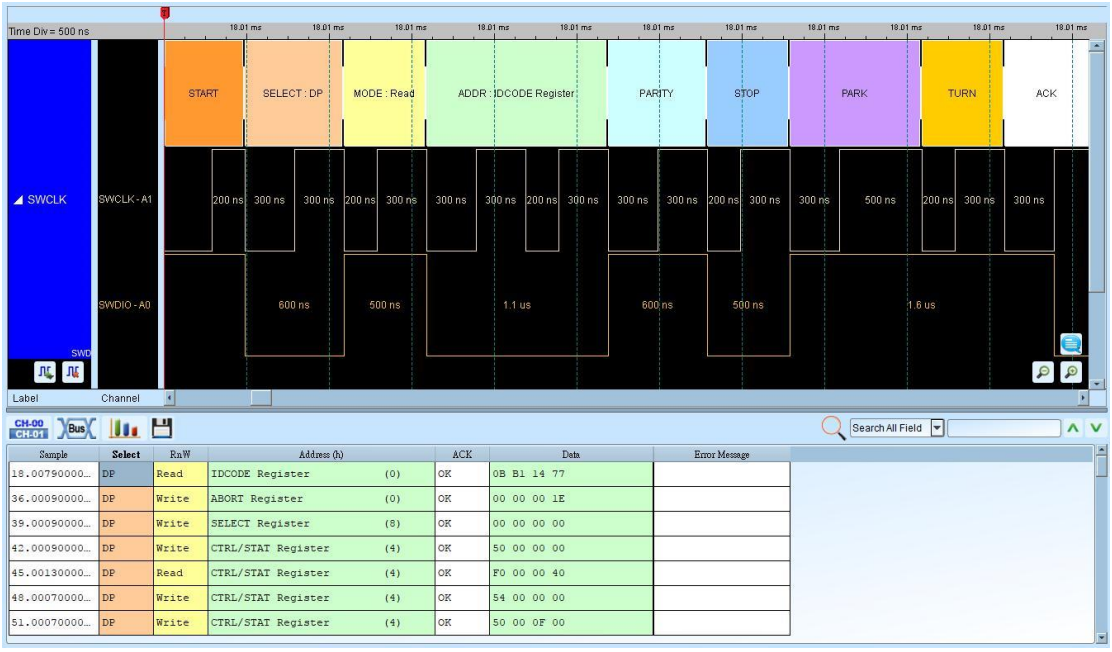
MEM AP Startup: Assign the initial MEM-AP value.



Filter Setting: Filter the unwanted Registers.



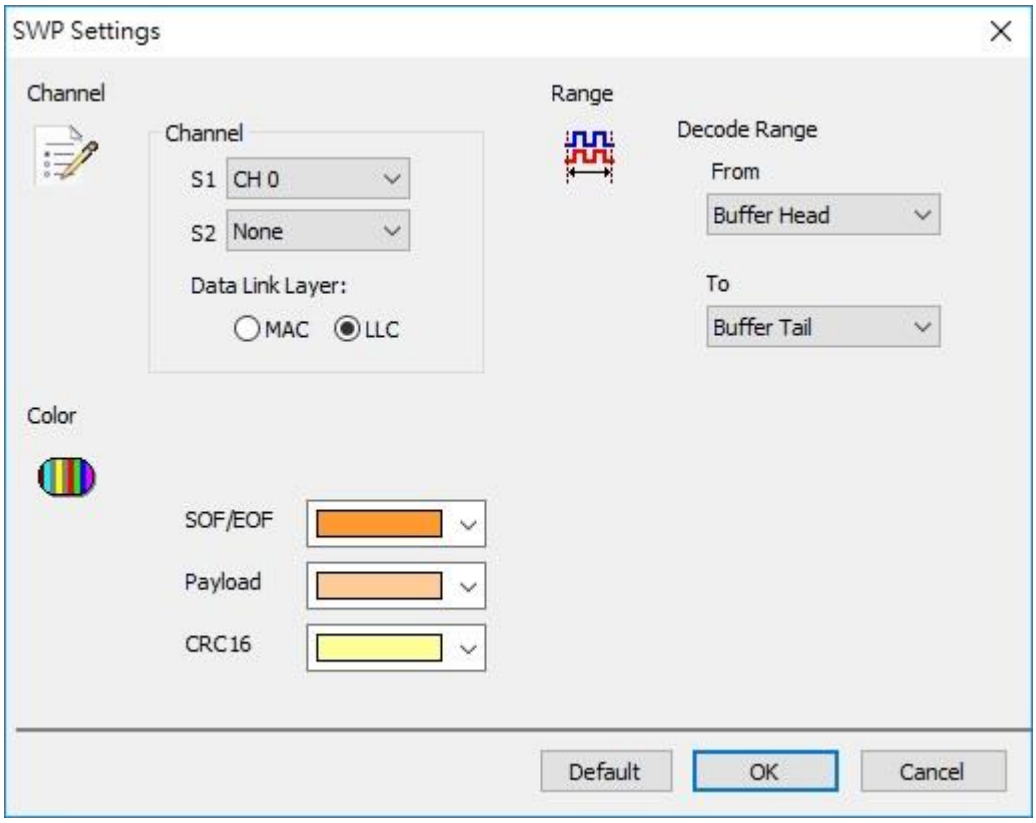
Result



SWP

The Single Wire Protocol (SWP) is a single-wire connection between the SIM card and a NFC chip in a cell phone.

Settings

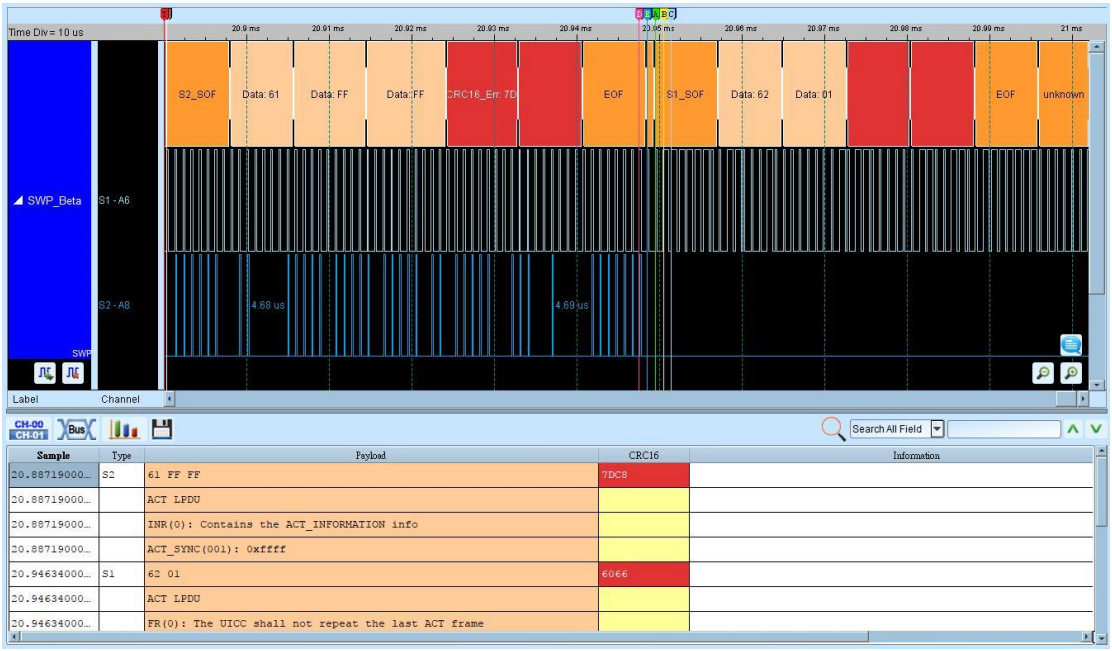


S1: I/O data.

S2: I/O data in current domain and it need convert to voltage domain.

Data Link Layer: Supported MAC and LLC layers

Result

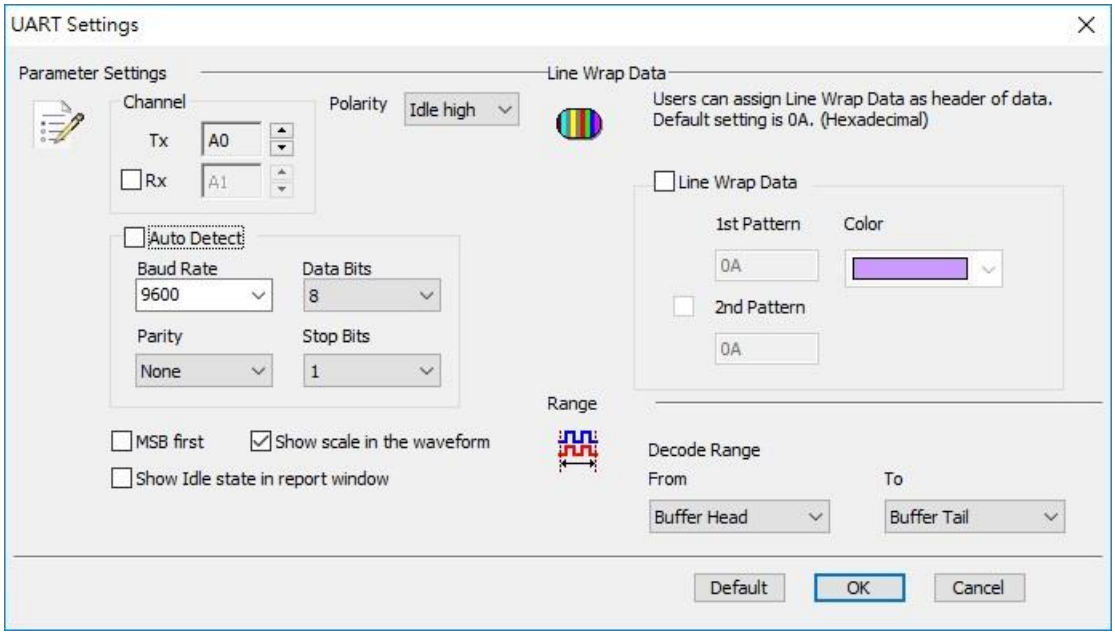


Sample	Type	Payload	CRC16	Information
20.88719000...	S2	61 FF FF	7DC8	
20.88719000...		ACT LPDU		
20.88719000...		INR(0): Contains the ACT_INFORMATION info		
20.88719000...		ACT_SYNC(001): 0xffff		
20.94634000...	S1	62 01	6066	
20.94634000...		ACT LPDU		
20.94634000...		FR(0): The UICC shall not repeat the last ACT frame		

Universal Asynchronous Receiver/Transmitter (UART)

The UART (RS-232 or RS-485) protocol has two message types: Transmitter (TX) and Receiver (RX); you can measure the UART protocol in one signal or two signals. RS-485 need convert to logic signal, because LA can not capture differential signal.

Settings



Data: Show the selected channel (CH0).

Rx: Show Rx data in report window.

Auto: Shows High or Low when auto detection Idle.

Idle high: Idle condition shows High.

Idle low: Idle condition shows Low.

Auto Detect: Set the Baud Rate manually if not selected.

Baud Rate: Data rate (bits per second), and the range is 110 ~ 2M (bps).

Protocol: (Parity - Data Bits - Stop Bits)

Parity: N (None), O (Odd), or E (Even).

Data Bits: 5 to 10 bits.

Stop Bits: 1 to 2 bits.

MSB first: The default is LSB first; click it to change to MSB first.

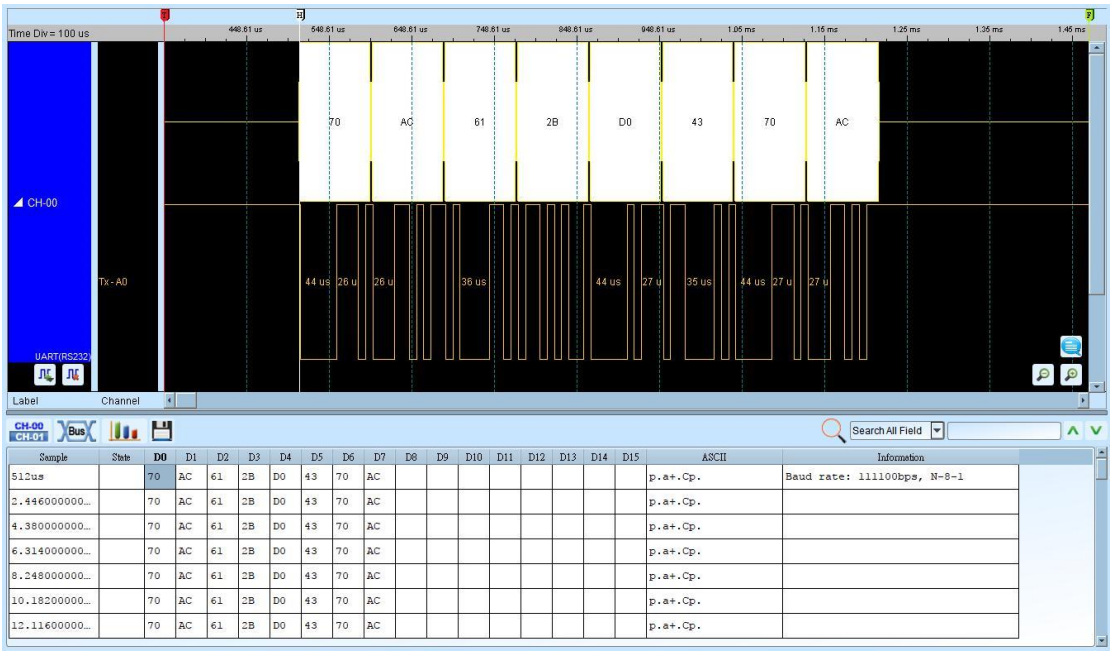
Report Unknown and Idle: Display the unknown and idle data in the Report Window.

Show scale in the waveform: Display the waveforms with scales.

Line Wrap Data: Use 1-2 value (hex) as header of data.

Result

Click **OK** to run UART Decode and see result on the Waveform Window below.

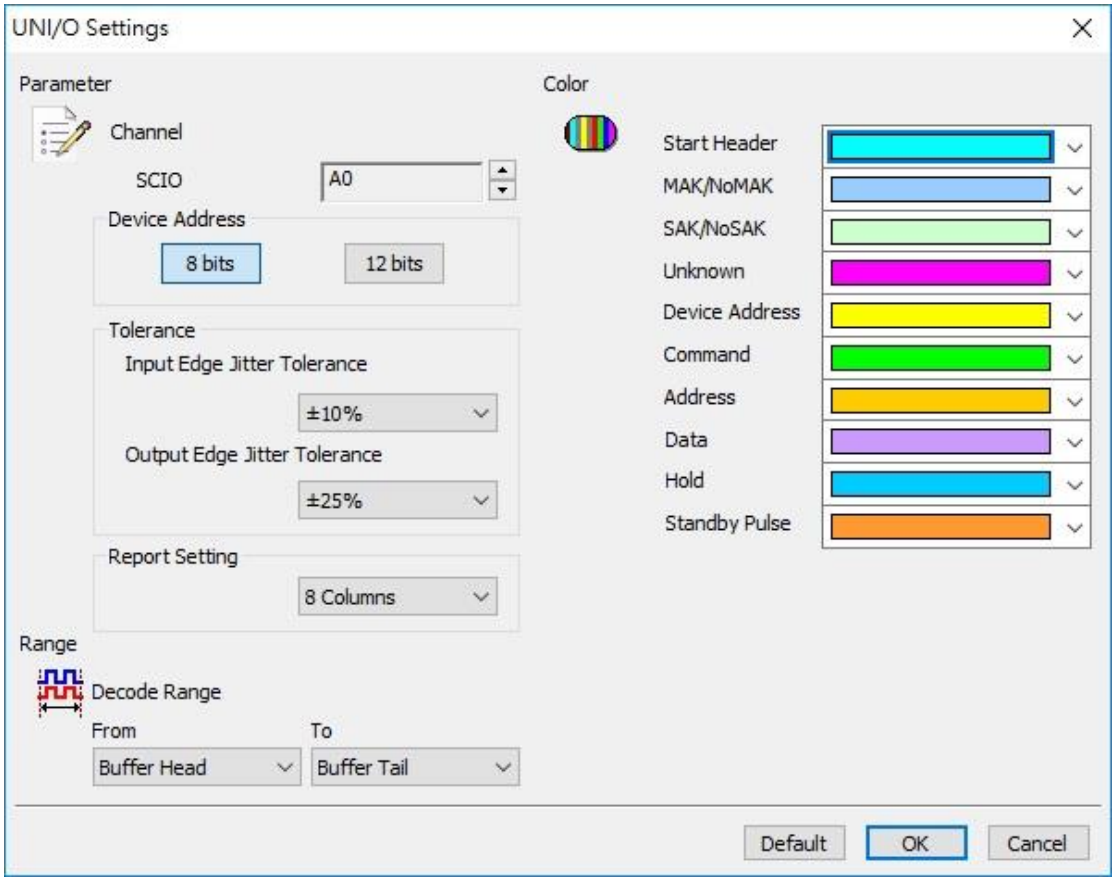


Sample	State	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	ASCII	Information
512us		70	AC	61	2B	D0	43	70	AC									p.a+.Cp.	Baud rate: 111100bps, N-8-1
2.446000000...		70	AC	61	2B	D0	43	70	AC									p.a+.Cp.	
4.380000000...		70	AC	61	2B	D0	43	70	AC									p.a+.Cp.	
6.314000000...		70	AC	61	2B	D0	43	70	AC									p.a+.Cp.	
8.248000000...		70	AC	61	2B	D0	43	70	AC									p.a+.Cp.	
10.18200000...		70	AC	61	2B	D0	43	70	AC									p.a+.Cp.	
12.11600000...		70	AC	61	2B	D0	43	70	AC									p.a+.Cp.	

UNI/O

The UNI/O interface was developed by Microchip. The data transfer rate is 10Kbps to 100Kbps.

Settings



Channel: Show the selected channels (SCIO CH0).

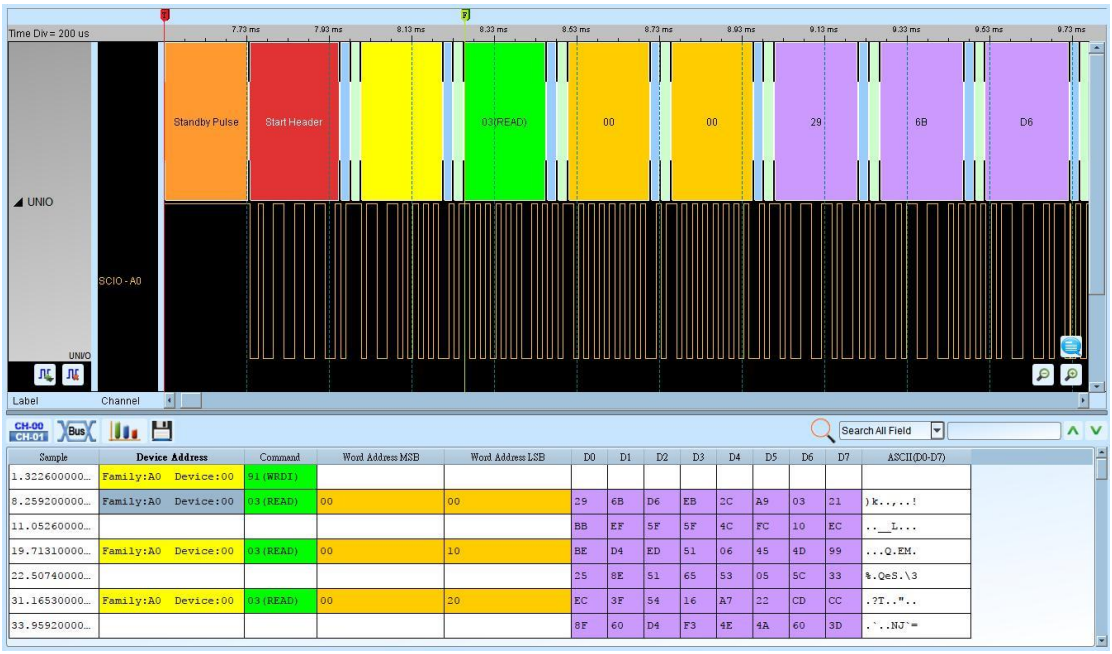
Device Address: Set data bits for the device address.

Tolerance: Set the Input / Output Edge Jitter Tolerance, ±10% / ±25% default.

Report Setting: To show the data by 8 or 16 columns in the Report Window.

Result

Click **OK** to run the UNI/O decode and see the result on the Waveform Window below.

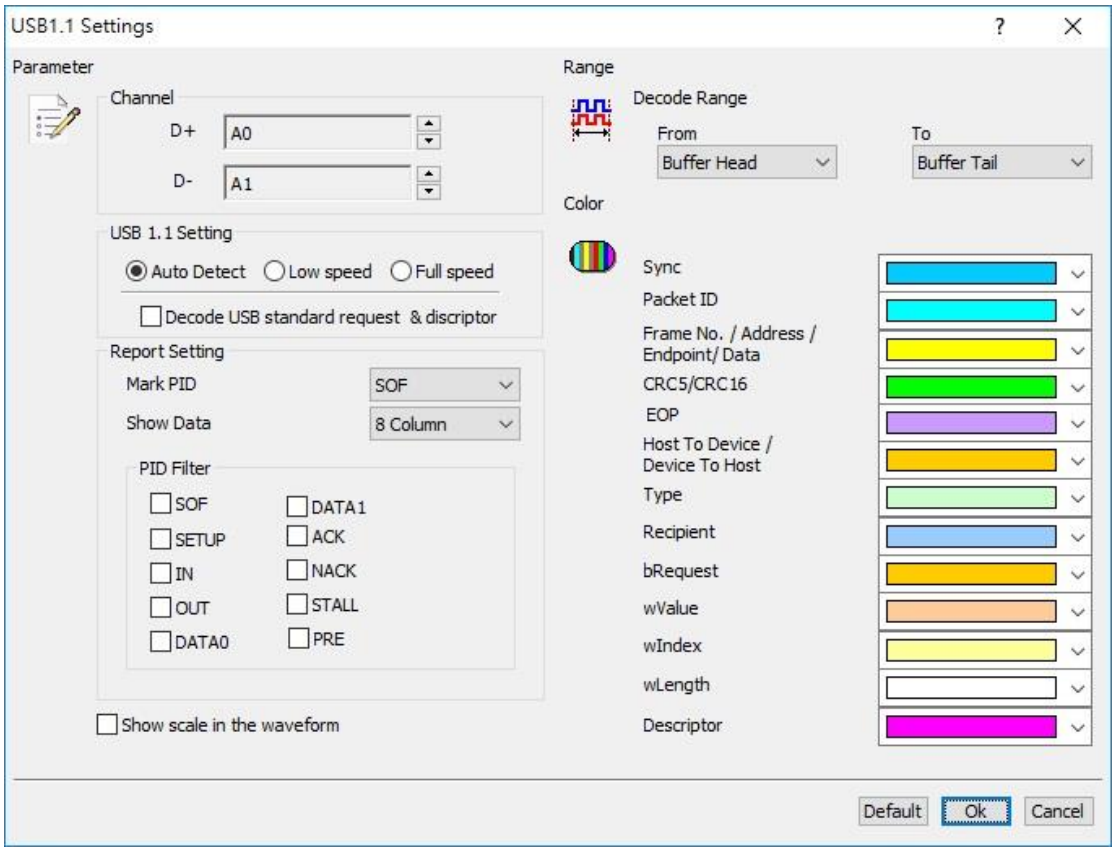


Sample	Device Address	Command	Word Address MSB	Word Address LSB	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)
1.322600000...	Family:A0 Device:00	91(WRDI)											
8.259200000...	Family:A0 Device:00	03(READ)	00	00	29	6B	D6	EB	2C	A9	03	21	)k..,..!
11.05260000...					BB	EF	5F	5F	4C	FC	10	EC	.._L...
19.71310000...	Family:A0 Device:00	03(READ)	00	10	BE	D4	ED	51	06	45	4D	99	...Q.EM.
22.50740000...					25	8E	51	65	53	05	5C	33	%.QeS.\3
31.16530000...	Family:A0 Device:00	03(READ)	00	20	EC	3F	54	16	A7	22	CD	CC	.?T.."..
33.95920000...					8F	60	D4	F3	4E	4A	60	3D	.`..NJ`=

USB1.1

The USB 1.0 specification was introduced in 1994. USB signals are transmitted on a twisted pair data cable with 90 Ohm ±15% impedance, labeled D+ and D−.

Settings

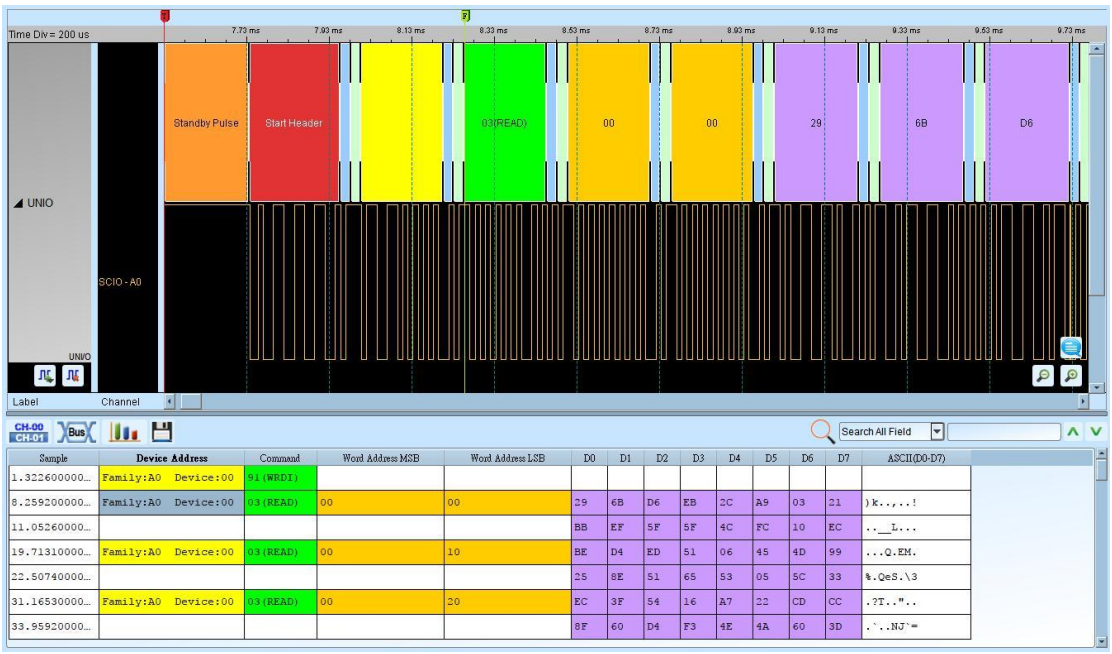


Channel: Show the selected channels (D+ CH0 and D- CH1).

USB1.1 Setting: Select USB state (low speed or full speed) and decode the USB standard request and descriptor.

Result

Click **OK** to run the USB1.1 decode and see the result on the Waveform Window.

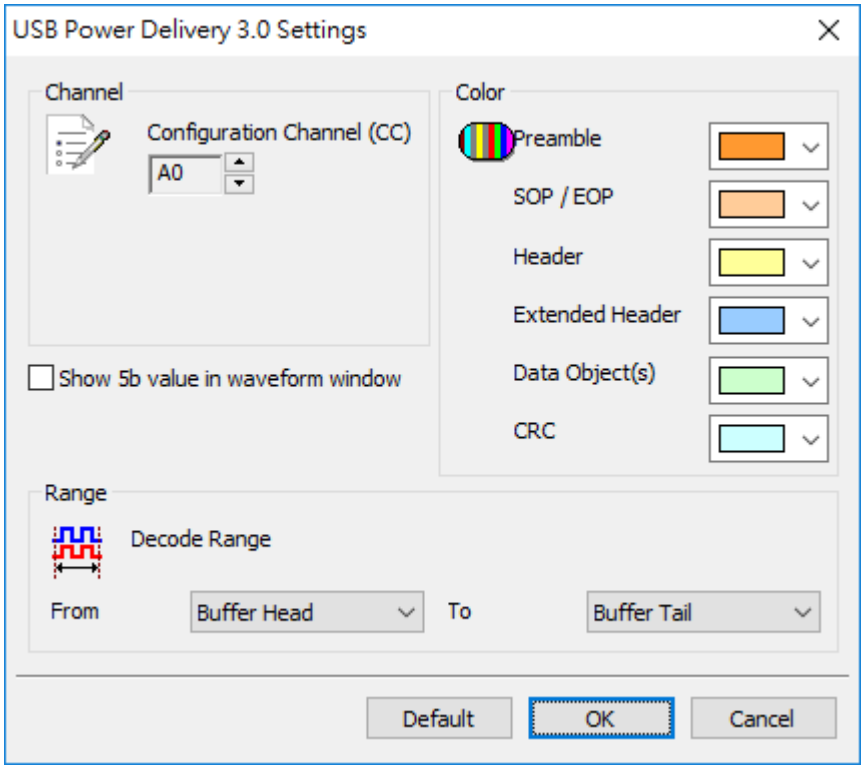


Sample	Device Address	Command	Word Address MSB	Word Address LSB	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)
1.322600000…	Family:A0 Device:00	91 (WRDI)											
8.259200000…	Family:A0 Device:00	03 (READ)	00	00	29	6B	D6	EB	2C	A9	03	21	)k..,..!
11.05260000…					BB	EF	5F	5F	4C	FC	10	EC	.._L...
19.71310000…	Family:A0 Device:00	03 (READ)	00	10	BE	D4	ED	51	06	45	4D	99	...Q.EM.
22.50740000…					25	8E	51	65	53	05	5C	33	%.QeS.\3
31.16530000…	Family:A0 Device:00	03 (READ)	00	20	EC	3F	54	16	A7	22	CD	CC	.?T.."‥
33.95920000…					8F	60	D4	F3	4E	4A	60	3D	.`..NJ`=

USB PD 2.0/3.0

USB PD (Power Delivery) 2.0 is the protocol based on BMC (Biphase Mark Coding) and can be applied to Laptops / Tablets / Mobile phones / Power banks or other devices with USB Type-C for power supplying or charging. The maximum power offered by USB Type-C can be 100W, and the users can charge the device by supporting USB Type-C connector.

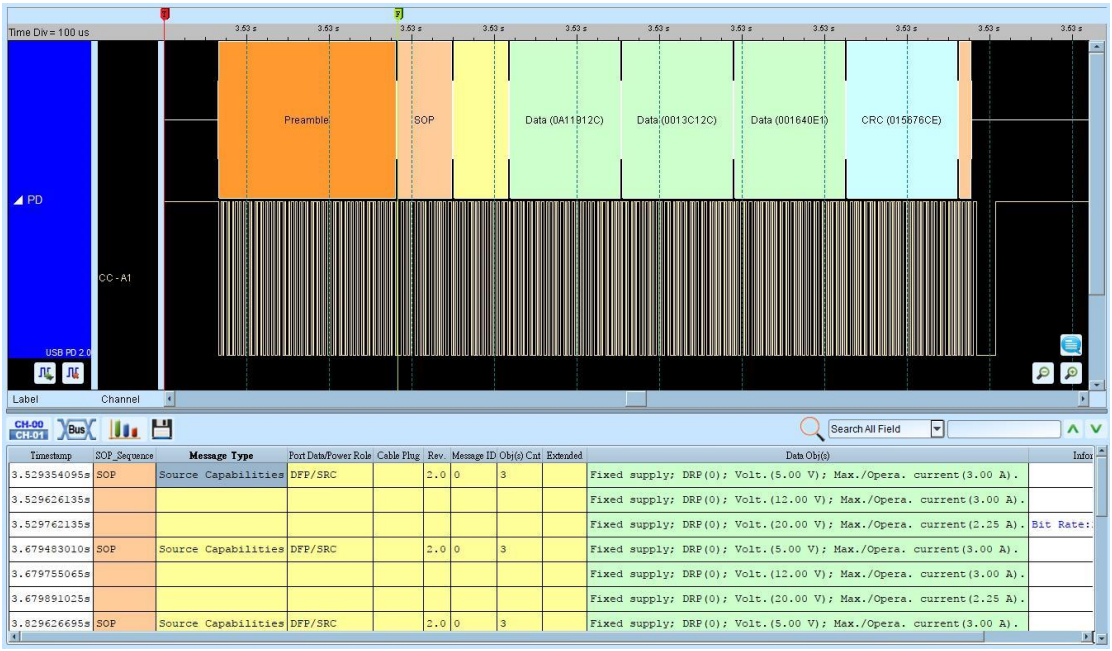
Settings



Channel: Set Configuration Channel (CC).

Show 5b value in waveform window: Show 4b or 5b value in the waveform.

Result

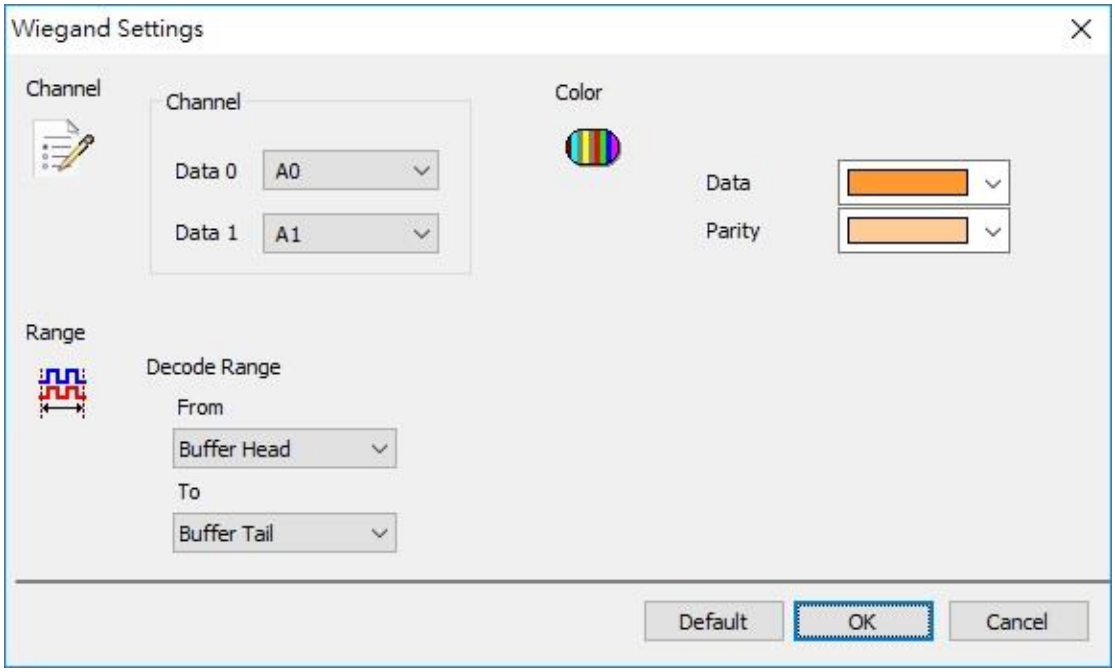


Timestamp	SOP_Sequence	Message Type	Port Data/Power Role	Cable Plug	Rev.	Message ID	Obj(s) Cnt	Extended	Data Obj(s)	Infor
3.529354095s	SOP	Source Capabilities	DFP/SRC		2.0	0	3		Fixed supply; DRP(0); Volt.(5.00 V); Max./Opera. current(3.00 A).	
3.529626135s									Fixed supply; DRP(0); Volt.(12.00 V); Max./Opera. current(3.00 A).	
3.529762135s									Fixed supply; DRP(0); Volt.(20.00 V); Max./Opera. current(2.25 A).	Bit Rate:
3.679483010s	SOP	Source Capabilities	DFP/SRC		2.0	0	3		Fixed supply; DRP(0); Volt.(5.00 V); Max./Opera. current(3.00 A).	
3.679755065s									Fixed supply; DRP(0); Volt.(12.00 V); Max./Opera. current(3.00 A).	
3.679891025s									Fixed supply; DRP(0); Volt.(20.00 V); Max./Opera. current(2.25 A).	
3.829626695s	SOP	Source Capabilities	DFP/SRC		2.0	0	3		Fixed supply; DRP(0); Volt.(5.00 V); Max./Opera. current(3.00 A).	

Wiegand

It is commonly used to connect a card swipe mechanism to the rest of an electronic entry system..

Settings



Channel: Show the selected channels (Data 0 and Data 1).

Result

Click **OK** to run the wiegand decode and see the result on the Waveform Window.

Chapter 2 Bus Trigger

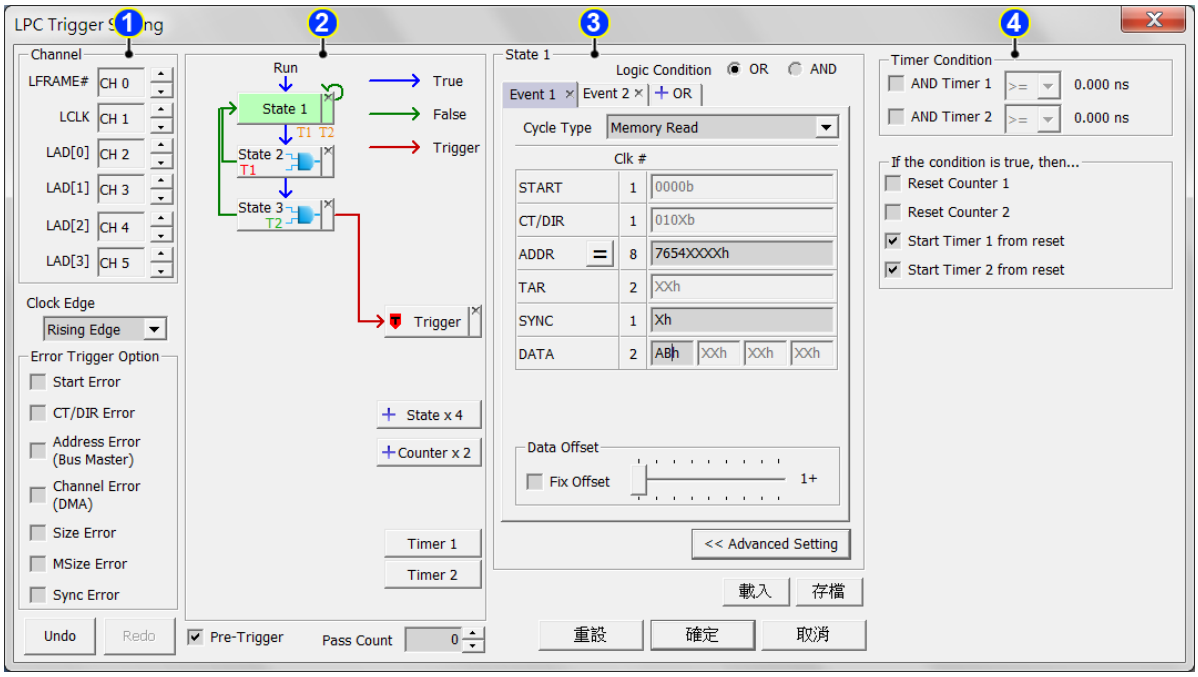
Bus Trigger

The bus trigger are only available for the TravelLogic Series.

Bus Trigger	TravelLogic B+	TravelLogic B	TravelLogic E	TravelLogic
CAN	◎	◎		◎
eSPI	◎			
I2C	◎	◎		◎
I2S	◎	◎	◎	◎
LIN	◎	◎		
LPC	◎	◎		
MIPI SPMI	◎			
NAND Flash	◎			
SD/eMMC	◎			
Serial Flash	◎			
SMBus/PMBus	◎	◎		
SPI	◎	◎		◎
SVI2	◎	◎		
SVID	◎	◎		◎
UART	◎	◎		◎
USB 1.1	◎	◎		

Clause Trigger

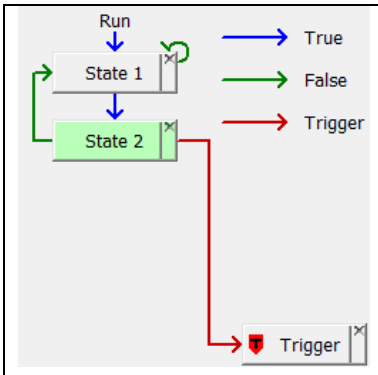
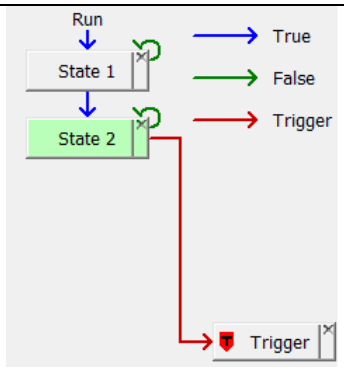
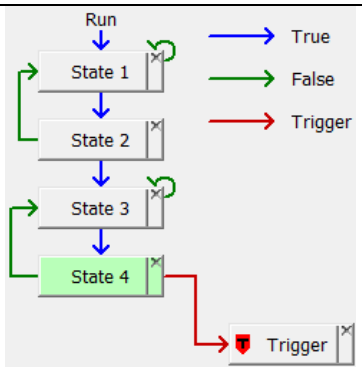
The Clause trigger settings dialog box is as below.

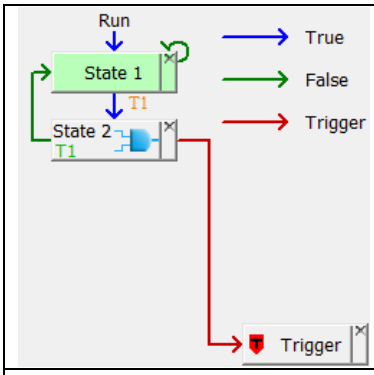
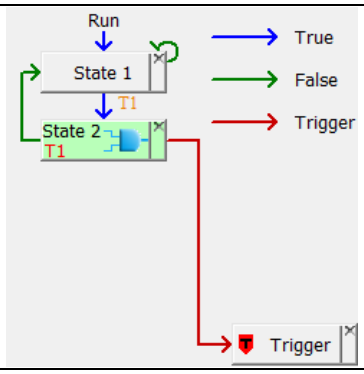


1. Channel and bus trigger settings:

Please refer to the descriptions in each bus trigger settings section.

2. Flow chart

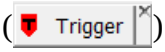
		
State 1 next State 2	State 1 then State 2	State 1 next State 2 then State 3 next State 4

	
State 1 (Active T1) next State 2 (Time >= T1)	State 1 (Active T1) next State 2 (Time < T1)

A state button represents a trigger state. The true state condition will only lead the branch to the next state, on the other hand, the false state condition could lead the branch to any state as below:

Click state 1 and state 2, then state 1 will branch to state 2 while state 1 is false.

Double click any state, the state will branch to itself if it is false.

Click the state button and trigger button (

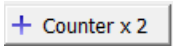
): triggere when the state conditions is satisfied.

Delete any state by clicking the cross sign on the state.

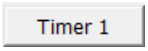
Clear the links to the trigger button by clicking on the trigger button (

)

Click 

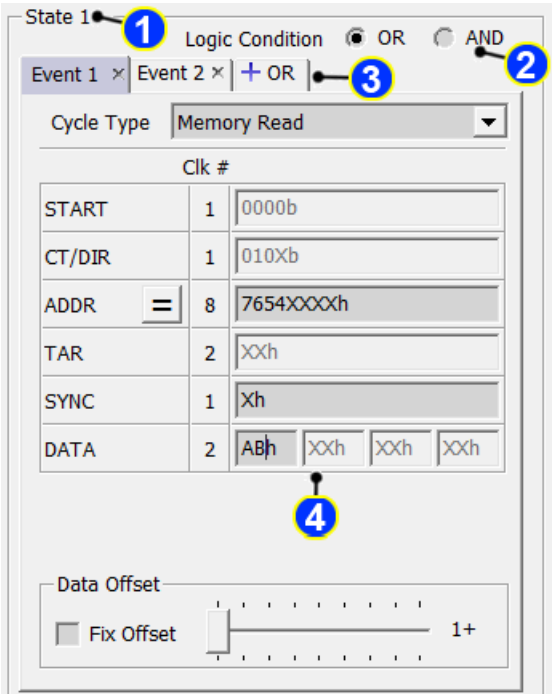
and 

to add a new state.



: The timer ranges from 5 ns to 8 days.

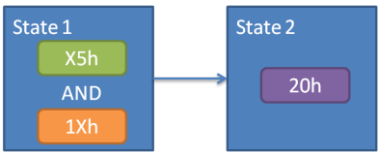
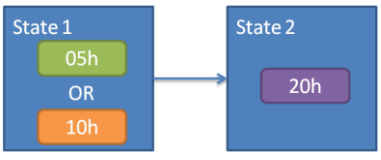
3. State settings

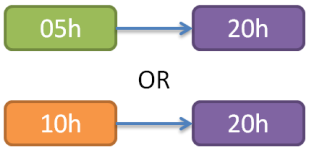


The trigger conditions of the state:

1. The current state index
2. Logic condition between every event in the state.
3. Switch between the tab windows to edit the trigger events . Click | + OR | / | + AND | to add new events (up to 8 events). All inputs are supported binary(e.g. **01000001b)**/decimal(e.g. **65**)/ hexadecimal(e.g. **41h**)
4. The bus trigger settings.

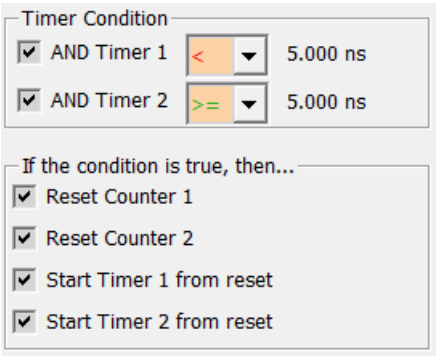
The relations between events and the trigger condition:

	AND	OR
Event settings		

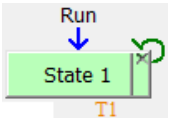
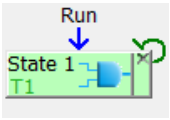
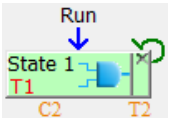
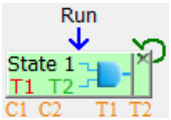
Trigger condition		

4. Timer and Counter settings

Press Advanced Setting >> button to edit the timer/counter reset settings of the state.



The following table describes the state button icons:

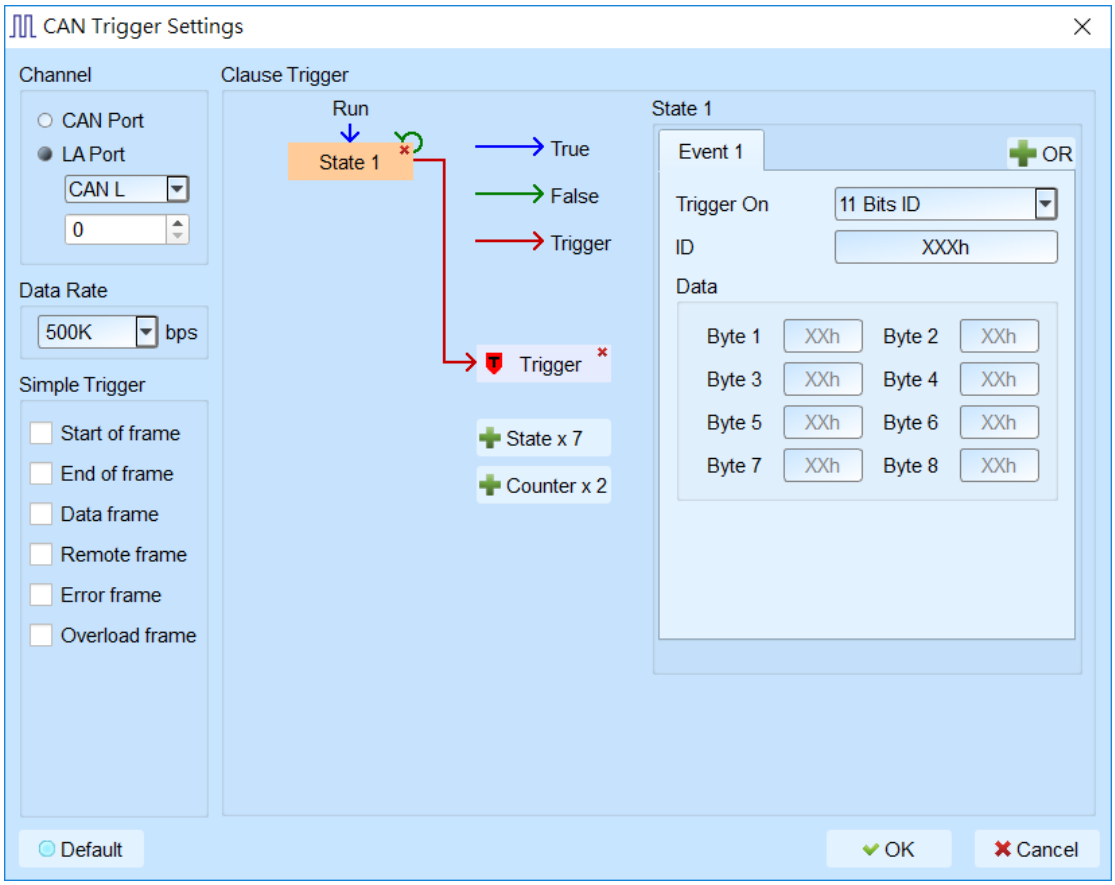
				
Conditions	State 1	State 1 And timer > T1	State 1 And timer < T1	State 1 And T2 < timer <T1
satisfied condition	Start T1	X	Start T2 Reset C2	Start T1 and T2 Reset C1 and C2

CAN Trigger

Supported Models：TB1016B. TB1016B+. TL3134B. TL3234B+. LA3068B. LA3136B

CAN Trigger Settings

Click CAN Trigger in the toolbar and will show the dialog as the following。



1. **Channel:** Select CAN_H or CAN_L as the trigger channel.
2. **Data Rate:** CAN data rate. Users could type the data rate if no data rate is available.
3. **Simple Trigger:** Specific trigger function of CAN.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; there are

11 Bits ID, 29 Bits ID, Data, 11 Bits ID + Data and 29 Bits ID + Data selections in the Trigger On; selecting one of them and typing the trigger values in the ID or Data fields, default value is XX means “don’t care”.

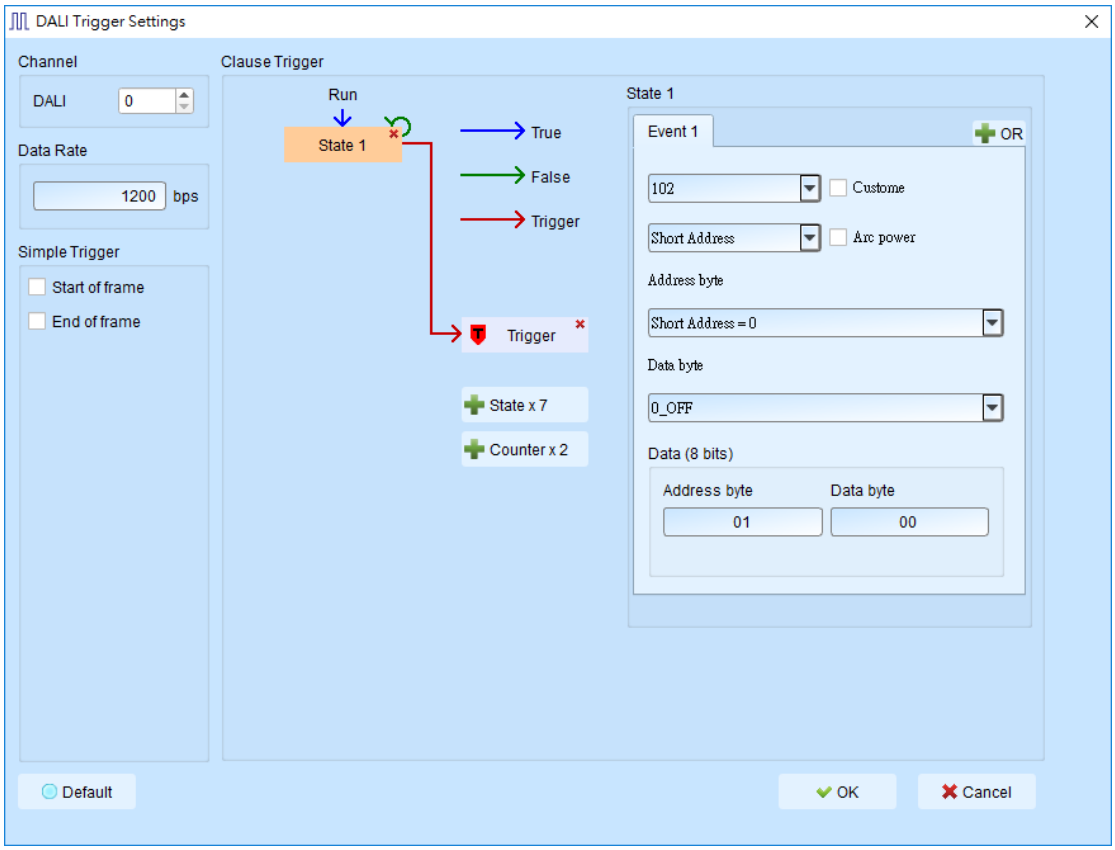
Note: Only TB1016B. TB1016B+ provide CAN port channel

DALI Trigger

Supported Models：TB1016E, TB1016B, TB1016B+, TL3134B, TL3234B+, LA3068B, LA3136B

DALITrigger Settings

Click DALI Trigger in the toolbar and will show the dialog as the following.



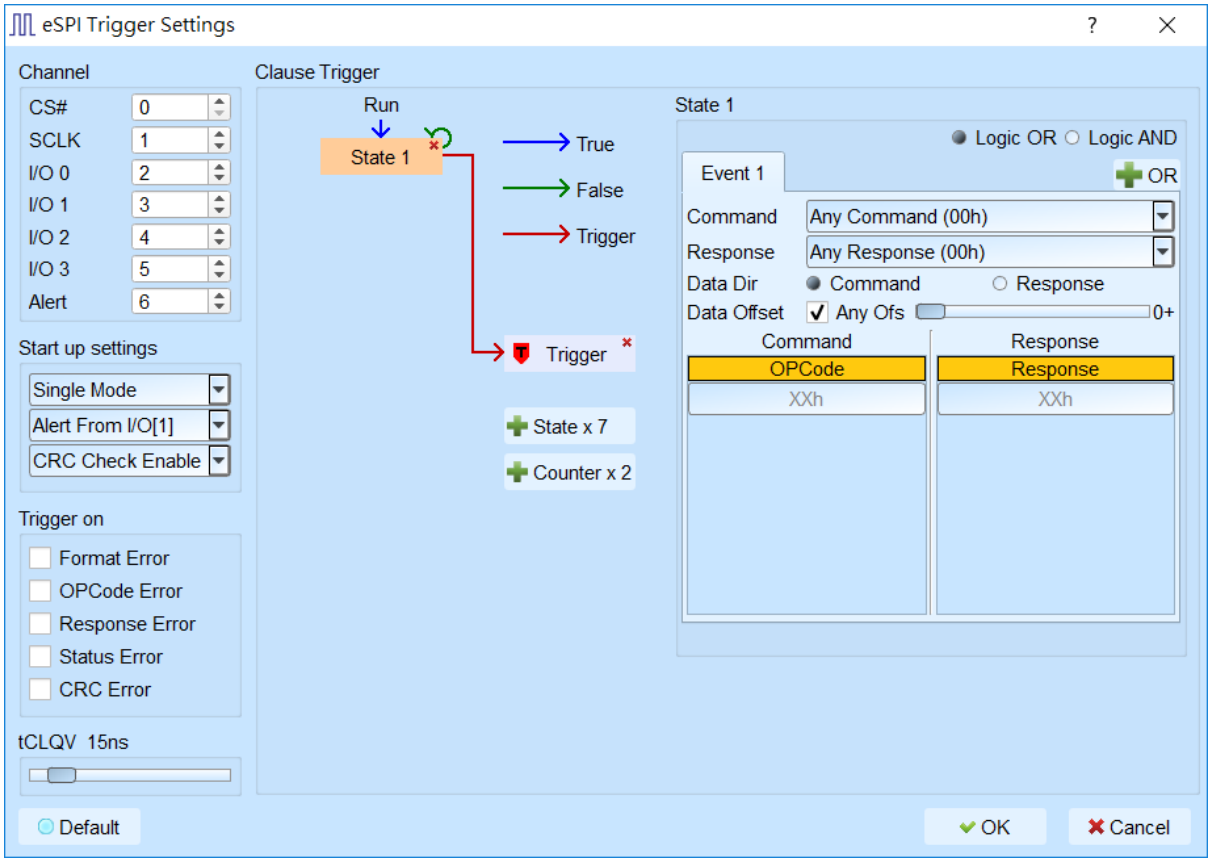
1. **Channel:** Select channels.
2. **Simple Trigger:** Trigger specific of DALI.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; selecting the trigger type of DALI (102, 103), command type (short address, group address, broadcast, response, special command), or custom cmd.

eSPI Trigger

Supported Models：TL3234B+. LA3068B. LA3136B

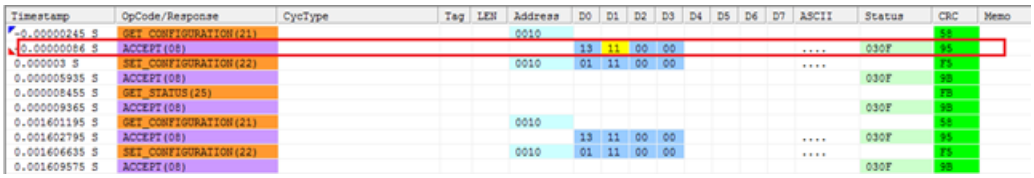
eSPI Trigger Settings

Click eSPI Trigger in the toolbar and will show the dialog as the following.



5. **Channel:** Select channels.
6. **Startup settings:** Set the initial parameters of eSPI.
7. **Trigger on:** Trigger specific error of eSPI.
8. **Clause Trigger:** Please reference Clause Trigger chapter.
9. **State:** Show the details of trigger condition in every state as left side; selecting the trigger values in the Command, Response fields, default value is 00h.

   Data Dir: Trigger the data in the Command or Response.



Timestamp	OpCode/Response	CycType	Tag	LEN	Address	D0	D1	D2	D3	D4	D5	D6	D7	ASCII	Status	CRC	Memo
-0.00000245 S	GET_CONFIGURATION(21)				0010											55	
0.00000086 S	ACCEPT(08)					13	11	00	00					....	030F	95	
0.000003 S	SET_CONFIGURATION(22)				0010	01	11	00	00					....		F5	
0.000005935 S	ACCEPT(08)														030F	9B	
0.000008455 S	GET_STATUS(25)															FB	
0.000009365 S	ACCEPT(08)														030F	9B	
0.001601195 S	GET_CONFIGURATION(21)				0010											55	
0.001602795 S	ACCEPT(08)					13	11	00	00					....	030F	95	
0.001606635 S	SET_CONFIGURATION(22)				0010	01	11	00	00					....		F5	
0.001609575 S	ACCEPT(08)														030F	9B	

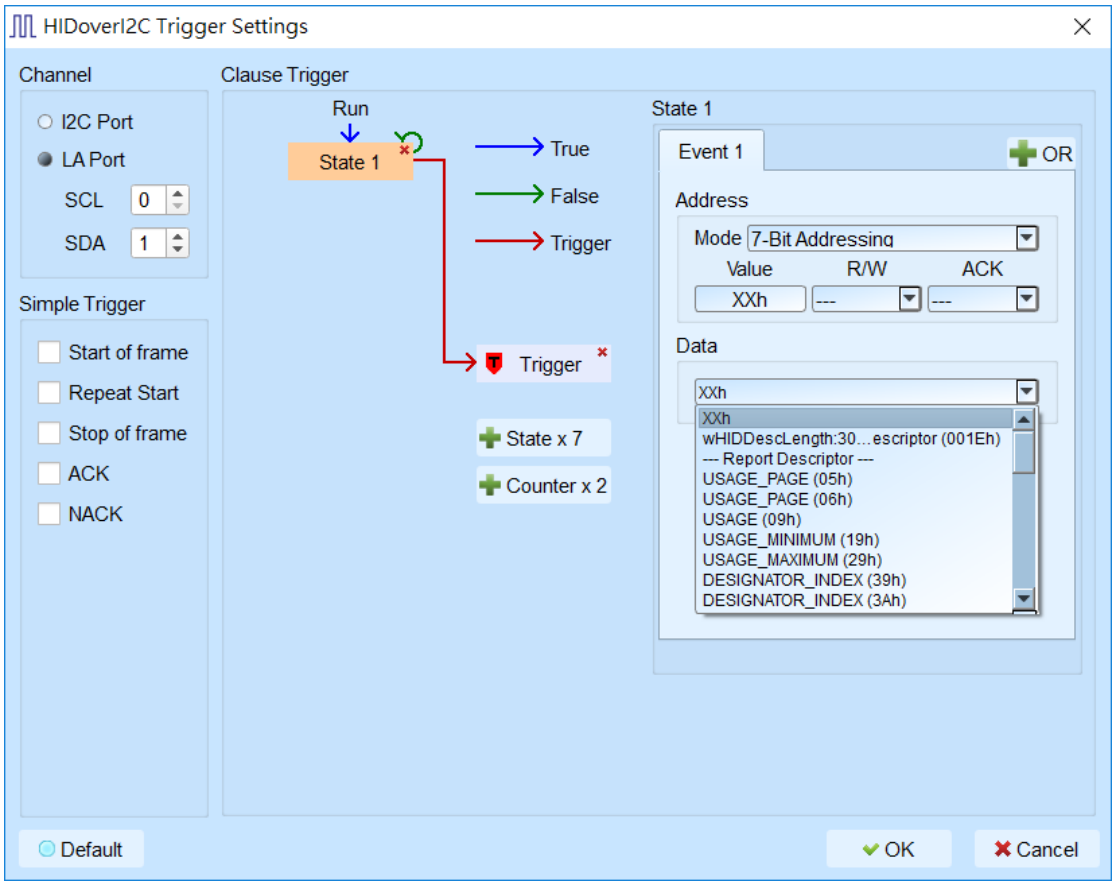
Data Offset: **Trigger the data from start of data frame without any offset. For example, setting D0 13h will check the first byte of data frame. With any offset, the siganl would be triggered by the byte pattern. For instance, setting D0+ XXh D1+ 11h, and the byte pattern of XXh and 11h will be triggered regardless of the position of the data.**

HIDoverI2C Trigger

Supported Models：TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+. LA3068B. LA3136B

HIDoverI2C Trigger Settings

Click HIDoverI2C Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select I2C / LA port.
2. **Simple Trigger:** Specific trigger function of I2C.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the R/W, ACK and Data(HID Descriptor) fields, default value is XX means “don’t care”. When trigger the descriptor, R/W field

will be selected Read state automatically.

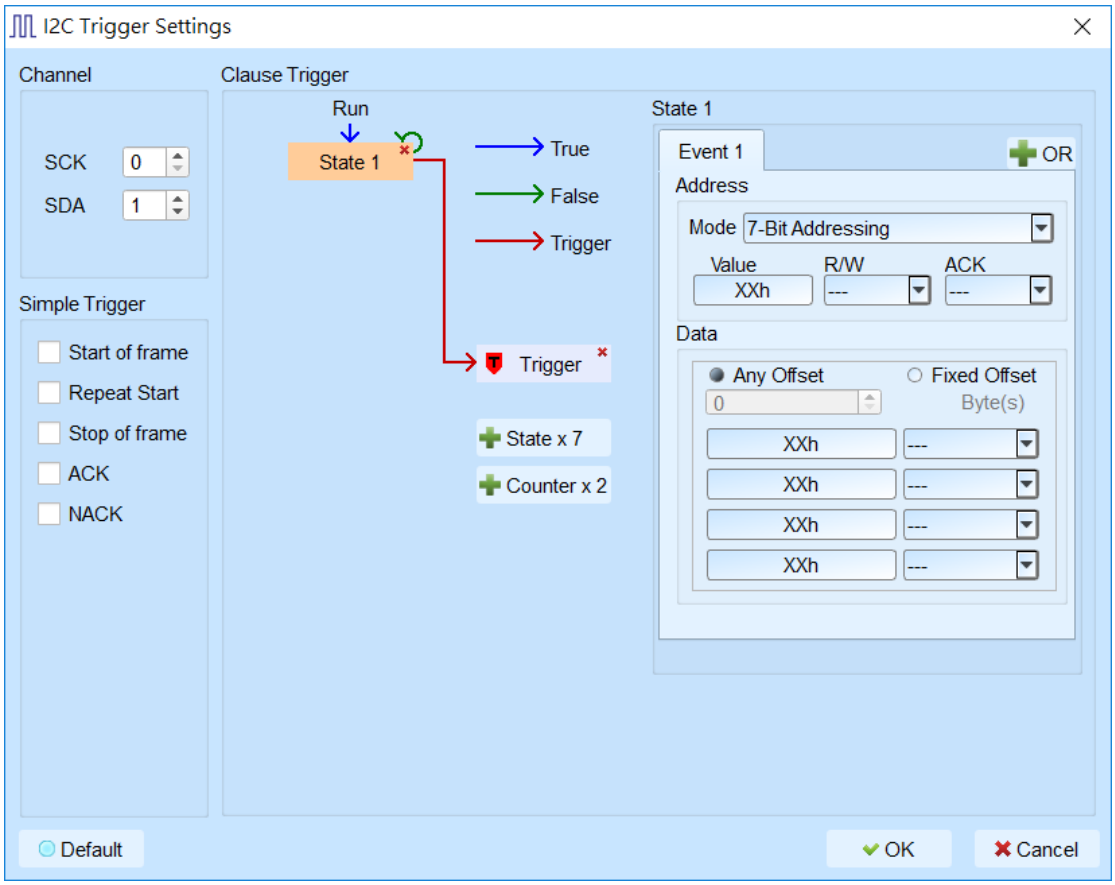
Note: Only TravelBus series provide I2C port channel

I²C Trigger

Supported Models：TravelBus series. TravelLogic series. Logic Analyzer series

I2C Trigger Settings

Click I2C Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select I2C / LA port.
2. **Simple Trigger:** Specific trigger function of I2C.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the R/W, ACK and Data fields, default value is XX means “don’t care”. Data field only provided 4 bytes data to trigger, checking the Fixed offset and selecting the offset value when want to trigger at the specific

position.

Note: Only TravelBus series provide I2C port channel

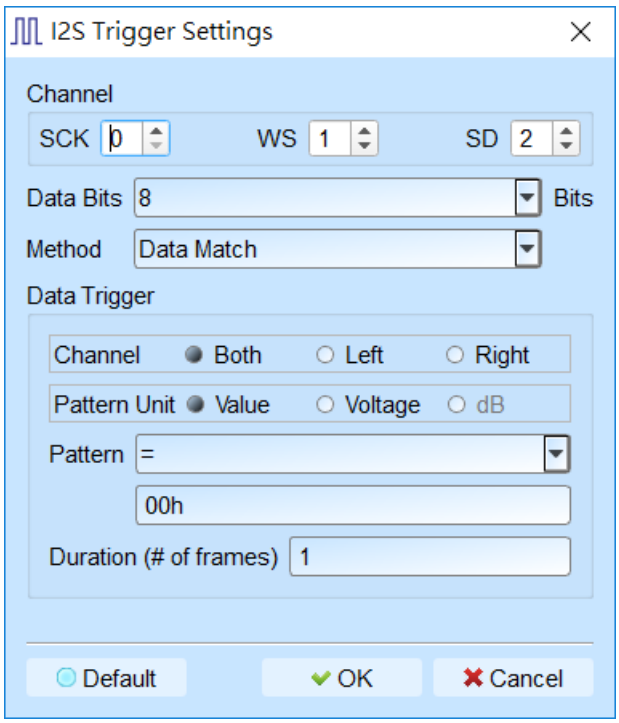
I²S Trigger

Supported Models：TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+.

LA3068B. LA3136B

I2S Trigger Settings

Click I2S Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select Serial clock (SCK), word select (WS) and serial data (SD).
2. **Data Bits:** 1-32 bits, normally it is 8, 12, 16, 24 or 32.
3. **Method:**

   Data Match： Trigger when the conditions matched.

   Rising Edge： Trigger when it is a rising edge between two patterns.

   Falling Edge： Trigger when it is a falling edge between two patterns.

   Glitch： Trigger when there is a glitch.

   Mute： When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of -P < X < +P.

Clip： When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of -P < X ∪ +P > X.

Timing Violation： Provide 6 trigger conditions and this function will be enabled at 200 MHz sampling rate.

4. **Data Trigger:** Select Both, Left, Right channel and pattern unit.

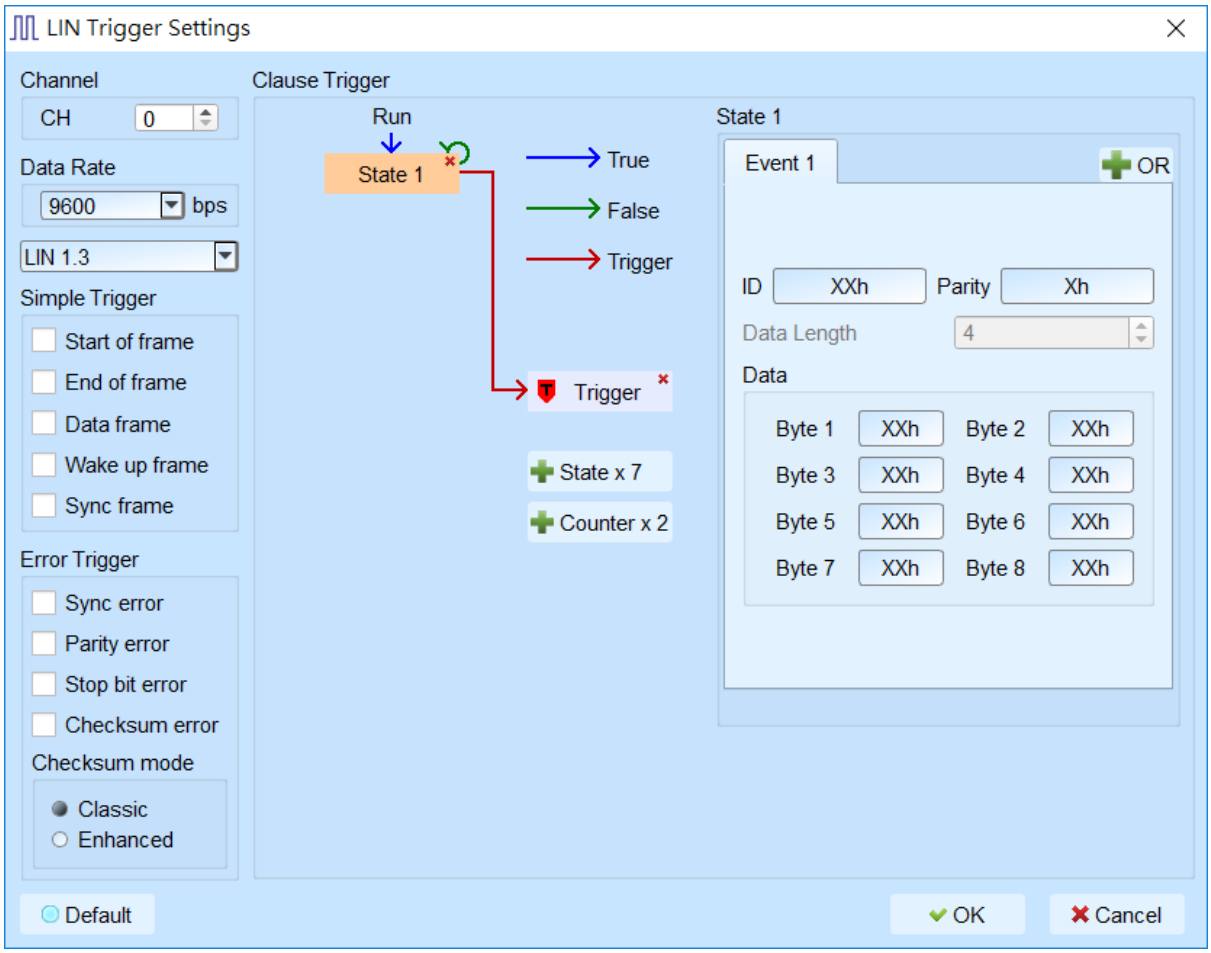
LIN Trigger

Supported Models：TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+.

LA3068B. LA3136B

LIN Trigger Settings

Click LIN Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select channels.
2. **Simple Trigger:** Specific trigger function of LIN.
3. **Error Trigger:** Trigger specific error of LIN.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the ID, Parity, Data Length and Data fields, default value is XX means “don’t care”. When select the LIN 2.2, Data Length field will

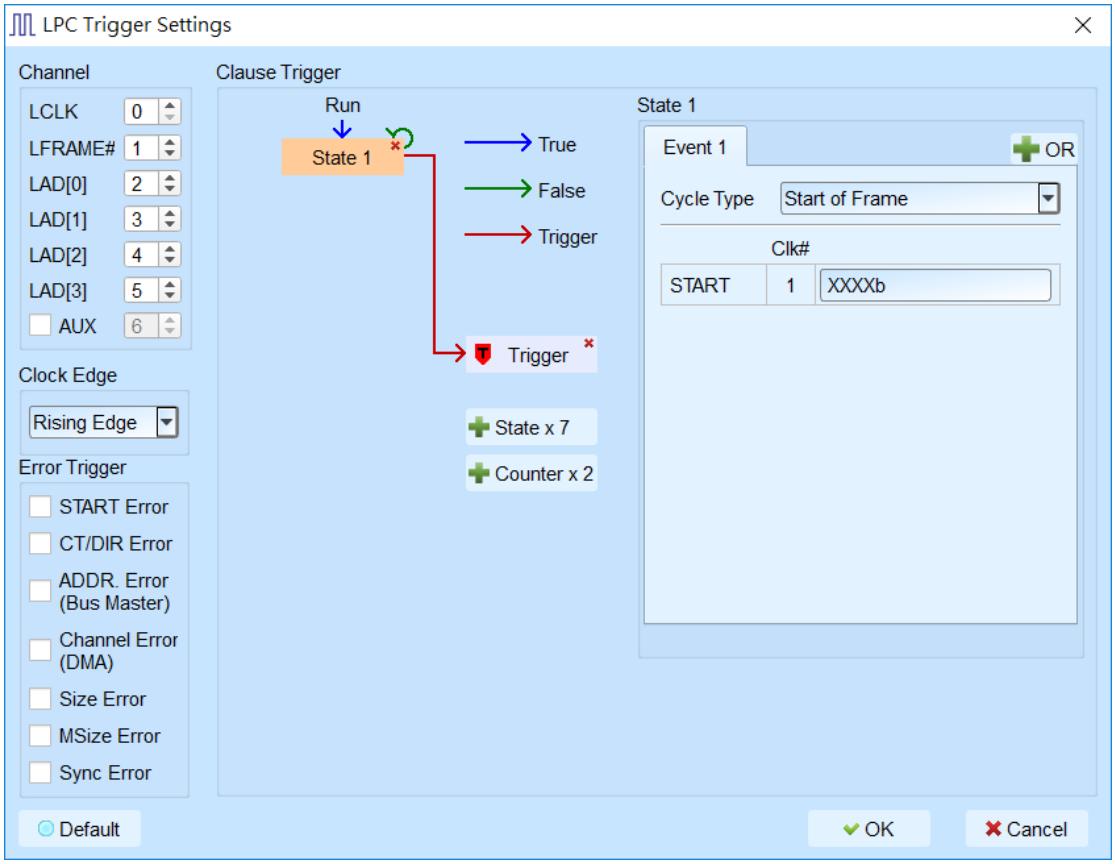
be enabled.

LPC Trigger

Supported Models：TL3134B. TL3234B+

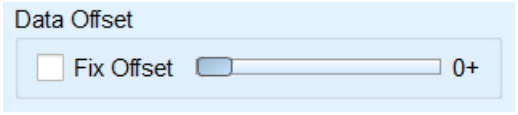
LPC Trigger Settings

Click LPC Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select LPC channels.
2. **Clock Edge:** Select Rising/Falling clock edge.
3. **Error Trigger:** Trigger specific error of LPC.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Cycle Type and its parameters, default value is XX means “don’t care”. Switch =/≠/>/≤ by click = button.

Data offset setting:



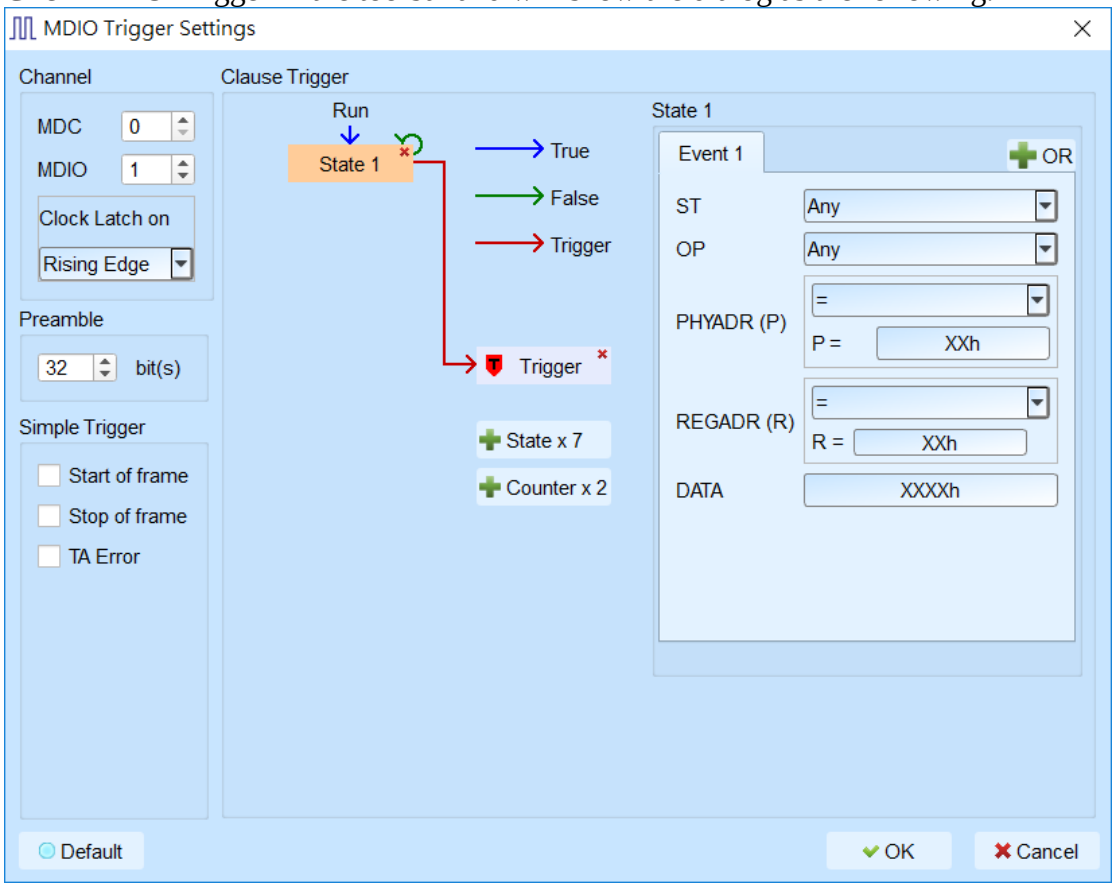
MDIO Trigger

Supported Models：TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+.

LA3068B. LA3136B

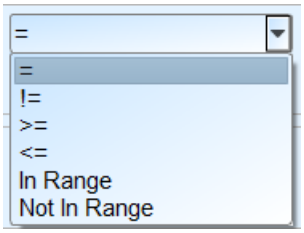
MDIO Trigger Settings

Click MDIO Trigger in the toolbar and will show the dialog as the following.



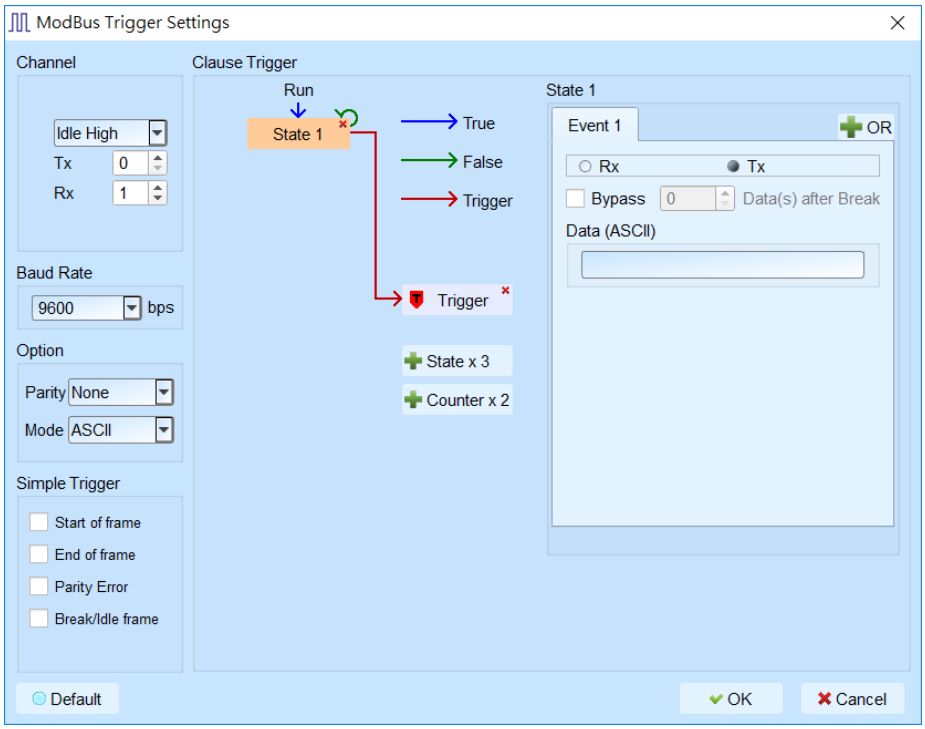
1. **Channel:** Select MDC / MDIO channels.
2. **Preamble:** Select the length of preamble.
3. **Simple Trigger:** Specific trigger function of MDIO.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the ST, OP, PHYADR, REGADR and DATA fields, default value is XX means “don’t care”.

   PHYADR(P) / REGADR(R) fields provided the range function:

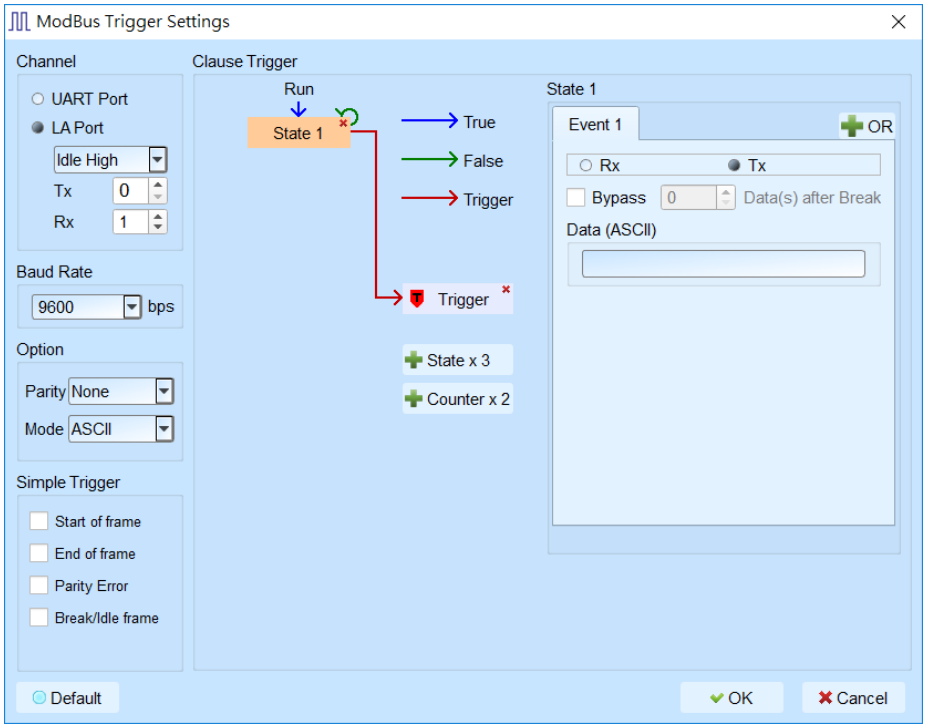


ModBus Logic Trigger

TL3K/LA3K Settings



TBA Settings



Channel

UART Port / LA PortSelect ModBus channels.

Baud Rate

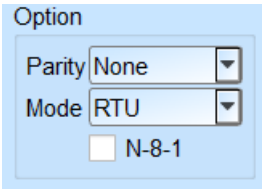
Select the baud rate and providing the manual input if no appropriate selection.

Option

Parity Provide None/Odd/Even selections, none parity defaulted.

Mode Provide ASCII/RTU mode, ASCII mode defaulted.

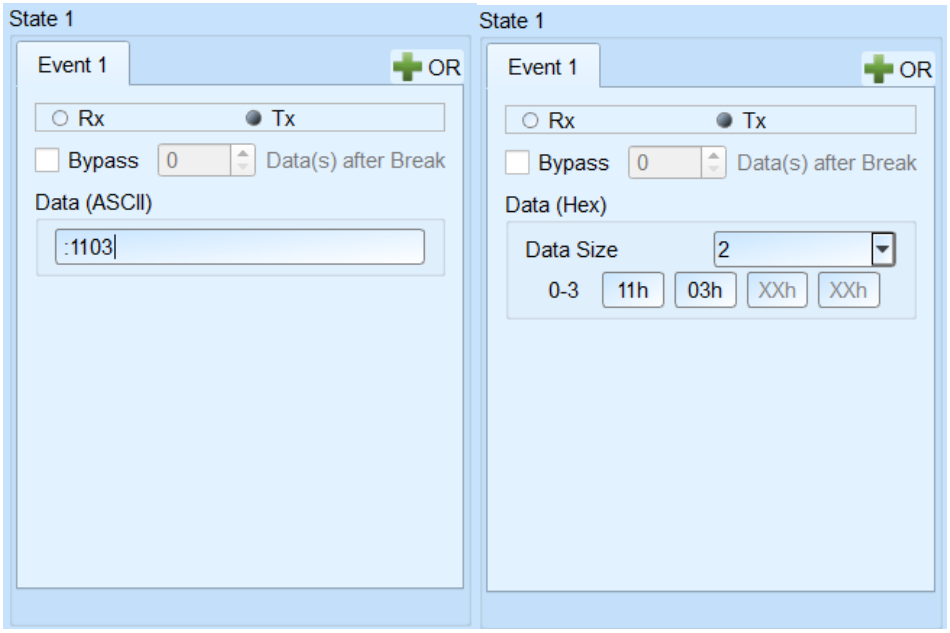
Support the 8-N-1 protocol under RTU mode, 8-N-2 protocol defaulted.



Simple Trigger Provide Start of frame, End of frame, Parity Error, Break/Idle frame triggers。

State Provide ASCII/HEX input mode by ASCII/RTU mode.

ASCII RTU

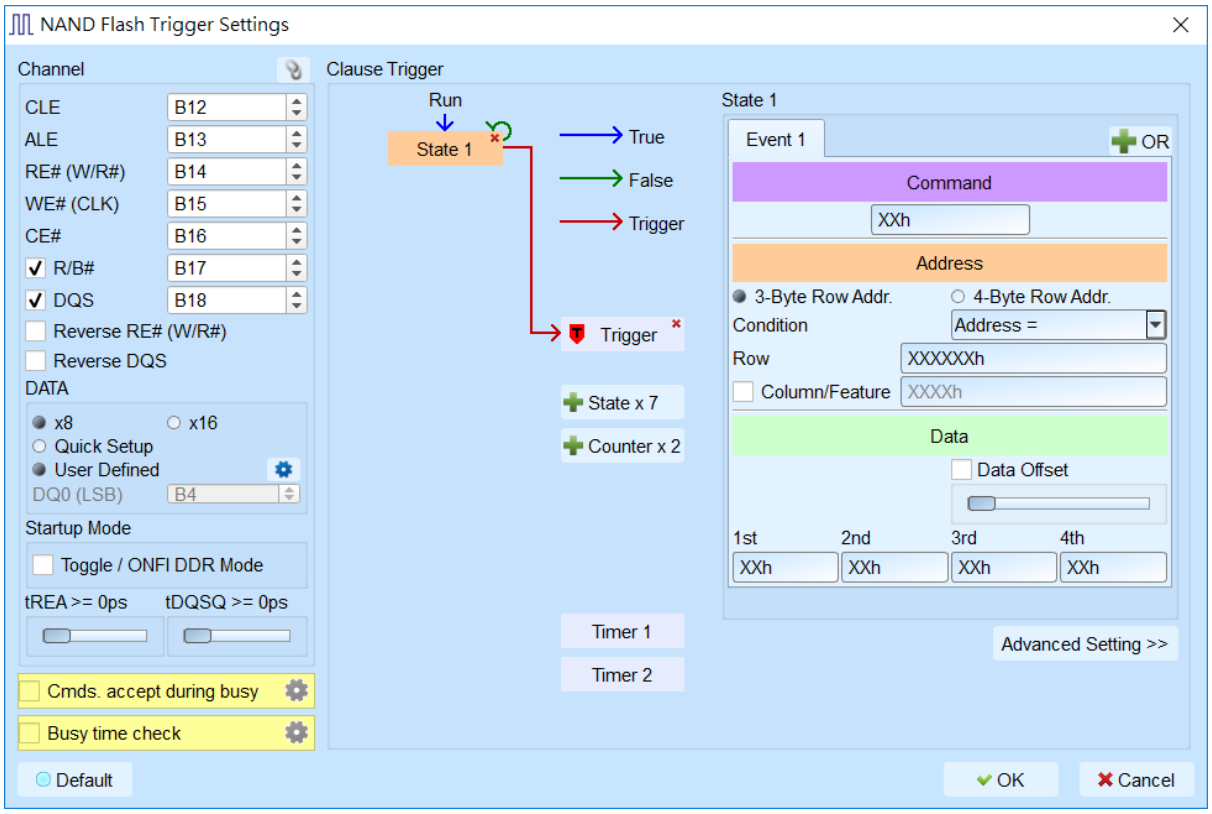


NAND Flash Trigger

Supported Models：TL3234B+. LA3136B. BusFinder (NAND Flash solution)

NAND Flash Trigger Settings

Click NAND Flash Trigger in the toolbar and will show the dialog as the following.

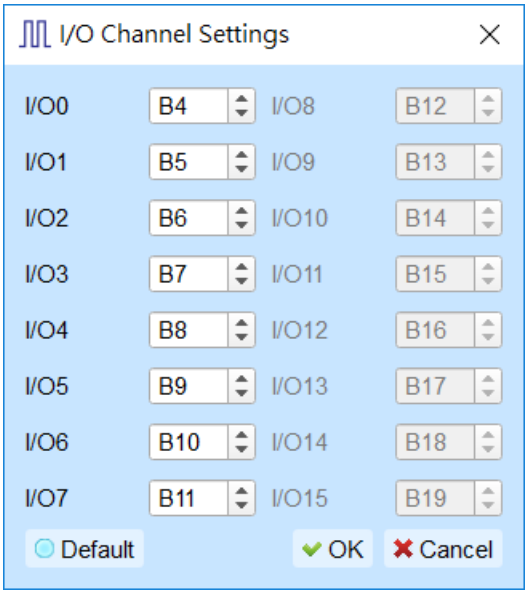


1. **Channel:** Select CLE, ALE, RE, WE, CE, R/B, DQS channels.
2. **DATA:** Select x8 or x16 bits

   I. **Quick Setup:** Only set DQ0(LSB), others will be set automatically.

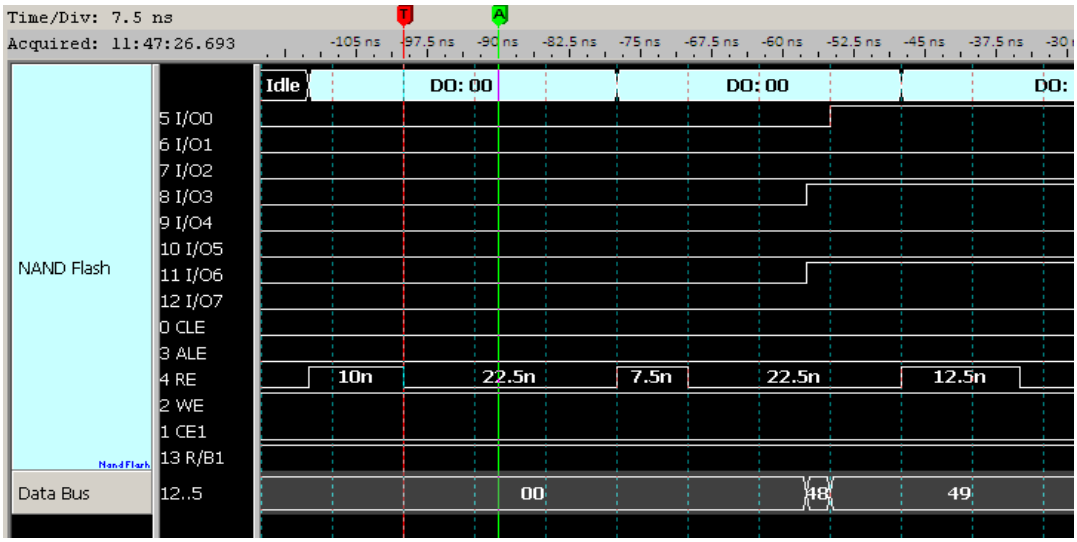
   (e.g. LSB = B4, MSB = B11; LSB = B7, MSB = B14)

   II. **User Defined:**

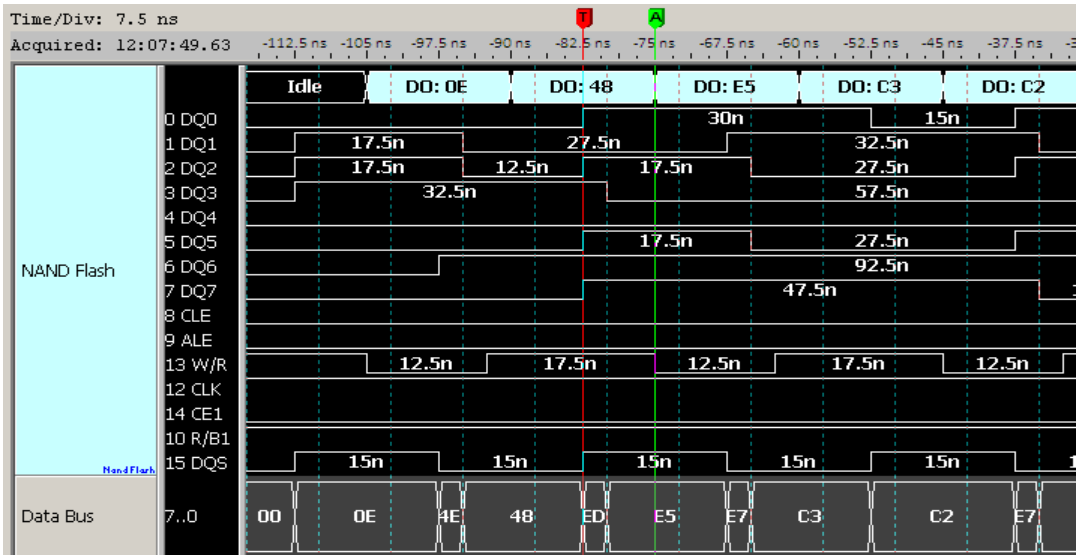


6. **Startup Mode:** Set DDR mode.
7. **tREA / tDQSQ:** Set tREA at SDR mode and tDQSQ at DDR mode.

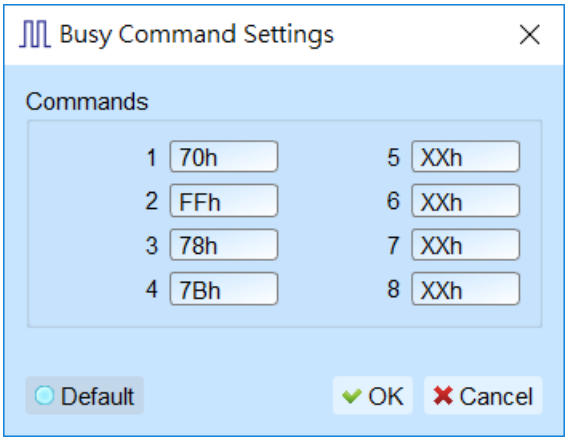
tREA:



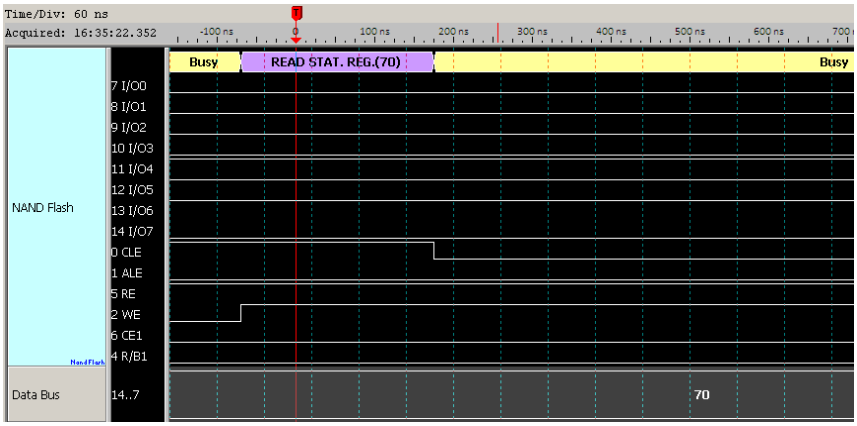
tDQSQ:



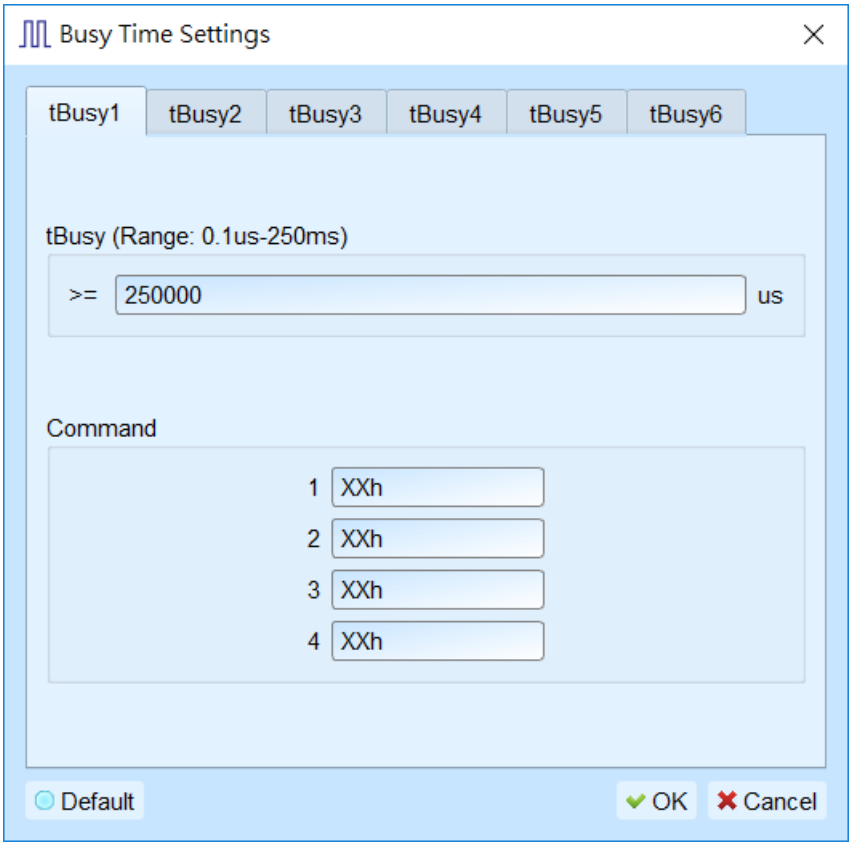
8. **Commands accepted during busy:** Set NAND commands still could be triggered during busy state, default is 70h/FFh/78h/7Bh.



Trigger 70h during busy state:



9. **Busy time check:** Triggers when timing >= tBusy, providing 6 tBusy to check.



Trigger the tBusy >= 25 us after NAND command (10h)

10. **Clause Trigger:** Please reference Clause Trigger chapter.
11. **State:** Show the details of trigger condition in every state as left side; selecting the trigger values in the Command, Address and Data fields, default value is XX means “don’t care”.

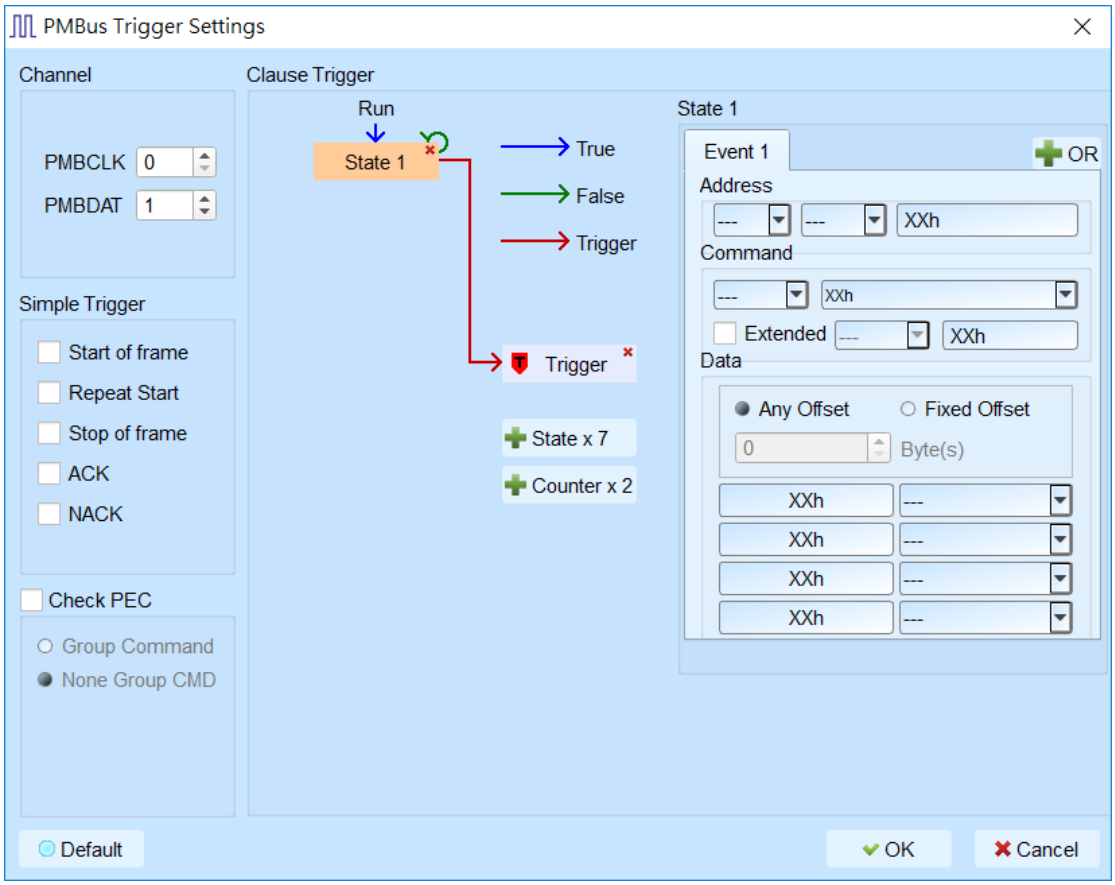
PMBus Trigger

Supported Models：TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+.

LA3068B. LA3136B

PMBus Trigger Settings

Click PMBus Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select I2C / LA port.
2. **Simple Trigger:** Specific trigger function of I2C.
3. **Check PEC:** Trigger PEC.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Address, Command and Data fields, default value is XX means “don’t care”.

   Data field only provided 4 bytes data to trigger, checking the Fixed offset and

selecting the offset value when want to trigger at the specific position.

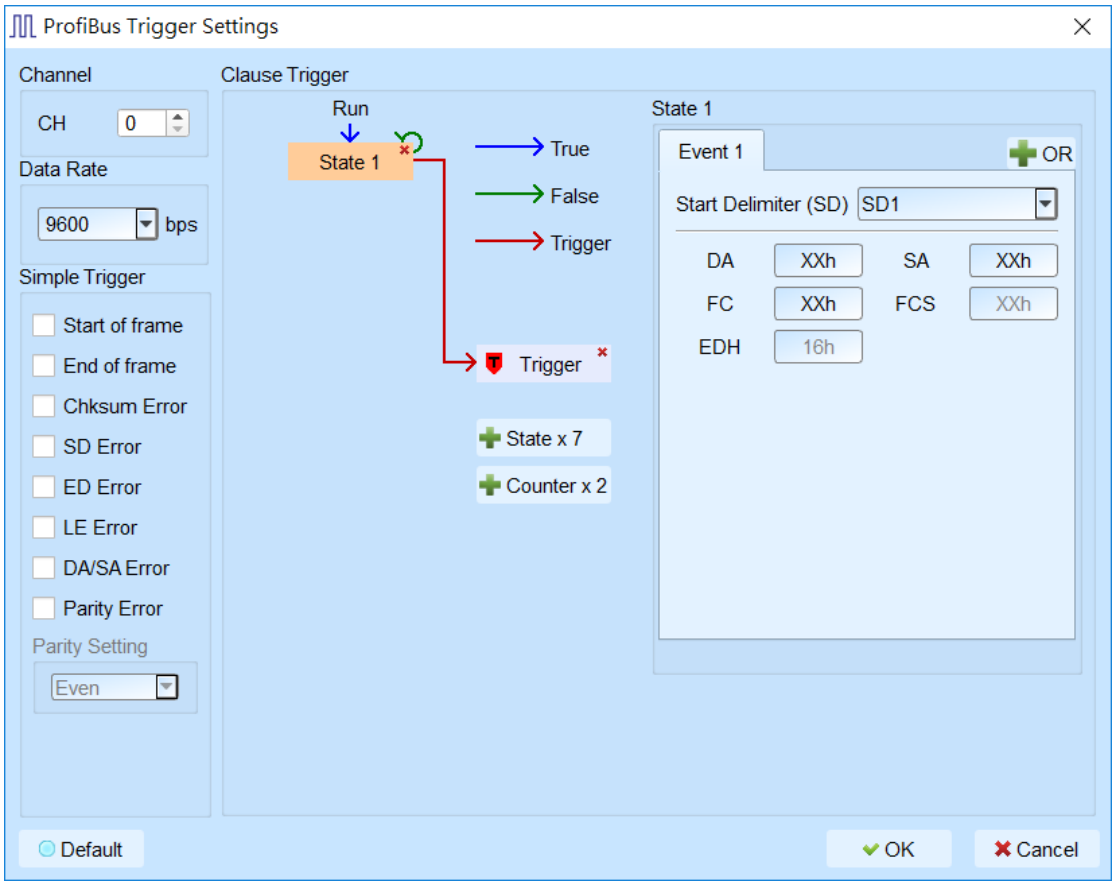
Note: Only TravelBus series provide I2C port channel

ProfiBus Trigger

Supported Models：TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+. LA3068B. LA3136B

ProfiBus Trigger Settings

Click ProfiBus Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select channels.
2. **Simple Trigger:** Specific trigger function of ProfiBus.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing or

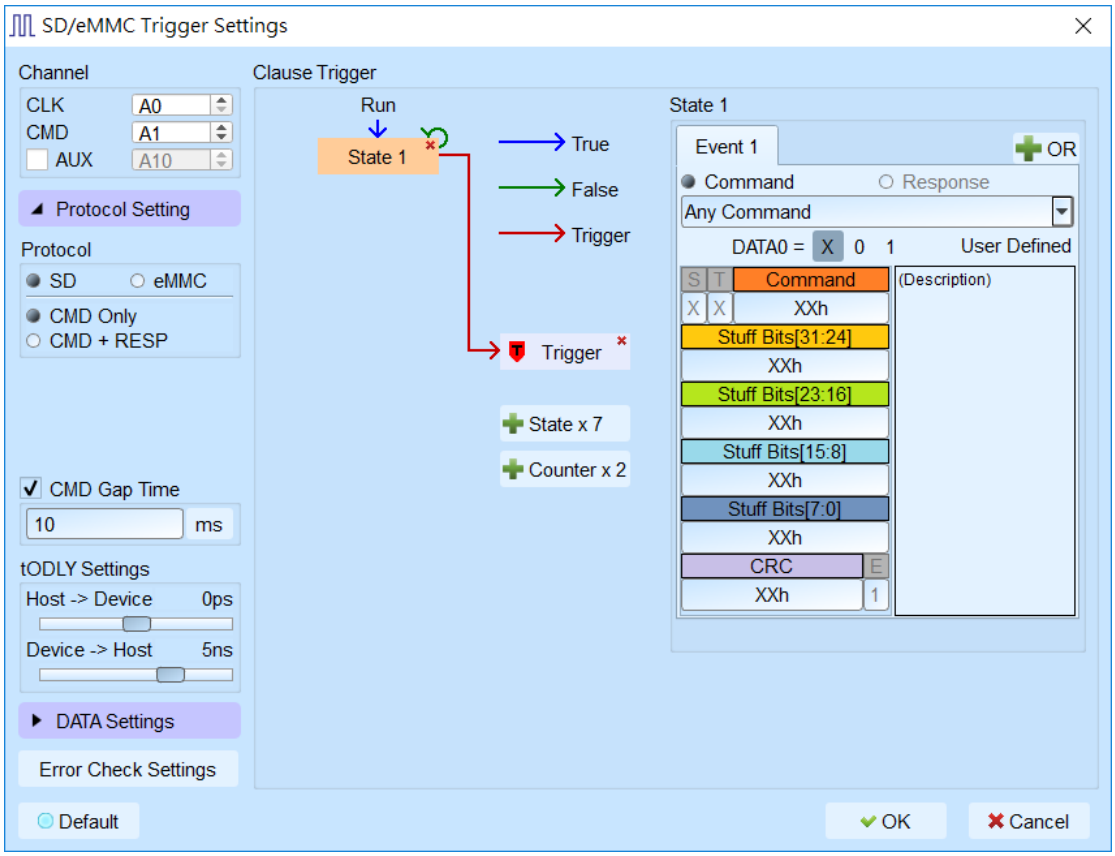
selecting the trigger values in the SD packet and its fields, default value is XX means “don’t care”.

SD/eMMC Trigger

Supported Models：TL3234B+. LA3068B. LA3136B. BusFinder (SD/eMMC solution)

SD/eMMC Trigger Settings

Click **SD/eMMC** Trigger in the toolbar and will show the dialog as the following。



1. **Channel:** select CLK, CMD as the trigger channel

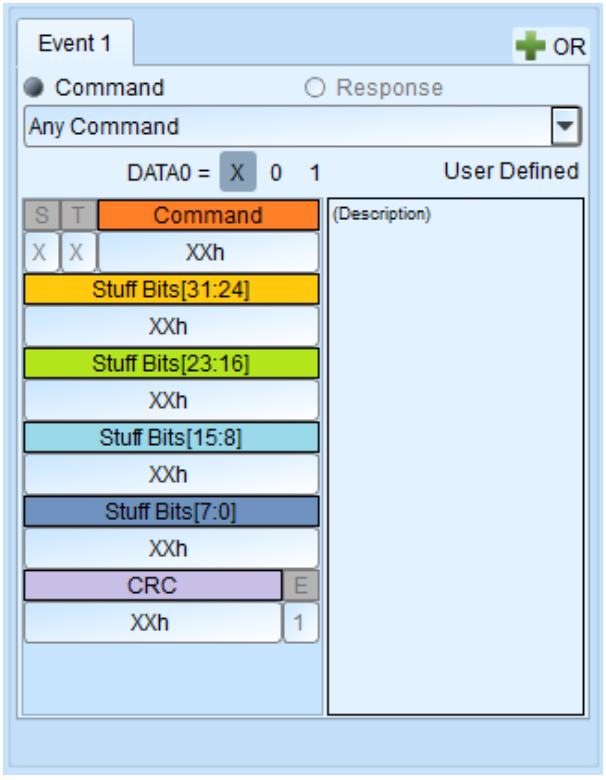
   AUX can be used for checking power state before running CRC error check, disabled by default.

2. **Protocol:** select SD or eMMC trigger
3. **CMD Gap time:** delay trigger between the two CMDs.
4. **tODLY Settings:** set the phase delay time such that the device can latch valid

command and response.

5. **Clause trigger settings:** Please reference Clause Trigger chapter

6. **Trigger settings**



Parameter：

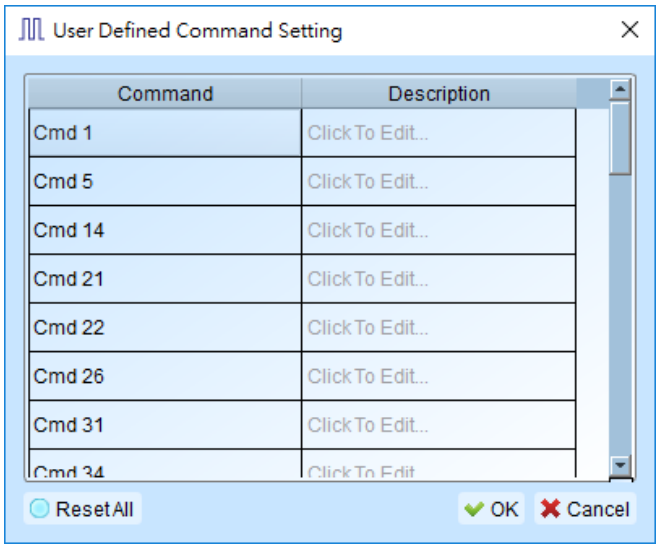
DATA0 = X 0 1 : use Data0 to judge the R1 and R1b.

Input trigger value, input ‘X’ means don’t care.

Append ‘h’ for HEX, ‘b’ for binary, no append for DEC.

When cursor on the input table, the information showed in the right side field.

User Defined add the command reserved:

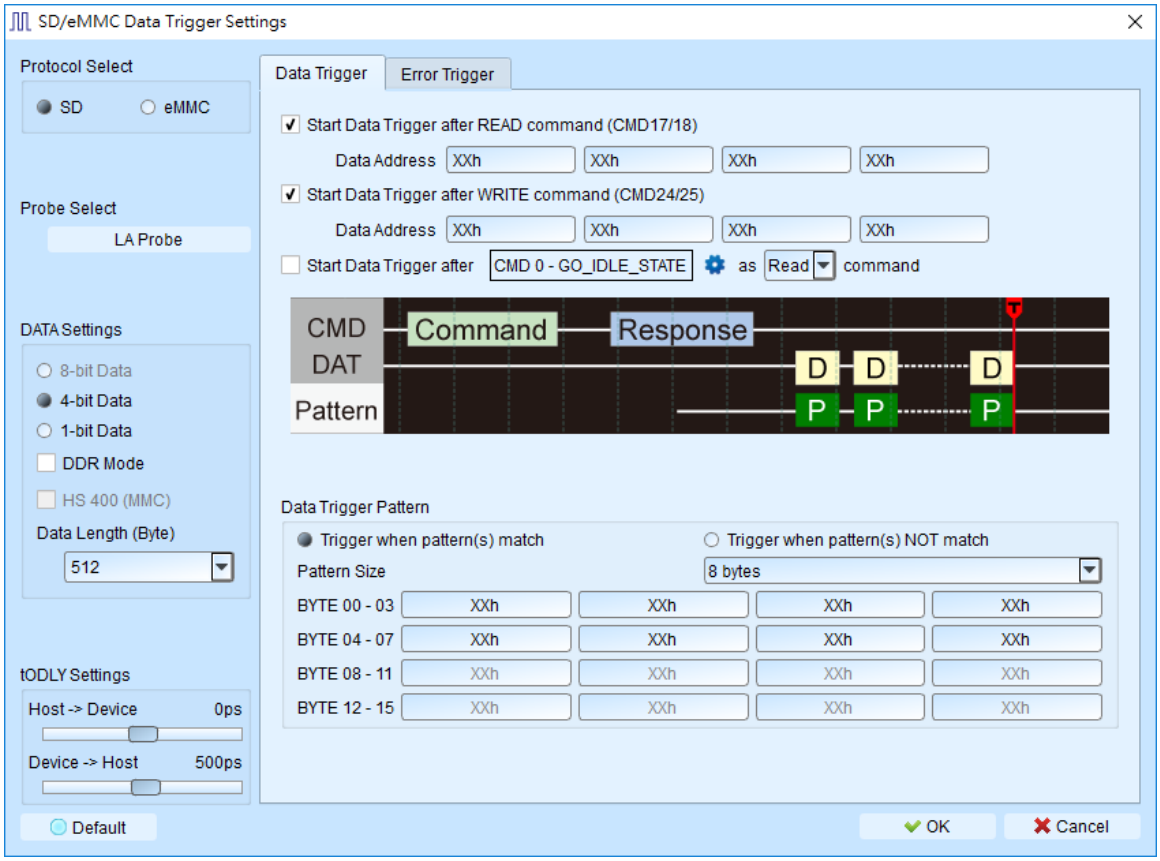


SD/eMMC Data Trigger

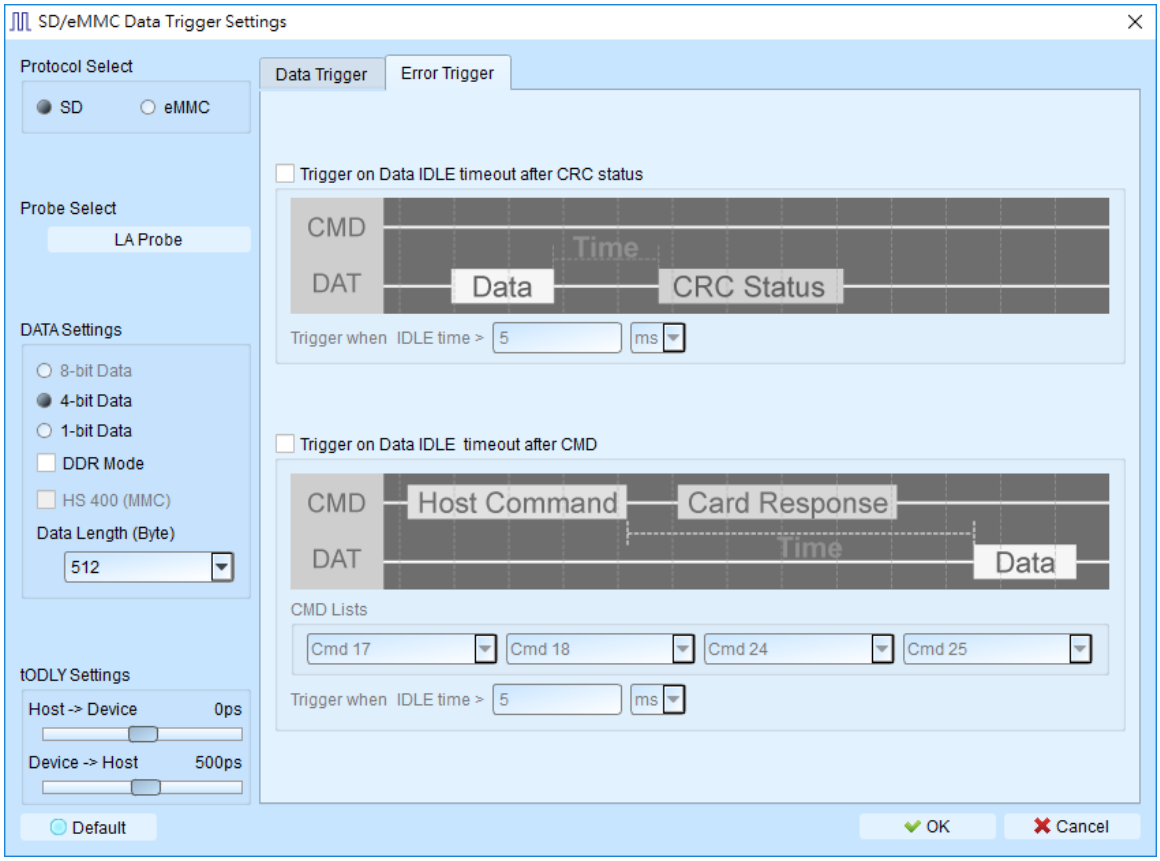
Supported Models：TL3234B+. LA3068B. LA3136B. BusFinder (SD/eMMC solution)

SD/eMMC Data Trigger Settings

Click **SD/eMMC Data** Trigger in the toolbar and will show the dialog as the following。



1. **Protocol:** select SD or eMMC trigger
2. **Probe Select:** select CLK, CMD and AUX as the trigger channel.
3. **Data Settings:** select current bus width, byte, SDR, DDR of the test object
4. **tODLY Settings:** set the phase delay time such that the device can latch valid command and response.
5. **Data Trigger:** set the patterns of data trigger.



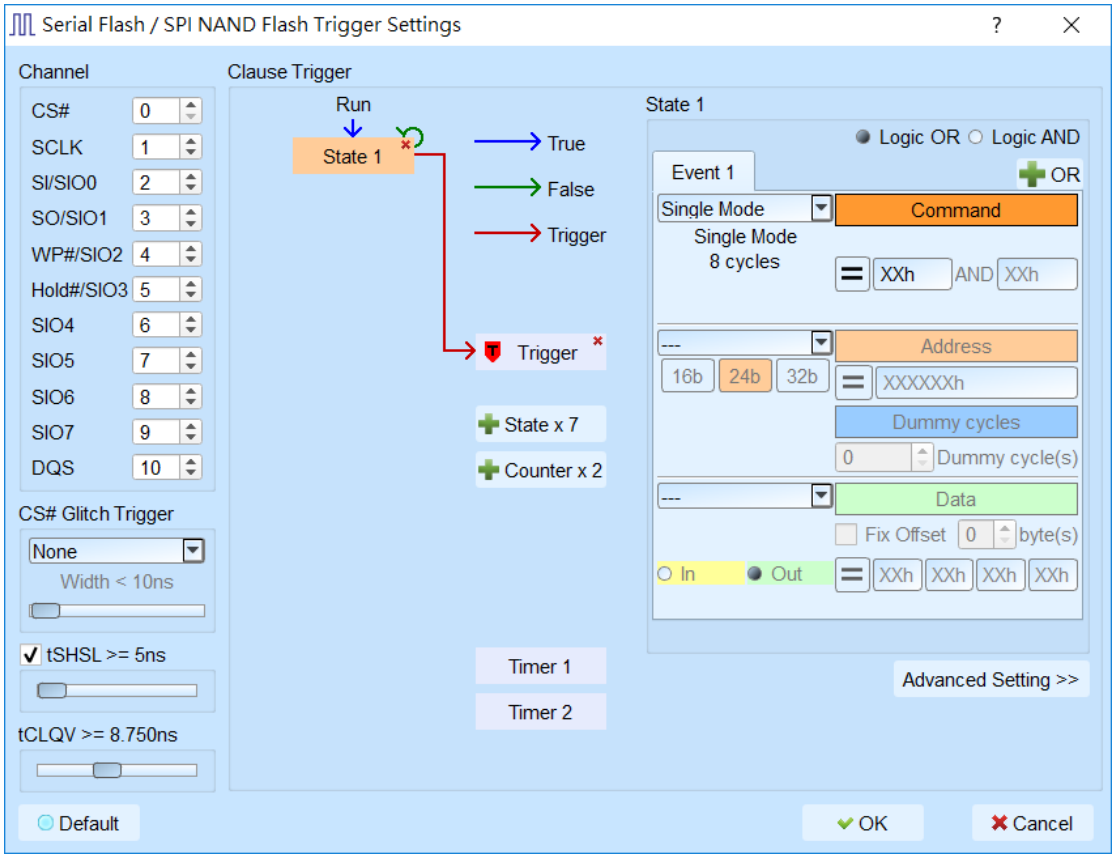
6. **Error Trigger:** set the condition of idle time to trigger.

Serial Flash / SPI NAND Trigger

Supported Models：TL3234B+. LA3136B. BusFinder series

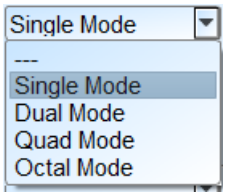
Serial Flash / SPI NAND Flash Trigger Settings

Click Serial Flash Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select channels.
2. **CS# Glitch Trigger:** Trigger the glitch on CS# channel.
3. **tSHSL / tCLQV:** Set tSHSL / tCLQV.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Command, Address and Data fields, default value is XX means “don’t care”.

   Provided the Single / Dual / Quad / Octal mode.



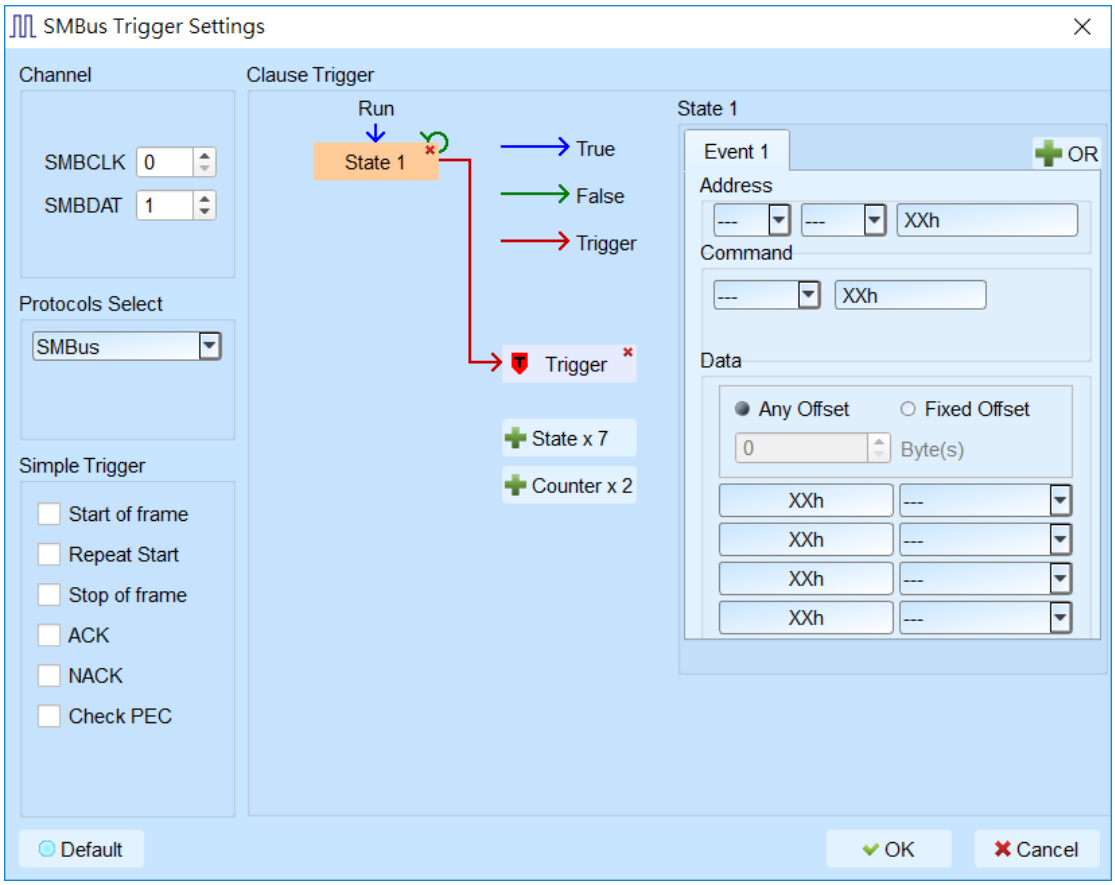
SMBus Trigger

Supported Models：TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+.

LA3068B. LA3136B

SMBus Trigger Settings

Click SMBus Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select I2C / LA port.
2. **Protocols Select:** Select SMBus / SBS / SPD protocol.
3. **Simple Trigger:** Specific trigger function of SMBus.
4. **Clause Trigger:** Please reference Clause Trigger chapter.

5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Address, Command and Data fields, default value is XX means “don’t care”.

   Data field only provided 4 bytes data to trigger, checking the Fixed offset and selecting the offset value when want to trigger at the specific position.

Note: Only TravelBus series provide I2C port channel

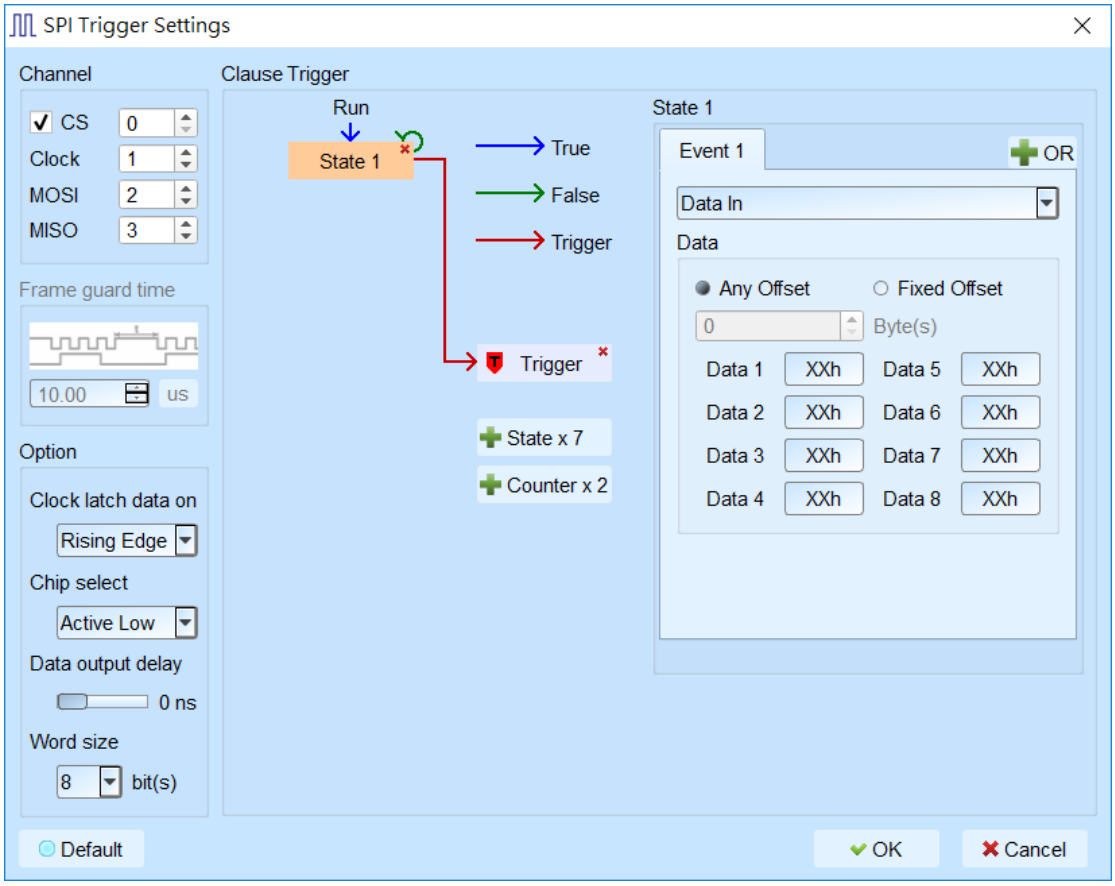
SPI Trigger

Supported Models：TravelBus series. TL3134E. TL3134B. TL3234B+.

Logic Analyzer series. BusFinder series

SPI Trigger Settings

Click SPI Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select SPI channels.

2. **Frame guard time:** Only for unchecked CS state.
3. **Option:** Set SPI parameters.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Data fields, default value is XX means “don’t care”.

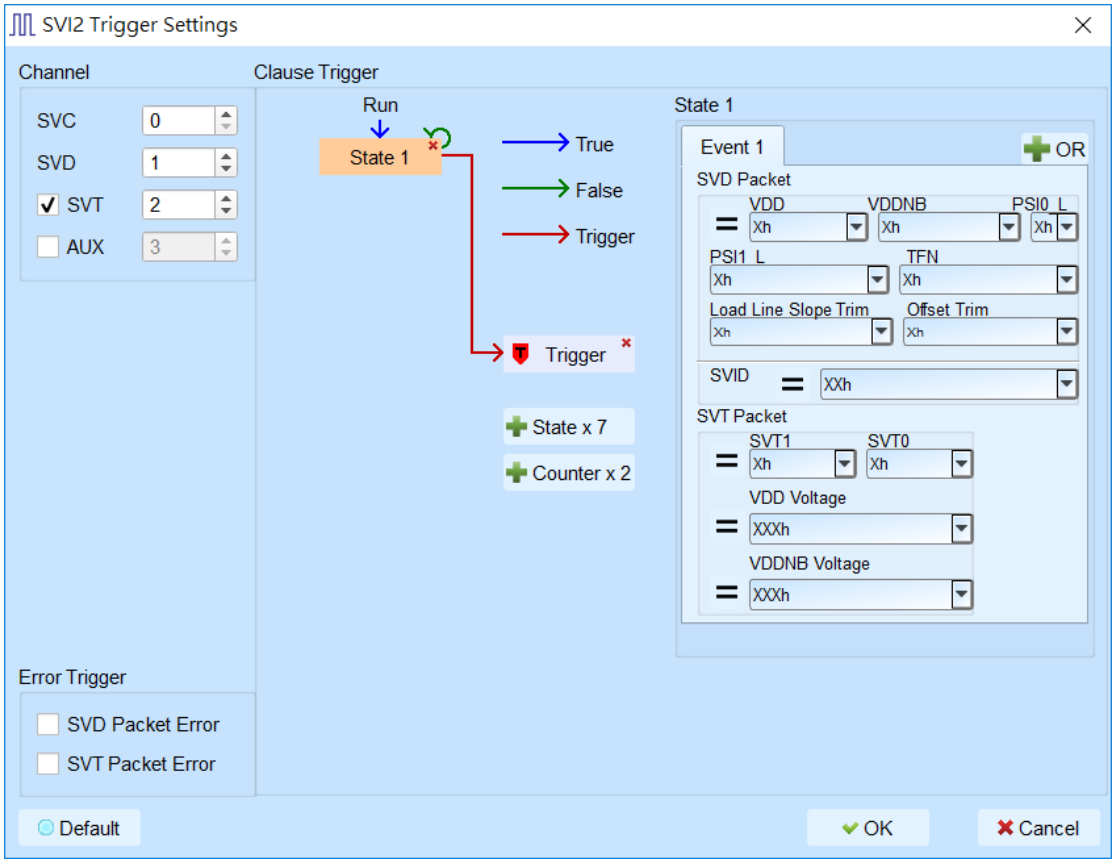
   Data field provided 8 bytes data to trigger, checking the Fixed offset and selecting the offset value when want to trigger at the specific position.

SVI2 Trigger

Supported Models：TL3134B. TL3234B+

SVI2 Trigger Settings

Click SVI2 Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select channels.
2. **Error Trigger:** Trigger specific error of SVI2.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the SVD and SVT packet, default value is XX means “don’t care”.

   When check the AUX, the trigger function will refer to the state of AUX (High/Low).

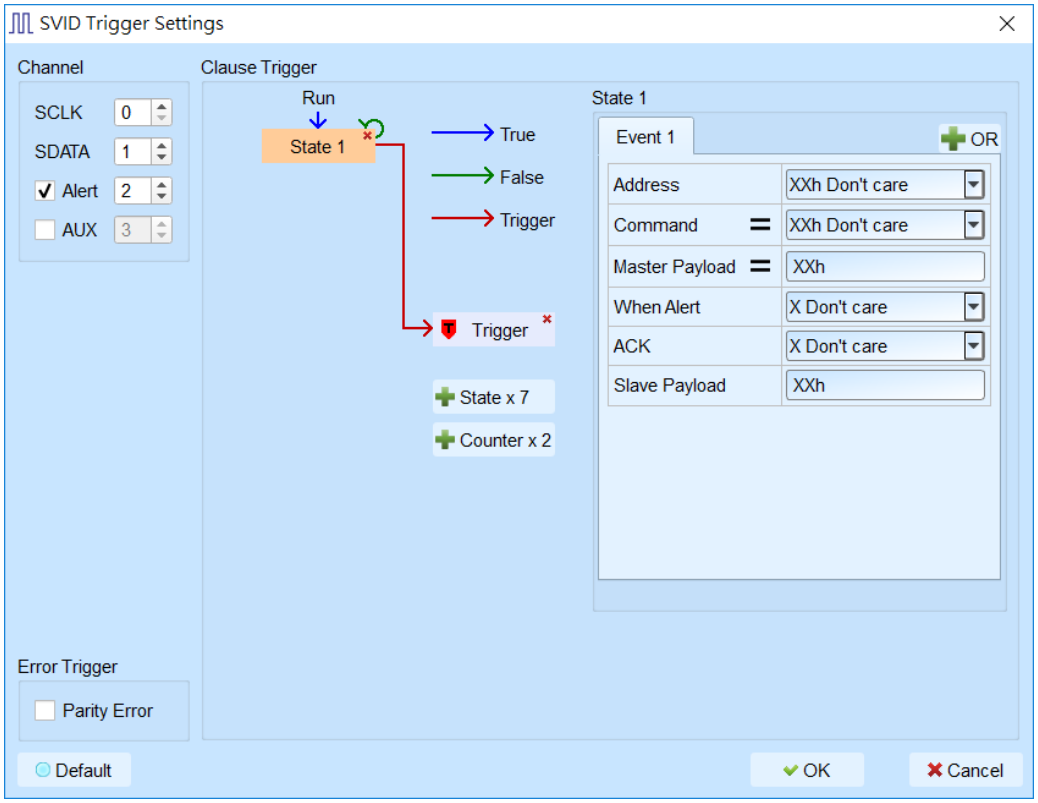
SVID Trigger (Upon Request)

Supported Models：TL3134B. TL3234B+. LA3068B. LA3136B

If you have any issues with SVID protocol features, please contact your Intel Field Representative.

SVID Trigger Settings

Click SVID Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select channels.
2. **Error Trigger:** Set SVID Parity Error trigger.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Address, Command, Master Payload, ACK and Slave Payload fields, default value is XX means “don’t care”.

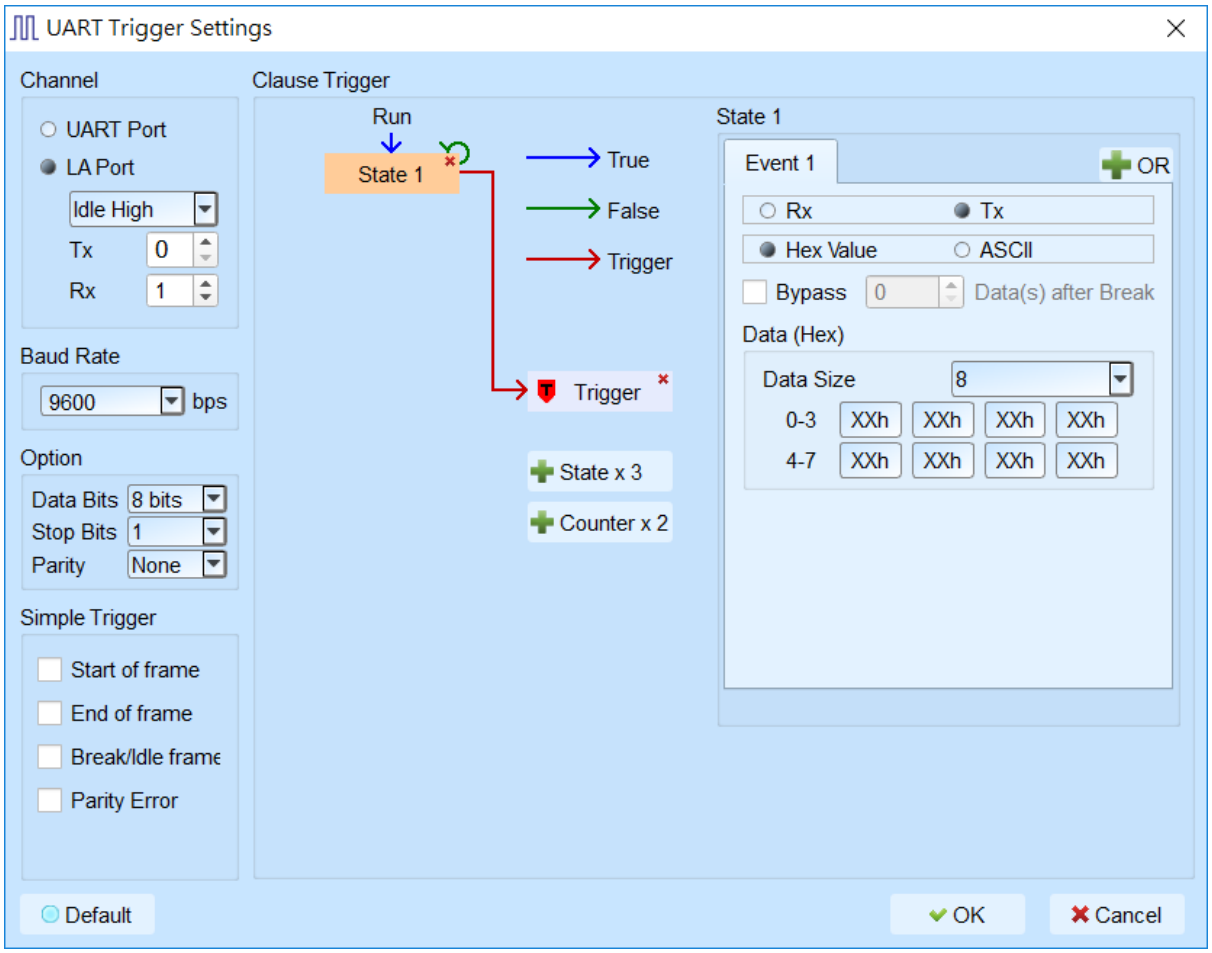
   When check the AUX, the trigger function will refer to the state of AUX (High/Low).

UART Trigger

Supported Models：TravelBus series. TL3134E. TL3134B. TL3234B+. Logic Analyzer series

UART Trigger Settings

Click UART Trigger in the toolbar and will show the dialog as the following.



1. **Baud Rate:** Select UART baud rate.
2. **Simple Trigger:** Specific trigger function of UART.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing the trigger values in the Data fields, default value is XX means “don’t care”.

Data field provided 16 bytes data to trigger, checking the Bypass and selecting the offset value when want to trigger at the specific position.

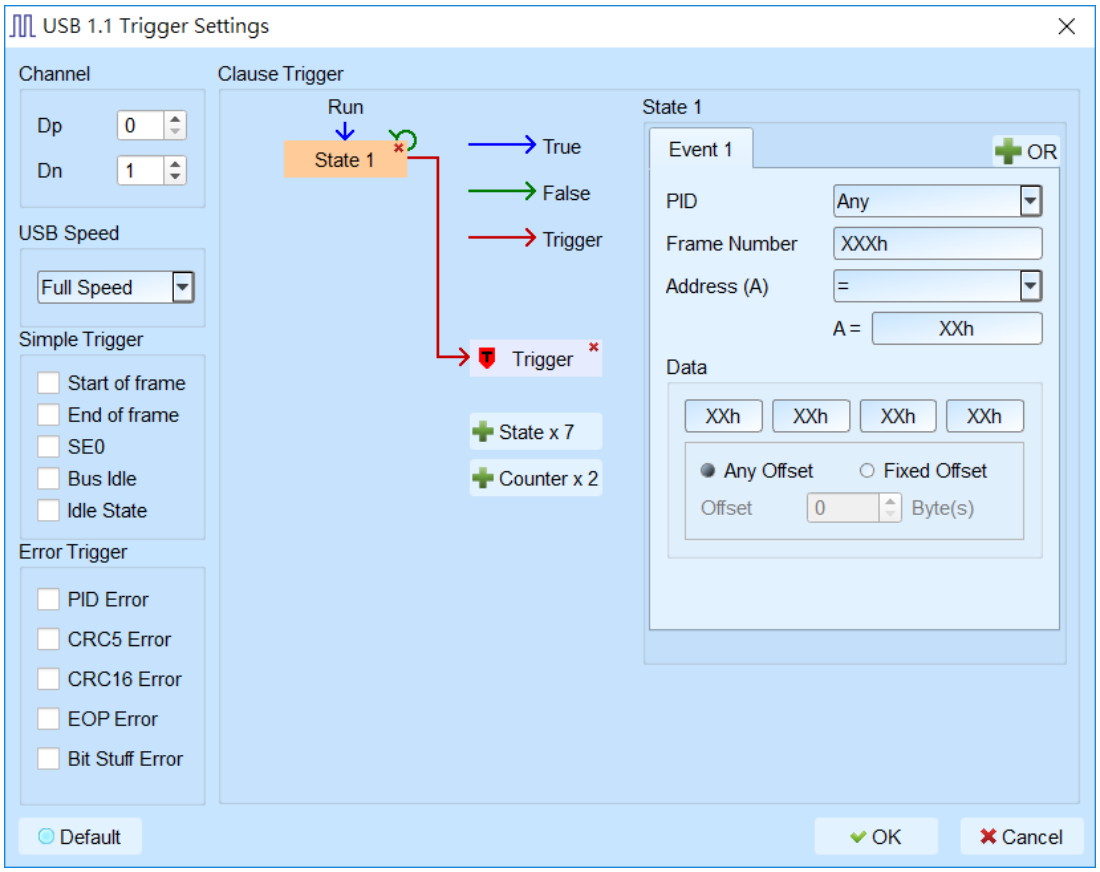
Note: Only TB1016B. TB1016B+ provide UART port channel

USB 1.1 Trigger

Supported Models：TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+. LA3068B. LA3136B

USB 1.1 Trigger Settings

Click USB 1.1 Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select channels.
2. **Simple Trigger:** Specific trigger function of USB 1.1.
3. **Error Trigger:** Trigger specific error of USB 1.1.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the PID, Frame Number, Address and Data Field, default value is XX means “don’t care”.

   Data field provided 4 bytes data to trigger, checking the Fixed Offset and selecting the offset value when want to trigger at the specific position.

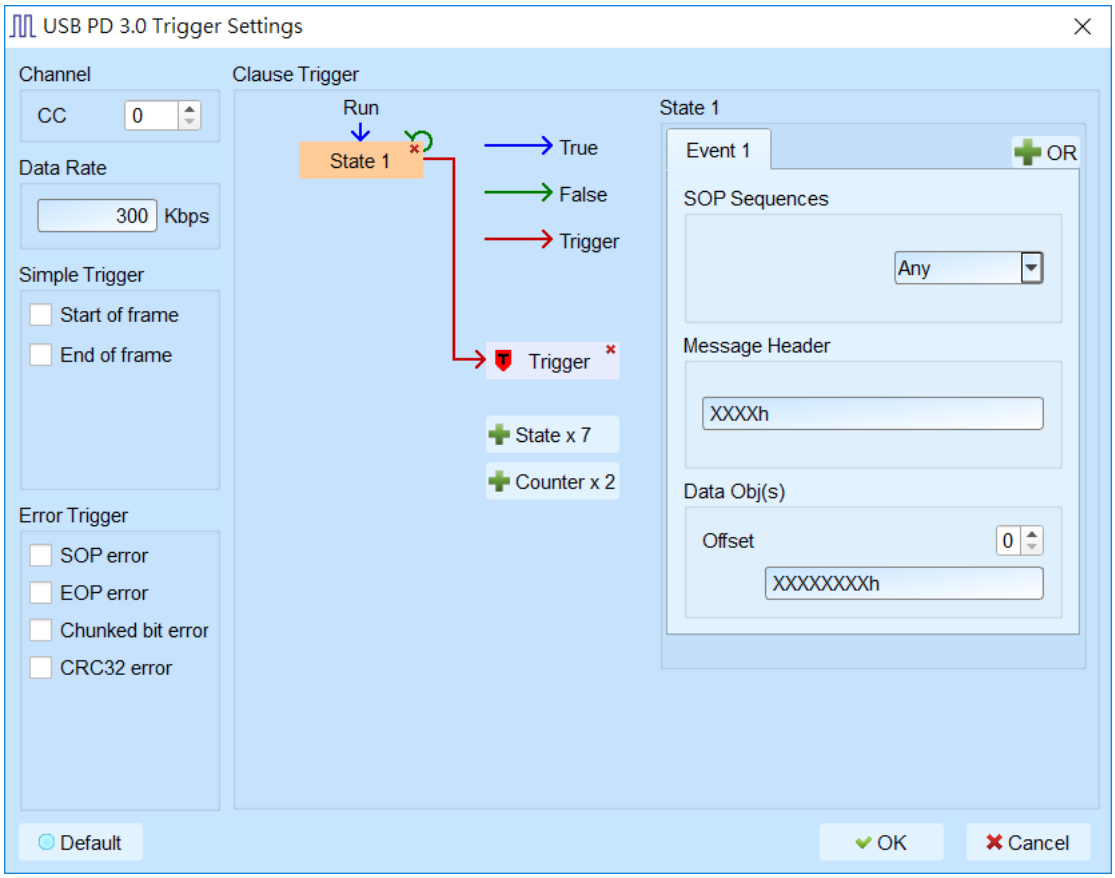
USB PD 3.0 Trigger

Supported Models：TB1016E. TB1016B. TB1016B+. TL3134E. TL3134B.

TL3234B+. Logic Analyzer Series

USB PD 3.0 Trigger Settings

Click USB PD 3.0 Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select channels.
2. **Simple Trigger:** Specific trigger function of USB PD 3.0.
3. **Error Trigger:** Trigger specific error of USB PD 3.0.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the SOP Sequences, Message Header and Data Obj(s), default value is XX means “don’t care”.

   Provide 0 ~ 7 offset value for Data Obj(s) field.