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Chapter 1 Bus Decode

Basic operation

Add a Bus Decode

Method 1:

Click the Quick Setting Ruse i

in the menu, and select the bus decode.

Acute BusFinder												
File Capture	Adv. Capture	Cursor										
	Setting	Sample Rate 200MHz (5ns)	Memory 2000 Mb - 16CH	HT Threshold	Run Repeat			Zoom -	Stack DSO PI	emo nase Delay 0 ps 👻		
ne/Div= 200 us	A	178.41 us	358.82 us	B) 535.24 us	713.65 us	892.06 us	C) 1.07 ms	1.25 ms	1.43 ms	1.81 ms	1.78 ms	1.96 ms
H-00	A0											
H-01	Al											
H-02	A2											
H-03	A3											
10 10												•

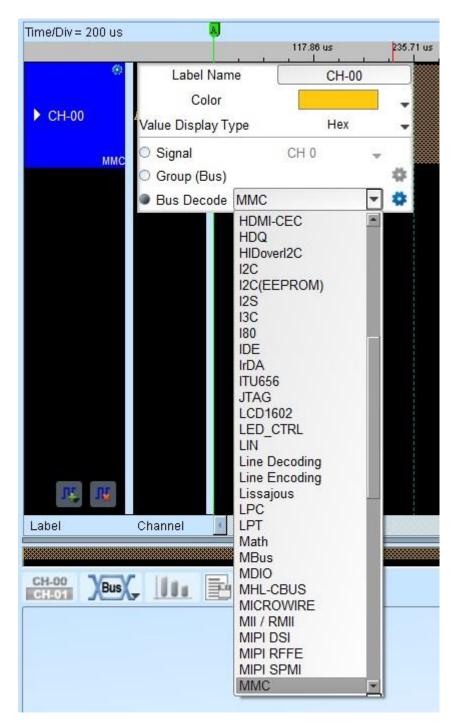
Method 2:

Click Add Bus Decode in the Label menu or right-click the label field to show the

dialog box.



Advance channel setting

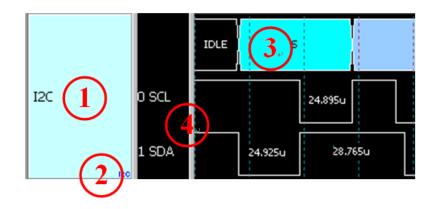


- **1. Bus Name:** Enter the label name with 31 characters or less. (Chinese word expresses two characters.)
- **2.** Color: Set the waveform color.
- 3. Display the waveforms with decode
- 4. Display the waveforms with its decode together.
- 5. Advance:



LTN SHE	tras 🗶
Channel	
;	Sunza Canzo Canaz
	Cardounimede P Dapais C Enhanced
	Lh Damed Of B
	final site A.T.S. 💌 Ign
Color —	
	Vekt-op
Range —	Decode Range From Buffer Head To Buffer Tail
	Default OK Cancel

Set the decode parameters or press **OK** to use default settings. There are "Channel", "Color", "Range" settings



- 1. Bus name
- 2. Decode type
- 3. Result
- 4. Channel name & signal

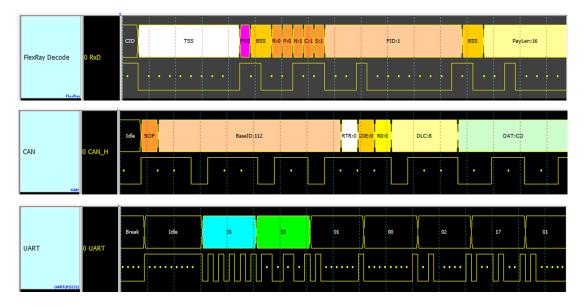


Specially Bus Decode:

The bus decodes display the data in text format, but some decodes are able to show the original form for the data such as voice (I2S decode...), image, analog waveform (ADC decode) etc.

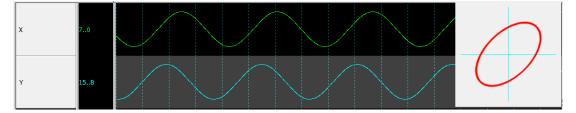
UART/CAN/FlexRay..bus decodes:

The data is displayed according to bit points in order to calculate the bit number \circ



Lissajous analysis (released in 2009/09, LA Viewer Ver.2.0):

Display the signal in graph by X-Y or I-Q data. •





S/PDIF analysis:

Display the data in sound waveform $\,\circ\,$

S/PDIF(wave) 0 S/PDI	Min: -5766	00: 1:17.96 00:00: 1:19.19 00:00: 1:20.42 00:00: 1:21.65 0	30000 -10000 -10000 -10000 -10000 -2000 -200 -2000 -
Setting Channel O.0000 (384Kb/s~12 Display th	▼ Mb/s	Block 192 (32 ~192) frames Bit Order Aux. Data LSB first Audio Data LSB first	Data Bits 16 Parity mode Even parity Playback

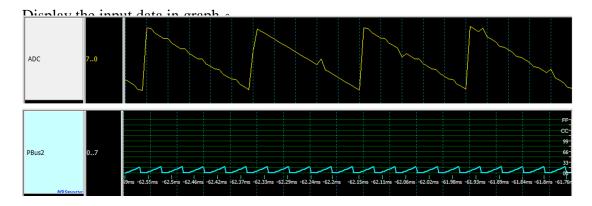
I2S analysis:

Display the data in sound waveform $\,\circ\,$

125 02 Min: -10500 Min: -20004 Min: -20004 Min: -20004 Min: -20004 UI	30000 30000
Channel	
Clock Channel	(SCK) CH 0 -
Word Select Channel	(WS) CH 1 -
Data Channe	el (SD) CH 2
Da	ta bits 16 Bits
Display the audio wavef	orm 🔽 Playback
Mode	Report
I2S Justified Mode	▼ 8 Column ▼

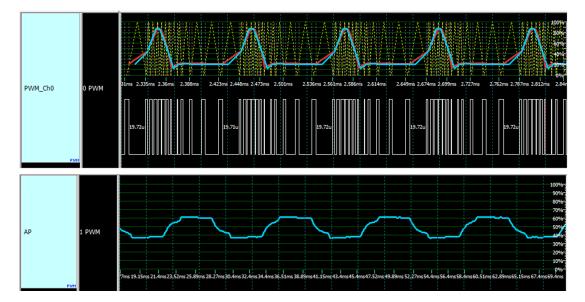


ADC bus decode:



PWM analysis:

Restore and display the data in the waveform window as percentile or frequency \circ





1-Wire

The 1-Wire bus has data bits (Reset Pulse, Presence Pulse, Write 1, Write 0, Read 1, Read 0) in standard or overdrive speed as the diagram below.

Settings

	ttings			×
Channel -				
2	Communicatio	n Speed	Bit Order	
:	Standard	~	LSB First	~
	Sampling Point	t		
	35	us	, →	
	Setting the cha	nnel of 1-w	ire in LA CH 0	
Color —				
	Set color of dat	a		
	Set color of dat Reset Pulse	a		_ ~
				· ·
	Reset Pulse			
nange –	Reset Pulse Presence Pulse			· ·
Range –	Reset Pulse Presence Pulse			
Range –	Reset Pulse Presence Pulse Data		ad	
Range –	Reset Pulse Presence Pulse Data Decode Range		ad	*

Communication Speed: Standard or overdrive.

Bit Order: LSB first or MSB first.

Sampling point: Set the sampling point N microseconds (us) after the beginning of

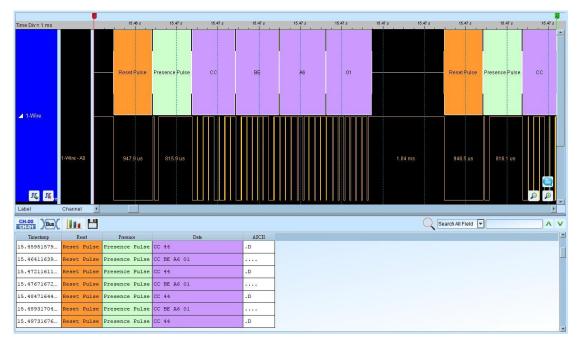
each data bit.



Result

Click OK to run the 1-Wire decode and see the result on the Waveform Window

below.





3-Wire

3-Wire protocol is established by HOLTEK SEMICONDUCTOR INC. It's Applied to control LED/LCD driver IC or EEPROM.

Settings

3-Wire (H	OLTEK) Settir	ngs			×	
Parameter	rs Channel CS A0 • WR A1 • WR A1 • MR A3 • DATA A2 • Application • LED Driver IC			OPERATION ADDRESS COMMAND DATA START		
	CLED DI CLED DI CEEPRO HT 1620x HT 93LC4 x8	iver IC		Decode Range From Buffer Head V	To Buffer Tail ──	
	Latch Chip Select E O Active H Data Edge () Rising		Low			
				Default	OK Cancel	

Channel: Show the selected channels (CS:CH0, WR:CH1, DATA:CH2, RD:CH3)

LED Driver IC: Select LED driver IC application.

LCD Driver ID: Select LCD driver IC application.

EEPROM: Select EEPROM application.



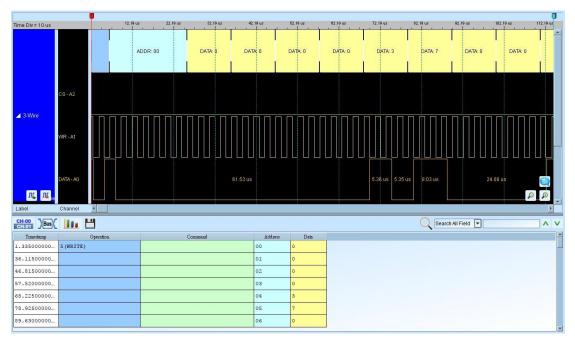
Active High: Select Active High.

Active Low: Select low chip select (CS).

Rising: Select Rising Data Edge.

Falling: Select Falling Data Edge.

Result





7-Segment

A seven-segment display, is a form of electronic display device for displaying decimal numerals that is an alternative to the more complex dot-matrix displays.

Digit	LED	А	В	С	D	E	F	G
0	F G B C C D DP	ON	ON	ON	ON	ON	ON	OFF
1	F G B E C D DP	OFF	ON	ON	OFF	OFF	OFF	OFF
2	F G B E C D DP	ON	ON	OFF	ON	ON	OFF	ON
3	F G B E C D DP	ON	ON	ON	ON	OFF	OFF	ON
4	F G B F C D DP	OFF	ON	ON	OFF	OFF	ON	ON
5		ON	OFF	ON	ON	OFF	ON	ON
6	F G B E C C D DP	ON	OFF	ON	ON	ON	ON	ON
7	F G B F C D DP	ON	ON	ON	OFF	OFF	OFF	OFF
8	F G B F C C D DP	ON						
9		ON	ON	ON	ON	OFF	ON	ON



Settings

7-Segr	ment Se	ttings						×
Chann	nel –				[A	
A	A0	-	E A	4	•	F		в
В	A1	-	FA	5	-	- I	G	
С	A2	-	GA	6	-	е 🚺		с
D	A3	-		0	A	- I_		
Range	• •	of data [¥		
		e Range						
	From		153	To	- 1		1000	
	Buffe	r Head	~	Buffe	er Tail		~	
				Default		OK		Cancel

Channel: Show the selected channel (CH 0).

DP: to analysis decimal point.

Common cathode/anode: Show the same cathode or anode.



Result

Click **OK** to run the 7 Segment decode and see the result on the Waveform Window

below.

		9	-8,4		-7.9 us		-7.4 us) us	-6.4 us		-6.9 us	-5.4		-4.9 us		-4.4 us		9 us	-3.4 us
ime Div= 500 ns			r <u>* * </u> †					1			(<u> </u>		r <u>i i (</u>					(<u> </u>	<u> </u>	
		9.	Unknown	8	Unknown	A	Unknown	1.	Unknown	2.	Unknown	3.	Unknown	4.	Unknown	5.	Unknown	7.	Unknown	b.
	A- A0		300 ns	300 ns	300 ns	300 ns		900 ns		300 ns	300 ns	300 ns		900 ns		300 ns	300 ns	300 ns		
	B - A1		300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns		900 ns		300 ns		
	C - A2		300 ns	300 ns	300 ns	300 ns	300 ns	300 ns		900 ns		300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	
PBus1	D - A3		300 ns	300 ns			1.5 us			300 ns	300 ns	300 ns		900 ns		300 ns		900 ns		
	E - A4				300 ns	300 ns]	900 ns		300 ns					2.7 us					
	F - A5		300 ns	300 ns	300 ns	300 ns				2.1 us				300 ns	300 ns	300 ns		900 ns		
	G - A6		300 ns	300 ns	300 ns	300 ns		900 ns		300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns		900 ns		
л, л	DP - A7					300 ns	300 ns	300 ns	300 ns	300 ns			300 ns			300 ns	300 ns	300 ns	300 ns	0 0
Label	Channel	4																		,
CH-00 Bus		Ľ													Q	Search	All Field 🔻	•		^
Timestamp	A		В		с	D		E		F	G		DP	V	alue					
-9us		1		1		i	1		0		1	1		1						
-8.4000000		1		1	1	i.	1		1		1	1		0						
-7.8000000		1		1		L	0		1		1	1		1						
-7.2000000		0		1			0		0		0	0		1						
	-			122	- 1	5	1		1		0	1		1						
-6.6000000		1		1		·	-													
-6.6000000		1		1		í	1		0		0	ī		1						



A/D Converter

A/D Converter (Analog-To-Digital Converter), is a device that uses sampling to convert a continuous quantity to a discrete time representation in digital form.

Settings

A/D Conv	verter Settings		×
Paramete	Channel Data Channel Data Width Channel Start From	8 Bit ✓ A2 ← ✓ CS(OE) Channel A1 ←	Draw Curve:Time(X)-Data(Y) Ramp Function Step Function
	Data MSB First Chip Select Edge Data Edge	2's Complement Active High Rising Falling	Use the maximum and minimum as the bound of Y axis Insert Y axis bound(Save it in the LA work directory) Top(Decimal) 255 Bottom(Decimal) 0
Color Color Range	DATA	· ·	
	Decode Range From Buffer Head	To V Buffer Tail V	Default OK Cancel

Data Channel Start From: ADC data channel start from

CLK Channel: ADC clock in channel

CS(OE) Channel: ADC chip select (output enable) channel

Data Width: ADC data width, range: 4Bit ~ 32Bit

MSB First: Data bit starts form MSB; LSB defaulted

2's Complement: Show the 2's complement result.

Chip Select Edge: Set the chip select edge; Active Low defaulted

Data Edge: Set the Data Edge; Falling Edge defaulted

Curve: Time(X)-Data(Y) Show the diagram in form of time as X axis; data as Y

axis.



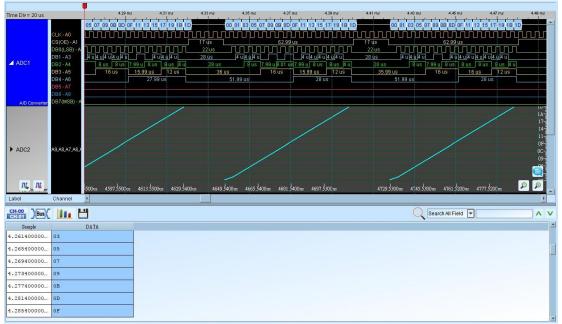
Ramp/Step Function: Select Ramp/Step curve, Ramp Function defaulted Color: Select the curve color

Use the maximum and minimum as the bound of Y axis: Use the maximum data as the top bound of Y axis and minimum data as the bottom bound of Y axis. **Insert Y axis bound:** Set the maximum and minimum bounds of Y axis.

Note: When Insert Y axis boundaries is actived (Save it in the LA file directory), the Top and Bottom values will always be saved as an independent text file named as ADC.txt, different from the waveform file, at file work directory unless a different name is assigned. If you need the specific boundary settings, please save it, so you can reload the settings next time.

Result

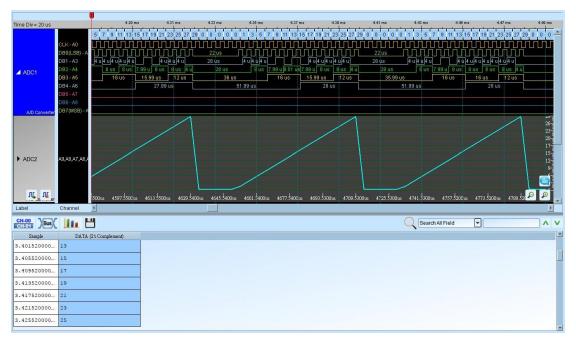
Click **OK** to run the A/D Converter decode and see the result on the Waveform Window below.



Select 8-bit data, CLK/CS channels:



Select 8-bit data:





AcceleroMeter

AcceleroMeter (AccMeter) decoder is the SPI interfaced accelerometer data decoder, which provides bus value to acceleration value conversion and curve drawing function.

Settings

AccMe	ter Settir	ngs				×
Parame	ter Settin	gs	2			
	Chann	el Setting	js	Edge S	elect	
1	CS	A0		CS	Active Low	~
	CLK	A1	•	SDI	Rising	~
	SDI	A2	•	SDO	Rising	~
	SDO	A3	•			
	Model	AIS326	DQ ~			
	Plo Ad	v Settings t: Time (vanced E culate A	X) - Dat Decode		X Y	z
Color	-	-				
	R/M Address				M/S	
Range	-					
2	Decode R From	ange		То		
	Buffer H	ead 🗸	•	Buffer Ta	il 🗸 🗸	
		1	Default	0	Car	ncel

CS: Chip Select, must specified the active state of the CS pin.

CLK: Clock

SDI: Data Input Pin, must specified the data sampling edge.

SDO: Data Output Pin, must specified the data sampling edge.

Model: The IC model of the target accelerometer.



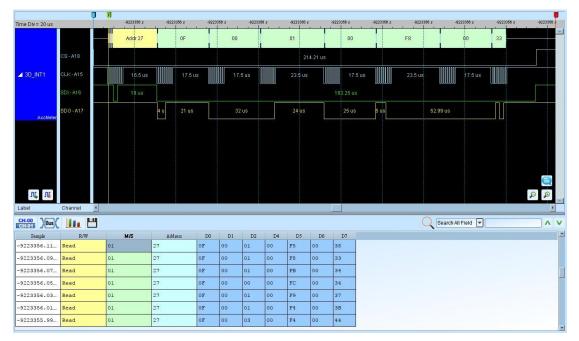
Initial Full-Scale: The default Full-Scale setting.

Plot: Enable/Disable to display the waveform in Time-Value curve.

Advanced Decode: Enable/Disable the address, value convert function.

Result

Standard decoder result



Advanced decode result + Time-Value curve display





AD-Mux Flash

AD-Mux Flash is one kind of parallel flash that utilize an Address and Data multiplexed interface.

Settings

hannel			Configuration					
Amax A22 V	ADQ[0](LSB)	A7	Wait State			Burst	t Length	
				13th	\sim	Con	tinuous	~
O Quick Setup			RDY Polarity					
User Defined	A[22:16] =			high	\sim	RDY	active	
			Burst Wrap Aro	und		with	i data	~
Flash				Yes	~			
CE#f A24	▲ AVD#	A23 🔹	Color		Rang	e		
OE# A29	CLK	A26 •				L Decod	led Range	
WE#	 RDYf/WAITp 	A30 +	Address		Fron		Buffer Head	~
PSRAM			Burst Address				burrer fredu	
has PSRAM	LB#p	A28 🔺	Read Data		то Т v		Buffer Tail	~
CE#p A25	UB#p	B0			<u> </u>			

Amax: Setting the number of address pin.

Quick Setup/User Defined: Only set ADQ[0](LSB) when select the Quick Setup,

other channels will be set automatically. When check User Defined and press the

ADQ[0]							×
	A7 •	ADQ[8]	A21 •	A[16]	A0 +	A[24]	A0
ADQ[1]	A8 🔺	ADQ[9]	A22	A[17]	A1 +		
ADQ[2]	A15 +	ADQ[10]	A9	A[18]	A2 +		
ADQ[3]	A16 +	ADQ[11]	A10	A[19]	A3 •		
ADQ[4]	A17 +	ADQ[12]	A11	A[20]	A4 •		
ADQ[5]	A18	ADQ[13]	A12 +	A[21]	A5 🔶		
ADQ[6]	A19 •	ADQ[14]	A13 +	A[22]	A6 +		
ADQ[7]	A20	ADQ[15]	A14	A[23]	A0		

button will show the dialog below:



Flash: Control pins of flash.

PSRAM: Control pins of PSRAM. Some MCP include Flash and PSRAM in one package. It will decode PSRAM at the same time when "has PSRAM" is checked. **Configuration:** The default setting of configuration register. User must set here to make a correct analysis.

Result

Click OK to run the AD-Mux Flash Decode and see result on the Waveform Windows

Time Div = 10 ns		2.27 us	2.28 us	2.29 us	2.3 us		2.31	us	2	.32 us		2.33 us		2.34 us		2.3	6 us	:	2.36 us	
						- L - L					1 1		1		1 1			1		1
Address/Data	A6:A6																			
AVD#	A23														_			10 ns	Γ	
CE#f	A24											İ		i i						
CE#p	A25																			
CLK	A26	6 ns 6 ns 4	ns 6 ns	4 ns 6 ns	6 ns	4 ns	6 ns	4 ns	61		6 ns	4 ris		4 ris			hs		8 ns	
CREp	A27																			
.B#p	A28												32 ns	3 <u>(</u>						
DE#	A29													1						
RDYf/WAITp	A30				8					-									_	
RESET#f	A31																			
UB#p WE#	80				_		_						32 ni	8						
) Bus 1	B0,A28,A3	5 A FB_R:E59F	FB_R:0800	FB_R:E1A0	FB_R:1	000	FB_R	:E594										10 ns	Q	
JL,	L L sh BO,A28,A3 Channel	25 A FB_R E59F	FB_R:0800	FB_R:E1A0	FB_R:1	000	FB_R	:E594										10 ns		Q
_abel	Channel	75 A FB_R:E59F	FB_R:0800	FB_R:E1A0	FB_R:1	000	FB_R	:E594					C	Seal	rch All Fi	ield 🔻		10 ns		Ø
.abel	Channel	FB_R £59F	FB_R:0800	FB_R:E1A0	FB_R:1	000	FB_R D2	:E594 D3	D4	D5	D6	D7	D8	Seat	rch All Fi D10	ield 💌 D11	D12	10 ns		
AL Label CH-00 CH-01 DBus Timestamp	Channel						D2	D3	D4 FFE7	D5 EBFF	D6 FFD4	D7 EBFF	Contract of the	D9	D10				Q	
Label CH-00	Channel		Address	R/W	DO	D1 E92D	D2 0017	D3 EB00	The states of	and the second second	Louisver	Las an start	FEB1	D9 EBFF	D10 4048	D11 E59F	D12	D13 E1A0	D14	D15
.abel CH-00 Bus Timestamp 0.066000000	Channel Channel Device Flash		Address 033830	R/W Sync.Read	D0 4010	DI E92D	D2 0017 0020	D3 EB00 E59F	FFE7	EBFF	FFD4	EBFF	FEB1 F20F	D9 EBFF EBFF	D10 4048	D11 E59F E59F	D12 0800	D13 E1A0	D14 1000	D15
Abel CH-00 C	Channel Channel Device Flash PSRAM		Address 033830 023800	R/W Sync.Read Sync.Write	D0 4010 F213	DI E92D EBFF	D2 0017 0020 1040	D3 EB00 E59F E201	FFE7 F211	EBFF EBFF	FFD4 001C	EBFF E59F	FEB1 F20F 0000	D9 EBFF EBFF E350	D10 4048 0018	D11 E59F E59F 0BFF	D12 0800 4008	D13 E1A0 E8BD EBFF	D14 1000 F20C	D15 ES94 EAFE
ALE abel CH-00 Timestump 0.066000000 0.588000000 0.588000000	Channel Channel Device Flash PSRAM Flash		Address 033830 023800 033840	R/W Sync.Read Sync.Write Sync.Read	D0 4010 F213 0820	DI E92D EBFF E1A0	D2 0017 0020 1040 1D01	D3 EB00 E59F E201	FFE7 F211 1003	EBFF EBFF E381	FFD4 001C 1000	EBFF E59F E584	FEB1 F20F 0000 1B01	D9 EBFF EBFF E350	D10 4048 0018 FEA6 1C01	D11 E59F E59F 0BFF	D12 0800 4008 FEA7	D13 E1A0 E8BD EBFF E92D	D14 1000 F20C 0800	D15 E594 EAFF E1A0 EB00
CH-00 CH-01 CHL01	Channel Channel Device Flash PSRAM PSRAM		Address 033830 023800 033840 023810	R/W Sync.Read Sync.Write Sync.Read Sync.Write	D0 4010 F213 0820 1801	DI E92D EBFF E1A0 000F	D2 0017 0020 1040 1D01 0820	D3 EB00 E59F E201 000F E1A0	FFE7 F211 1003 1901	EBFF EBFF E381 000F	FFD4 001C 1000 1A01	EBFF E59F E584 000F	FEB1 F20F 00000 1B01 1004	D9 EBFF EBFF E350 000F	D10 4048 0018 FEA6 1C01 0000	D11 E59F E59F OBFF 000F	D12 0800 4008 FEA7 4010	D13 E1A0 E8BD EBFF E92D	D14 1000 F20C 0800 0017	D15 EAFF



Advanced Platform Management Link (APML)

APML protocol is established by AMD for it's Opteron CPU platform.

Settings

APML Se	ettings			×
Paramet	ter		Color	
	Channel SCL SDA	A0 •	Command Address Write / Read Start / Stop / Sr	
	Address 7-bit addressing	(Indude R/W in Address)	ACK / NACK PEC / Byte Count /Word Data	· · ·
Range	Ignore glitch Decode Range From	То		
	Buffer Head \checkmark	Buffer Tail 🛛 🗸 🗸		
			Default	OK Cancel

Channel: Show the selected channels (CS:CH0, WR:CH1, DATA:CH2, RD:CH3)

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit

addressing and 1-bit R/W).

PEC: Packet Error Check.

Ignore glitch: Ignore the glitch when the slow transitions.



Result

Time Div = 50 us		-500 us -460 us	-400 us -3:	350 us -300	us -250 us -20	00 us -150 us	-100 us	-50 us 0 ps
		S	3_TSI(4C) V	WrA	Data:SBTSL_x01(01)	A		s
APU-SIC	SCL-A0						199.93 us	
ΛĻ ΛL _L	SDA-A1 Channel 4	21.95 U	5.95 us 21	11.47 u			189.94 us	
							Search All Field 💌	
CH-00 Bus							Search All Fleid	
Timestamp -479.960000	Address SB-TSI (4C)	Value SBTSI_x01(01)	CPU	J Temperature H	Description	n		
Ops	SB-TSI (4C)	CpuTempInt (07)		J Integer temp.	10 10 10			
49.51592500	SB-TSI (4C)	SBTSI_x01(01)			ligh Byte Register			
49.99588500	SB-TSI(4C)	CpuTempInt (07)	CPU	J Integer temp.	7			
99.51181500	SB-TSI (4C)	SBTSI_x01(01)	CPU	J Temperature H	ligh Byte Register			
99.99177500	SB-TSI (4C)	CpuTempInt (07)	CPU	J Integer temp.	7		11	
149.5077000	SB-TSI (4C)	SBTSI_x01(01)	CPU	J Temperature H	ligh Byte Register			



BiSS-C

BiSS-C (Bidirectional Synchronous Serial C-mode) designed by Ic-Haus. The BiSS Interface is based on a protocol which implements a real time interface. It enables a digital, serial and secure communication between controller, sensor and actuator. It is used in industrial applications which require transfer rates, safety, flexibility and a minimized implementation effort.

Settings

BiSS-C Setting	×
Channel	Color
Single Cycle Data	Start
Serial data length (bits) 12	Data/Cmd
	Flag/IDL/ID
Range	CRC V
From Buffer Head V	Stop/Ex V
To Buffer Tail 🗸	Write/IDA
	Default OK Cancel

MA/SLO: Setting the channel of MA and SLO.

Type of data: Setting the type you want to decode. It include "Register Data-CDM",

"Register Data-CDS", "Single Cycle Data".

Serial data length(bits): Setting the data length when Single Cycle Data mode.



-

Result

1me Div = 1 us		173.2 m	s 173.2	ms 173.2 m	۶ 	173.2	ms	17:	3.2 ms		173.2 ms		173.2 m	ы. 	173.	2 ms	17	3.2 ms		173.21 ms		173.21 m
SCD BISS-C	A1,A0		A	S CDS:0						D:000							F:3			CRC:3	IA	
CDM BISS-C	A1,A0	Reading									s											
		CRC:7									P											
⊿ CDS	MA-A0								-													
1# 1# C	SLO-A1		425 ns	445 ns					5.65	us								2.19	us		42° 🔎	
	Channel •														_)
CH-00 Bus	111																earch All	Field	•			^
Sample	CIS	ID(IDS)	ADR (CMD)	R/W	DO	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15		
19.0656250	1	0	OF	Read	00	40	80	80	00	0A	00	82	00	00	00	00	00	00	00	00		
21.3059250	1	0	lF	Read	00																	
233.1228400	1	0	42	Read	2C	0C																
262.5506200	1	0	78	Read	4D	48	59	20	00	00	00	00										
317.3331600	1	0	76	Read	1F	00																
517.5551000					1		1	-			-	1	1	-	-	-		1	1			
	1	0	7D	Read	00	00	00															

Click OK to run the BiSS-C Decode and see result on the Waveform Windows below.



BSD

BSD(Bit Serial Device) is a serial communications protocol for battery monitoring in automotive application.

Settings

D Settings					0
Channel	a A0	-	Color	DIR	
	te Auto	~		Address Data	
Bitra					
Range Deci	ode Range				
From	Buffer Head	~	То	Buffer T	`ail ∨

Data: The BSD data.

Bit rate: The bit rate of the BSD data

Result

Click OK to run the BSD Decode and see result on the Waveform Windows below.



1me Div = 2 ms		287.96 m	s 289.96 ms	291.96	ms	293.96 ms	205.96 ms	297.96 ms	200.06 ms	301.96 ms	303.96 ms 305.96 r	ns 307.96 m:
		UNKNOWN	Sync	Master	Salve Add	ir: 6	Register Addr. 9	P1 OK		Data: 1	P2 OK	UNKNOWN
BSS	BSD - AO		749 u 749 us								665 u	
Л, Л, р	Channel	1										Q Q
Label										Q Search.	All Field	Q 2
Label	Channel		Register Addr	P1	Data	P2	Ack			C Search	All Field	
Label	llu E	<u></u>	Register Addr 2	P1 Ok	Data	P2	Ack			Q Search.	All Field	Q 2
Label	DIR			Ok		P2 Ok	Ack			C Search	All Field	Q
Label CH-00 CH-00 Timestamp 190.8714000 290.8838000	DIR Master	Salve Addr 6	2	Ok			Ack			C Search.	All Field	Q
Label CH-00 Bus Timestamp 190.8714000 290.8838000 390.8650000	DIR Master Master	Salve Addr 6 6	2	Ok Ok Ok	01		Ack			C Search	All Field	Q
Label CH-00 Bus Timestamp 190.8714000 290.8838000 390.8650000	DIR Master Master Master	Salve Addr 6 6 6	2 9 2	Ok Ok Ok	01	Ok	Ack			Search	All Field	Q 2
CH-00 CH-00 CH-01 Bus	DIR Master Master Master Master Master	Salve Addr 6 6 6 6 6 6	2 9 2 8	Ok Ok Ok Ok Ok	01 6a	Ok	Ack			C Search		



CAN 2.0B/ CAN FD

The Controller Area Network (CAN) protocol has version 2.0A (Basic CAN, 11 bits) and version 2.0B (Extended CAN or Peli CAN, 29 bits); both versions have four message types: Data Frame, Remote Frame, Error Frame and Overload Frame as the diagrams below. The CAN Bus has two kinds of data output: CAN High (CAN_H) and CAN Low (CAN_L).

The data rate is flexible in CAN FD (CAN with Flexible Data-Rate). When CAN FD is transferring, it is 64 (bytes/per data) and including CRC17/CRC21.

CAN Settings	X
Setting Channel CAN_L(Rx) CAN_L CH 0	Auto detect Data Rate 0.00 Kbps (5 Kbps ~ 1 Mbps)
	Show scale in the waveform CAN FD ISO-CRC Non ISO-CRC Data phase 500 Kbps
Start of Frame Identifier Data length code CRC ACK Slot End of Frame Start of Frame Mathematical Start of Frame Mathematical	
Range Decode Range From To Buffer Head ▼ Buffer Tail ▼ Default	OK

Settings



Channel: The differential data from the DSO channel (CAN_H or CAN_L) is shown by default.

Auto detect Data Rate: Check this option for auto-detecting the CAN bit rate by the LA Viewer; this option will be disabled when enabling CAN FD decode, the maximum input range of the Data rate is from 5Kbps-1Mbps.

Show scale in the waveform: Display the scale in the Waveform Window, this option will be disabled when enabling CAN FD decode.

Result

Click **OK** to run the CAN decode and see the result on the Waveform Window below.

		F) 314.0	09 us 31	9.09 us	324.09 us	329.09 us	334.09 us	339.09 us	344.09 us	349.09 us	354.09 us	359.09 us	364.09 us
Ime Div= 5 us		SOF				BaselD:112			RTR:0 IDE:0	R0.0	DLC:8		DAT.CD
▲ CAN	CAN_H-A0		7.5 us	2.5	ius 7.5	us 2.49 us	5.01 us	s 2.49 us	10.01 us	2.49 us	7.51 us		4.99 us
TIL TIL N	Channel 💽												Q
Label							-				rch All Field 💌		Q Q
Label	Channel		D	DLC		Data	CRC(h)	ASCII(Data)				: Duration	
abel	Channel 🧾		D	- 1	CD F1 97 E1 (CRC(h) 38F5	ASCII(Data)	Data Rate: 4	Information			
Label CH-00 CH-01 Bus Bus Sample 311,9600000	Channel 💽	I		8		01 9C 07 7D	Concession of the second			Information	Frame	us	
Label CH-00 Bus Sample 311.9600000 521.9100000	Channel	112		8	CD F1 97 E1 0	01 9C 07 7D 01 9C 07 7D	38F5)		Information	Frame 282.46	us us	
Label CH-00 Sample 311.9600000 621.9100000 931.8700000	Channel I Frame Type Std Data Std Data	1 112 112		8 8 8	CD F1 97 E1 (CD F1 97 E1 (01 9C 07 7D 01 9C 07 7D 01 9C 07 7D	38F5 38F5)		Information	Frame 282.46 282.47	us us us	
Label CHLO1 XBus Sample Sample S21.9100000 931.8700000 1.241820000	Channel (Frame Type Std Data Std Data	1 112 112 112		8 8 8 8	CD F1 97 E1 0 CD F1 97 E1 0 CD F1 97 E1 0	01 9C 07 7D 01 9C 07 7D 01 9C 07 7D 01 9C 07 7D	38F5 38F5 38F5	·····›}		Information	Frame 282.46 282.47 282.46	us us us us	
CH-00 CH-00 CH-01	Channel Channel Channe Type Std Data Std Data Std Data Std Data	112 112 112 112 112		8 8 8 8 8	CD F1 97 E1 (CD F1 97 E1 (CD F1 97 E1 (CD F1 97 E1 (01 9C 07 7D 01 9C 07 7D	38F5 38F5 38F5 38F5	······}		Information	Frame 282.46 282.47 282.46 282.47 282.47	us us us us us	



Closed Caption

Closed captioning is the process of displaying text on a TV or video screen. The text is encoded in the video data stream.

Settings

Closed C	aption Settings	×
Channel	A Channcel A0	
Color —		
	Clock run-in	
	Start	~
	Data	~
	Parity	~
Range		
inn:	Decode Range	
	From	То
	Buffer Head 🛛 🗸	Buffer Tail 🛛 🗸
	Def	Fault Ok Cancel

LA Channel: Show the selected channel (CH0).

Result

Click OK to run the Closed Caption Decode and see result on the Waveform Window

below.



Time Div = 5 us		-1.84 s	-1.84 s	-1.84 s	-1.84 s	-1.84 s	-1.84 s	-1.84 s		1.84 s -1.84 s	-1.84 s	-1.84 =
			Clock run-in		Start		Data:14		Ρ	Data 25	Ρ	
Closed Caption	CC-A0	1.4 0 1.4	u 1.4 u 1.4 u 1.4		4 us 2 us	4 us 1.8 u	s 2.2 us 1.8 us	4.2 us	3.8 us	2.2 us 1.8 us 4.2 us	1.8 us	() () () () () () () () () () () () () (
CH-00 Bus	- Lan									Q Search All Field 🔻		
Sample	Data Byte 1	Data Byte 2	ASCII							· · · · ·		
-1.86854060	and a second	00										-
-1.83517380	14	25	. %									
	00	00	• •									
-1.80180700		00	2.2									
-1.80180700	00	00										
-1.76844020	1000	00										
-1.76844020	1000	- Second										



DALI

Digital Addressable Lighting Interface (DALI) is a technical standard for network-based systems that control lighting in buildings. The DALI standard, which is specified in the IEC 60929 standard for fluorescent lamp ballasts, encompasses the communications protocol and electrical interface for lighting control networks.

Settings

DALI Setti	ings		×
Channel			
	LA Channel A0	Polarity D-	~
Color —	Show scale		
	Start		- ~
	Address		_ ~
	Command		~
	Response		~
	Stop		
	Unknown		
Range —			
Inn	Decode Range		
in the second se	From	n Buffer Head	~
	Т	Buffer Tail	~
r 1		o Buffer Tail	ancel

LA Channel: Show the selected channel (CH0).

Polarity:

- **D-:** Access side of the signal polarity is D-.
- **D**+: Access side of the signal polarity is D+.



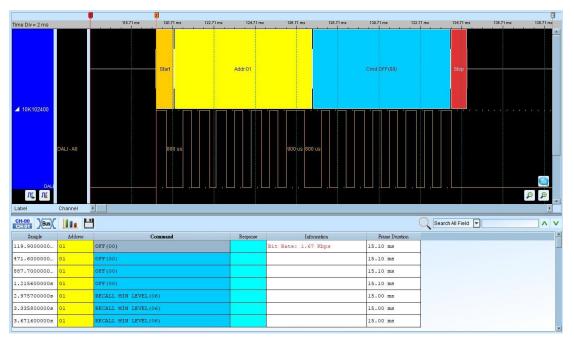
Auto: Automatically detect the polarity of the access end signal.

Show scale: Show Scale on the waveform.

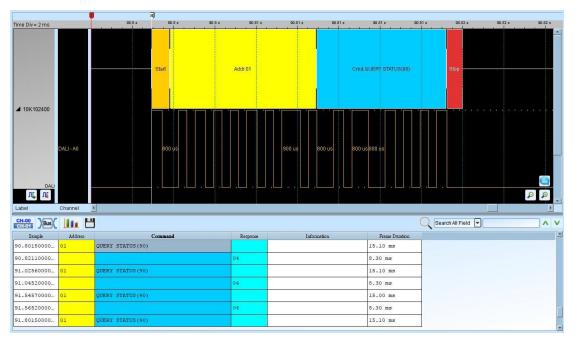
Result

Click OK to run DALI Decode and see result on the Waveform Window below.

Send data



Response data





DMX512

DMX512 is a standard for digital communication networks that are commonly used to control stage lighting and effects..

Settings

MX512 S		
Channel	Channel Data A0 ~	
	Auto Detect	
	Baud 250000	
Range		
22	Decode Range From	
	Buffer Head 🗸 🗸	
	+	
	То	

Data: Show the selected channel (CH0).

Auto Detect: Set the Baud Rate manually if not selected.

Result

Use grayscale to display the decode results.



Time Div = 50 us			3.1	81 ms		3.86 ms		3.91 ms	10.00	3.96 r	ms ,	4.0	1 ms		4.06 ms		4.11 ms	 4.16 ms	4.21 ms	4.26 ms	4.31 m
		Data	50	Data: 2	23	Data: 1	į	Data: 2	2		*	Data: 27		Data: BF		Data: 3	12	Data: 9F	Data: EA	Data: 28	Data: A0
DMX	Data - A0			12 u		12	U	12 u				2 U		24 us					20.2	5 u	23.75 u
DMX512																					Q
Л Ц ЛЦ Label	Channel	•																			
л ц лц Label	Channel																		th All Field 💌		
Label CH-00 Sample	State		D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	1	D13	D14	D15	Information	th All Field 💌		
ALABEI CH-00 CH-01 Sample 3.756850000	State	<u> </u>	D1	D2 15	22	77	27	BF	D7	92	9F	D10 EA	D11 28	D12 A0	9D	D14	D15		th All Field		
ALABEI CH-00 CH-01 Sample 3.756850000	State	<u> </u>	100		10000	D4 777 FE	27	10000	D7 32 27		1.4		D11 28	1		D14 23			th All Field 💌		
N. N. Label Bus (Sample 3.756850000 4.460850000 4.460850000	State	<u> </u>	100		22	77	27	BF	D7 32 27	92	9F	EA 89	D11 28 43 E6	A0 82	9D	D14 23 AB			th All Field		
M. M. Label Bus (Sample 3.756850000 4.460850000 5.164850000	State D[0:15] D[16:31]	D0 50 89	100	15 58	22 A9	77	27 2B	BF OF	D7 32 27 44	92	9F D8	EA 89	28 43	A0 82	9D C2	23 18	F9 82		th All Field		
M. M. Label Sample 3.756850000 4.460850000 5.164850000 5.868800000	State D[0:15] D[16:31] D[32:47]	D0 50 89	23 80 27	15 58 03	22 A9	77) FE 36	27 2D 9F	BF OF A6	D7 32 27 11 22 22 22 22	9E F1 #0	9F D8 OB	EA 89 70 30	28 43 26	A0 82 32	9D C2	23 79 AB	F9 82 DA		th All Field 🔽		
AL AL	State D[0:15] D[16:31] D[32:47] D[48:63]	D0 50 89	23 80 27	15 58 03	22 A9	77. FE 36 88	27 2D 9F 8A	BF OF A6	32 27 58 22	9E F1 40 13	9F D8 OB ED	EA 89 70 30	20 43 26 9D	A0 82 32 90	9D C2	23 AB AE	F9 82 DA DA		th All Field T		



Display Port Auxiliary Channel (DP Aux Ch)

The DP Aux Ch is to detect the link, configuration and status of the Display Port source. The Display Port is the digital display interface that is specified in the VESA standard.

Settings

DP AUX	CH Settings >	<
Channel	Channel Data A0 💽 🗋 Show DPCD	
Color		
	RequestImage: CMDAddressReplyImage: CMDImage: CMDCMDImage: CMDImage: CMD	
Range	Decode Range From To Buffer Head V Buffer Tail V	
-	Default OK Cancel]

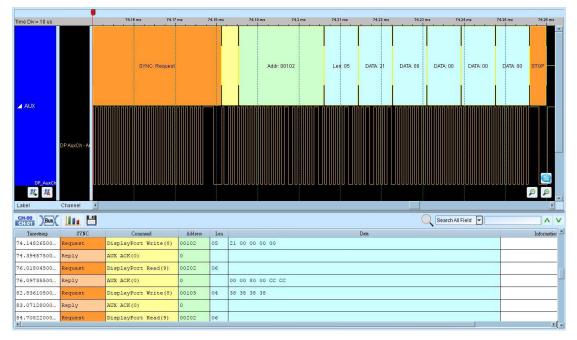
Data: Show the selected channel (CH0).

Show DPCD: Show the Display Port Configuration data.

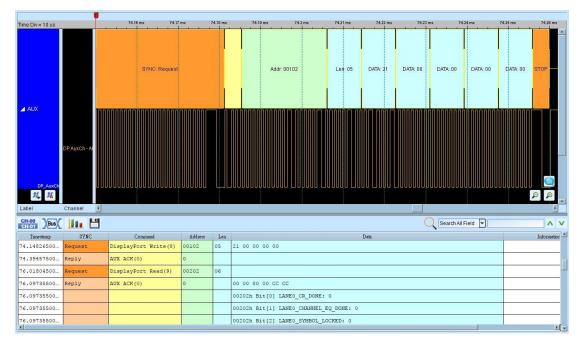


Result

Without the DPCD information



Show the DPCD information





Enhanced Serial Peripheral Interface (eSPI)

eSPI is the transmission protocol used in new generation baseboard of Intel, and its specification is to integrate SMBus / LPC / SPI Flash interface to simplify bus and increase transmission efficiency. Source of specification is based on Enhanced Serial Peripheral Interface (eSPI) Interface Base Specification (for Client and Server Platforms) June 2013, Revision 0.75.

Settings

Enhanced SPI (eSPI) Parameter Settings	×
Channel Settings CS# A0 SCK A1 Advanced Decode Setting I/O A2 I/O A3 Show RAW Byte Only I/O A2 I/O A3 Show Configuration Detail I/O A4 I/O A5 Show Status Bit Def. Alert A6 Reset # A7 Show VWire Detail Enable Glitch Filter Show Configuration Detail Show VWire Detail CS Work Mode Active Low Show OOB Detail Response latched on Clock Falling Reduced Report Startup Settings Vio Mede Settings Default Display	
I/O Mode Setting Single Mode PUT_PC Default Alert Mode From I/O[1] PUT_PC Auto-select protocol timing by clock speed PUT_PC Command deselect time 50ns Clock LOW to output valid 15ns	
Color OpCode Address Data Cycle Type Data Tag Response Status	$ \rangle \rangle \rangle \rangle \rangle$
Range Decode Range From To Buffer Head \checkmark Buffer Tail \checkmark Default OK Cancel	



Channel:

CS#:	Chip Select (Active Low)
SCK:	Clock
I/O0 – I/O3:	Data input / output
Alert:	Alert signal (Optional)
Reset:	Reset signal (Optional)

Startup Settings:

I/O Mode Setting: Set the initial I / O state to be Single / Dual / Quad, and I / O

state would be switched automatically by the content of the waveform.

Default Alert Mode: Set the channel of Alert signal.

Command deselect time: Set tSHSL, Chip Select# Deassertion Time.

Clock LOW to output valid: Set tCLQV, Output Data Valid Time.

Advanced Decode Setting:

Show Configuration Detail: Show details of SET_CONFIG / GET_CONFIG.

Show Status Bit Def.: Show details of Status.

Reduced Report: Reducing the report is easy to check the Command Flow.

Filter Setting: To show or hide the specific OP Code / Cycle Type or Address range in the report.

Note: The setting of Address Filter would be saved as LA\eSPI\eSPIFilterX.bin in the work directory.

Result

Click **OK** to run the eSPI decode and see the result on the Waveform Window below.



	P	0 ps	6 u		10 us		15 us		20 us		28	ius		30 us		36 us	40 us		46 us	50 us
me Div = 5 us		t t	(00) ADDF		i in i	SP (08)		DF) Data (0	+	. , ta (00)	1	1	, STS (0		. , ; (03)	CRC (B0)		ADDR	(00) ADDR (20) C	
	CS#-A2																			
	sck-аз															2	.69 us			
l eSPI1	SI/SO0 - A6	4.	78 us	2.38 us 2	2.39 us													3.9	7 us 1.99 u	1.99 u
	S0/801 - A5				1.6	u 2.7	79 us			11.15	us			2.39	us	1.6 u		16	.01 us	
	WP/802 - A1																			
espi	Hold#/SO3 - #																			۵
bel	Channel (_	_		_					
	Channel 💽															Q	Search All Fi	eld 🔻)	^
		onse		СусТуре		Tag	LEN	Address	DO	D1	D2	D3	D4 I	5 D6	D7	ASCII	Search All Fi	CRC]	Memo
Timestamp	III 💾			СусТуре		Tag		Address 0008				D3	D4 I	5 D6	D7	ASCII	•			
1.00 Bus Timestamp .80000000	OpCode/Resp	ION (21)				Tag			D0 OF			D3	D4 I	5 D6	D7	ASCII	Status 030F	CRC		Memo
H-00 Bus Bus Timestamp .80000000		ION (21)		Capabil:									D4 I	5 D6	D7		Status	CRC 10	FLASH_NP_FRE	Memo
H.00 Bus		ION (21)	CRC Che	Capabili cking Ena	able = 0								D4 I	5 D6	D7		Status 030F	CRC 10		Memo E
H.00 Bus Timestamp 0.54000000 0.54000000		ION (21)	CRC Che	Capabil:	able = 0								D4 I	5 D6	D7		Status 030F (Bit 9)	CRC 10	FLASH_NP_FRE	Memo E
Timestamp 2 . 80000000		ION (21)	CRC Che	Capabili cking Ena se Modifie	able = 0								D4 I	5 D6	D7		Status 030F (Bit 9) (Bit 8)	CRC 10	FLASH_NP_FRE	E



FlexRay

The FlexRay protocol has 2 bits with timing at 10Mbps.

FlexRay signal

Communication Data Layer: The FlexRay communication data is either at transmitter (Txd) or receiver (Rxd) of the FlexRay transceiver. You may set the threshold according to the FlexRay transceiver voltage.

Settings

FlexRay Settings X
Setting Channel Communication Data (TxD) V TxD CH 0 V Auto detect Data Rate 0.00 V Mbps (1 Mbps ~ 20 Mbps)
TxD FlexRay Channel TxEN Channel A RxD Show scale in the waveform
Color
Indicator Bits Frame ID Payload Length Header CRC Cycle count Data CRC CRC Indicator Bits Frame ID FSS FSS FSS FSS FSS FSS FSS FS
Range
Decode Range From To Buffer Head V Buffer Tail V
Default OK Cancel



Channel: Display the channel, Physical Layer is the default.

Communication Data (TxD): The TxD data is from the TxD and TxEN of the

FlexRay transceiver.

Communication Data (RxD): The RxD data is from the RxD and RxEN of the

FlexRay transceiver.

Auto detect Data Rate: Default is Auto Bit Rate. If disabled, you may use built-in

Bit Rate 10/5/2.5 Mbps or input manually, ranges from 1Mbps-20Mbps.

FlexRay Channel: Channel A or B, for Frame CRC checking.

Errors are:

Error	Description
TSS Error	Unable to detect TSS
FSS Error	Unable to detect FSS
BSS Error	Unable to detect BSS
FES Error	Unable to detect FES
Header CRC Error	The header CRC value is incorrect
Frame CRC Error	The frame CRC value is incorrect

Abbreviations are:

Abbreviation	Description
TSS	Transmission start sequence
FSS	Frame start sequence
BSS	Byte start sequence
FES	Frame end sequence
DTS	Dynamic trailing sequence
CAS	Collision Avoidance Symbol
MTS	Media Access Test Symbol



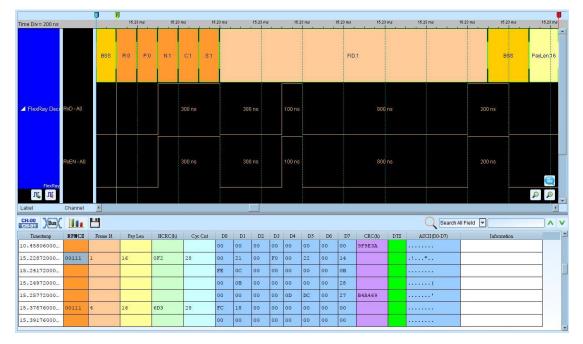
WUP	Wakeup Pattern
CID	Channel Idle Delimiter

Result

Click **OK** to run the FlexRay decode and see the result on the Waveform Window

below.

10Mbps FlexRay Communication Data(RxD)





HD Audio

High Definition Audio, also known as HD Audio or by its codename, Azalia, is an audio standard created by Intel to be used on their chipsets, i.e., it is a standard for high-quality on-board audio. In this tutorial we will explain more about this feature.

Settings

Chann	el 🚽			
1	SYNC A0 BCLK A1 V	I/O 0 A2	Direction SDI	
Color	Stream Data			
	Preamble Length		Stream ID Sample	~
	Response (SDI) Valid		UnSol	
	Reserved	~	Response	~
	Command (SDO) Reserved	-	CAd	
	NID		Verb ID	~
	Payload			
Range	Decode Range From	То		
	Buffer Head 🛛 🗸 🗸	Buffer T	ail 🗸	

Channel: Show the selected channel (CH 0-CH3).

Direction: Show the data with SDI or SDO decoding.



Result

Click **OK** to run the HD Audio decode and see the result on the Waveform Window

below.

ime Div = 200 ns		166.7	1 us	166.91 us	167.11 us	167.31 us	167.61	lus 1	67.71 us	167.91 us	168.11 us	168.31 us	168.51 u	168.71
		Frame Sync:FF					Respons	e:00000000				StreamTag:0	Length 00	Sample 0
	SYNC - A1	165 ns		67	Ons	6	i0 n 85 ns							
SDI_Bus	BCLK-A0								ΠΠΓ					
HD Audio	SDI - A2													
TID Addio		Frame Sync:FF	Reserved:00	CAB:0 N	ID:00	VID:0		Sample:FC	Samp	ile:4D Sample:4A	Sample:FF	Sample:49	Sample:AD	Sample:00
10000-000	SYNC - A1	165 ns		67	Ons	6	i0 n 85 ns		1					
SDO_Bus	BCLK-A0	חחחח		1000					ΠΠΓ		ΠΠΠ			
HD Audio	SDO-A3							125 ns 65	ns		165 ns			
ΛĻ Λ														Q Q
bel	Channel										0.5		_	
H-00 Bus	. 🌆 💾										Q	Search All Field	-	^
		Reserved	CAd	NID	5	/ID	Payloa	d Stre	am Tag)	Sam	plé		
Sample	Frame Sync													
7	Prame Sync									00 00 00 00 00	00 00			_
5.3700000		00	0	00	0			1		00 00 00 00 00 00 FC 4D 4A FF 49 3		0 00 00 00 0	00 00 00 00	
5.3700000 6.5350000		00	0	00	0			1			AD 00 00 0			_
55.3700000 56.5350000 70.2000000		.00	0	00	0			1		FC 4D 4A FF 49 2	AD 00 00 0	0 00 00 00 0	00 00 00 00	
55.3700000 56.5350000 70.2000000 72.8700000		00	0	00	0			1		FC 4D 4A FF 49 3	AD 00 00 0 00 00 00 0 00 00 00 0	0 00 00 00 00	00 00 00 00 00 00 00 00	
Sample 65.3700000 66.5350000 70.2000000 72.8700000 75.5350000 78.2000000		00	0	00	0			1		FC 4D 4A FF 49 3	AD 00 00 0 00 00 00 0 00 00 00 0 00 00 00	00 00 00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00 00 00 00 00	



HDMI-CEC

The HDMI-CEC bus is a one-wire, "party line" that connects up to ten (10) AV devices through standard HDMI cabling. The CEC protocol includes automatic mechanisms for physical address (topology) discovery, (product type based) logical addressing, arbitration, retransmission, broadcasting, and routing control. Message opcodes support both device specific (e.g. set-top-box, DTV, and player) and general features (e.g. for power, signal routing, remote control pass-through, and on-screen display).

Settings

	EC Settings	×
Channel	Report Format	O Advanced
Color	Setting the channel	of LA of CEC A0
	Start Bit Header Block	×
	Data Block EOM Bit	
	ACK Bit OPCode Block	· · ·
Range	Decoded Range From	To
	Buffer Head	∨ Buffer Tail ∨

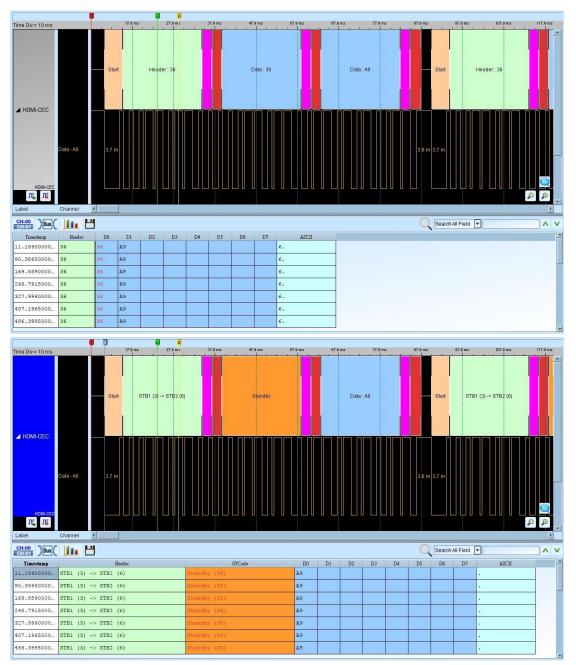
Latch data: Nominal (1.05 micro seconds) or User Define.



Result

Click \mathbf{OK} to run the HDMI-CEC decode and see the result on the Waveform Window

below.





HDMI-DDC (EDID)

EDID (Extended Display Identification Data) is I2C protocol base on DDC wire and transmitted monitor information. Now, HDMI, DVI and VGA are support this protocol.

Settings

DDC(ED	ID) Setting				×
Paramet	er Setting				
30	Channel Setti	ng			
:7	SCL AC		SDA	A1	•
	Address Mode	2			
	• 7-Bit Ac	Idressing			
	○ 7-Bit Ac	dressing(Incl	ude R/W in addre	ess)	
	Ignore glitch		Statistics Mo	de	
Color -					
	Start	~	Read/Write		
-	Stop		ACK		
	Address		NACK		
	Data	19		-	
Range					
	Decode Range				
H +I	From		to		
	Buffer Head	~	Buffer Head	~	
	Ĩ	Default	ОК		Cancel
	1			hund	

Channel: Display the channels (CH0 and CH1).

7-bit addressing: Show 7-bit addressing

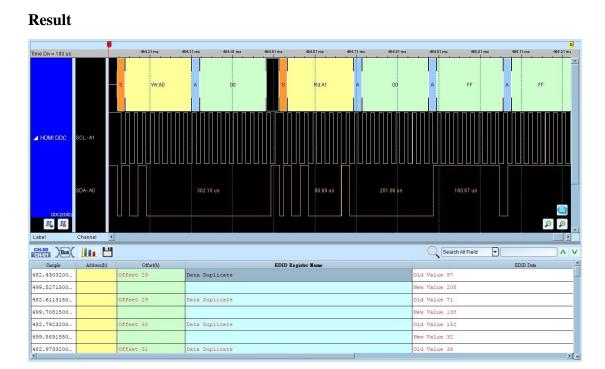
7-bit addressing(Include R/W in Address): Show 8-bit addressing(include 7-bit

addressing and 1-bit Rd/Wr).

Ignore glitch: Ignore the glitches occurred due to the slow transitions.

Statistic Mode: Collect all the data frames into one report by register address order.





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HDLC

HDLC (High-level Data Link Control) is the default synchronous data link layer protocol used in the equipment of Cisco.

Settings

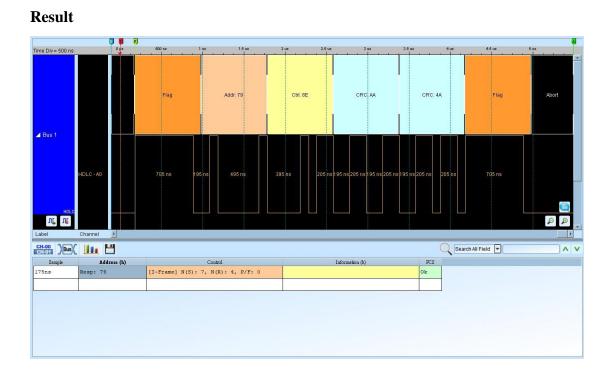
HDLC Settings	×
Channel HDLC A0 Mode Synchronous Bit rate Auto	Color Flag Addr Control Information FCS
Range Decode Range	To Buffer Tail
From Buffer Head	Buffer Tail

HDLC: Set the channel of the signal.

Mode: Synchronous or Asynchronous mode.

Bit rate: Set the specific data rate or auto detection.



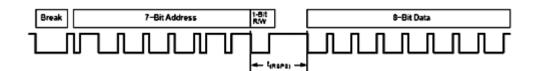


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HDQ

The HDQ bus has two kinds of formats: 8 bits or 16 bits signals as the diagram below.



Settings

HDQ Sett	ings			>
Channel		Color		
	Set the HDQ channel	i 🕕	Break	~
	Show Battery Information		Break Recovery	~
	bg27000		Address	~
	bq27010 bg27541		Read	~
	bg27541-V200		Write	
	bg27546-G1		Data	~
		Range		
	Enable glitch filter		Decode Range	
		HH	From Buffer Head	~
	Filter signal width <= 5.0 ns		To Buffer Tail	~
	-		Default OK	Cancel

Channel: Set the HDQ channel: Show the selected channel (CH 0).

Show Battery Information: monitor the command between battery and IC.

Result

Click **OK** to run the HDQ decode and see the result on the Waveform Window below.



Lee Channel Channel	me Div = 500 us	33.66 ms	B F 34.06 ms	34.56 ms	35.06 ms					The second se		
			Break	Addre	ss:34	w		15				
No. Image Addition Read/Within Data AddIt 1.0072000000 34 Vertice 15	HDQ-A0 HDQ JUL JUL		212 us	169 u	169 u 170 u	170 u 160	iu 169.u	169 u				() - Q -
Sanghal Address Dens ASCII 1: 00700000 34 Maine 15 1: 00700000 34 Maine 32 1: 00700000 34 Maine 32 1: 00700000 34 10 10 1: 00700000 34 10 10 1: 00700000 1: 00700000 34 10070000000 345 1: 0070000000 1: 0070000000 1: 0070000000 345 345 345 1: 0070000000 1: 0070000000 1: 00700000000 345 </td <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>arch All Field</td> <td></td> <td></td>										arch All Field		
10 DV = 500 US 32.50 ms 34.00 ms 34.50 ms 35.50 ms 35.50 ms 35.50 ms 35.50 ms 37.20 ms	.07700000 34	Write	15									
HDQ HDQ-A0 HDQ-A0 LC-Annel HC HC HC HC HC HC HC HC HC HC HC HC HC												
ноо - до 212 us 169 u 169 u 170 u 170 u 199 u 159 u 159 u 159 u 159 u 169 u 1	2 Div = 600 us	33.58 ms	B 8 34.06 ms	34.58 ms	25.08 ms	35.56 ms	38.08 ms	36.66 ms	37.08 ms	37.68 ms	38.06 ms	38.58 mi
bel Channel		33.38 ms	34.06 ms					<u> </u>	97.09 ms	37.58 ms	38,09 ms	38.66 m ; , , ,
	HDQ HDQ-A0	23 29 mm	Break	Addre	55:34			15	37.00 ms	97.66 ms	39.05 md	38.58 m
H00)Ba () Search All Field Sample Address/Command Code Write/Read Content Units	HDQ HDQ-A0 روم مراجع الله الله الله الله الله الله الله الله	33.58 ms	Break	Addre	55:34			15			39.05 me -]
setupe Address/common Code witheres Contrait othere .07700000 PassedCharge (34) Wite Image: Contrait Othere	HDQ HDQ-A0 HDQ A0 LDQ A	23.58 ms	212 US	Addre	55:34		10	15			38.05 ms	93.66 m



HID Over I²C

HID Over I2C (Human Interface Device Over I2C) protocol is established by

Microsoft. It's applied for Windows 8 ARM platform.

Settings

HIDove	rl2C Settings					×
Setting	Channel SCL SDA ATTN/Interrupt	A0 • A1 • A2 •	Color	Start / Restart Address Write / Read Data		
	O 10-bit addressing	ndude R/W in Address)		ACK NACK STOP		
Range	☑ Ignore glitch Decode Range From Buffer Head ✓	To Buffer Tail V				
				Default	ОК	Cancel

Channel: Show the selected channels (SCL:CH0, SDA:CH1, ATTN:CH2).

7-bit addressing: Show 7-bit addressing.

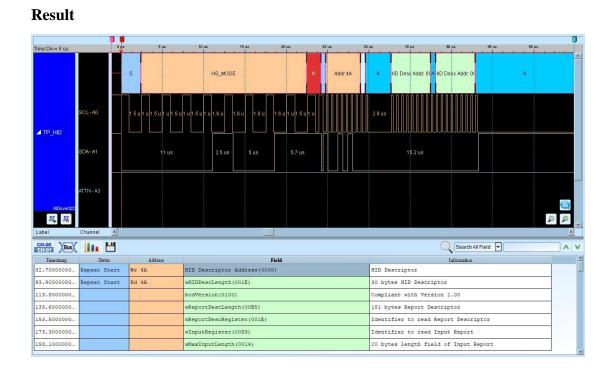
7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit

addressing and 1-bit Rd/Wr).

10-bit addressing: show 10-bit addressing.

Ignore glitch: Ignore the glitches occurred due to the slow transitions.





54



I^2C

The Inter-Integrated Circuit (I²C) bus has two data bits: Serial Data (SDA) and Serial Clock (SCL).

Settings

I2C Settir	ngs					?	×
Parameter	The second s			Color			
1	Channel Clock Channel (SCL) Data Channel (SDA)	A0	•		Address Data Write		·
	Address mode 7-bit addressing				Data Read Unknown		- ~
	 7-bit addressing (Ind 10-bit addressing 	lude R/W in Ac	ldress)		Start Re-Start		- ~ - ~
	Report Show data in report	8 Column	~		Stop ACK		
Range	Ignore glitch			Reser	ved Address		- ~
inn;	ecode Range From	То					
ł	Buffer Head 🛛 🗸 🗸	Buffer Tail	~				
					Default	ОК С	ancel

Channel: Display the channels (CH0 and CH1).

Address Mode: Select the 7-bit or 10-bit address.

7-bit addressing: Show 7-bit addressing.

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit

addressing and 1-bit Rd/Wr).

10-bit addressing: show 10-bit addressing.

Report: Show either 8 or 16-columns data in the report window.



Ignore glitch: Ignore the glitches occurred due to the slow transitions.

Result

Click **OK** to run the I^2C decode and see the result on the Waveform Window below.

It shows frequency in the Information field.





I3C

I³C is a bus interface for connecting sensors to an application processor. It is a core sensor integration technology that can combine multiple sensors from different vendors in a device to streamline integration and improve cost efficiencies. It gives developers unprecedented opportunity to craft innovative designs for any mobile product, from smartphones, to wearables, to safety systems in automobiles.

Settings

I3C Settings		×
Channel SDA A1	Color S / Sr / P ACK / NACK Address	
Range Decode Range From To	Command Data RnW T / PAR HDR RESTART	
Buffer Head V Buffer Tail V	HDR Exit	
	Default	OK Cancel

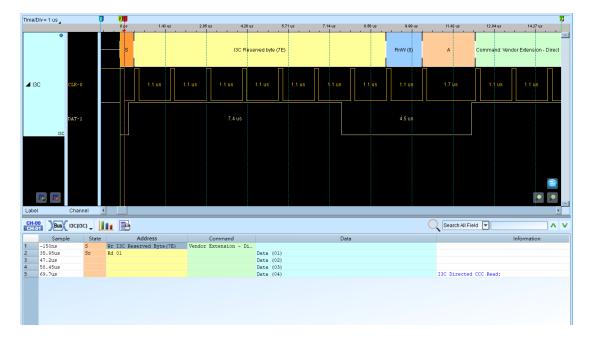
Channel: Display the channels (CH0 and CH1).



Result

Click **OK** to run the $I^{3}C$ decode and see the result on the Waveform Window below.

It shows frequency in the Information field.





I²C EEPROM

EEPROM can be erased and reprogrammed (written to) repeatedly through the application of higher than normal electrical voltage generated externally or internally in the case of modern EEPROMs.

Settings

I2C(EEPROM 24 Series) Settings		×
Parameters Channel	Color	
Clock Channel (SCL) A0 Data Channel (SDA) A1	Start Output Enable Control Control Device ID	~ ~
Address Address Width 7	Address Command Select Read Data Write Stop	
☐ 7-bit addressing (Include R/W in Ad ☐ 24LCS61 / 24LCS62 ☑ Ignore glitch Range	dress) ACK NACK Chip Chip	
Decode Range From To Buffer Head V Buffer Ta		
	Default OK	Cancel

Channel: Display the channels (CH0 and CH1)

Address: The default address width is 7.

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit

addressing and 1-bit Rd/Wr).

24LCS61/24LCS62: 24LCS61/24LCS62 EEPROM protocol.

Ignore glitch: Ignore the glitch when the slow transitions.



Result

Click OK to run the I^2C EEPROM decode and see the result on the Waveform

1 Time Div = 20 us 7.61 ms 7.63 ms 7.66 ms A Address(Lo): 40 A Address(Hil): 00 A A Data: 10 Data: 73 A Data ▲ I2C_eeProm 13.4 m 10 us ντ γι Q 0 anne Q Search All Field 🔽 CH-00 Bus III N V Read/Write Write Sample 7.439800000... D0 D1 D2 D3 D4 D5 D6 D7 Control Code Chip Select High Address Low Address ASCII 0A 40 !.s....Z 7.526500000... Read OA 7.776000000. Pc.2.... 7.991300000. .r@.ny. 8.206700000.... .+r6.g.v **B6** 8.422000000... 5*....lN 8.637400000...5...

Window below.



I^2S

The Inter-Integrated Circuit Sound (I2S) bus has three data bits: Serial Clock (SCK), Word Select Line (WS) and Multiplex Data Line (SD).

Settings

I2S Settings			×
Channel Clock Channel (SCK) Word Select Channel (WS) Data Channel (SD) Data bits	A0 A1 A2 16 Bits A0 A0 A1 A2 A2 A A A A A A A A A A		User can assign color for specific pattern. First Pattern & Color 0 Second Pattern & Color 0 Second Pattern & Color
Display the audio waveform Save as WAV file Mode I2S Justified Mode	□ Playback Report 8 Column ~	Range	Decode Range From Buffer Head To Buffer Tail
			Default OK Cancel

Channel: Show the selected channels (CH0, CH1 and CH2) and set Data bits (16

bits).

Display the audio waveform: Click to display the audio waveform in the Waveform

Window.

Playback: Click to display the audio from the speaker..

Save as WAV file: Click to save the data to a audio file(.wav) in the work directory.

Mode: I²S Justified/MSB Justified/LSB Justified/PCM/TDM.

Report: Select the column number.

Result

Click OK to run I²S decode and see the result on the Waveform Window below.



īme Div= 50 us		3.2 m	: 	3.25 ms	3.31		3.35 ms	3.41		3.46 ms 3.6	*	3.66 ms	3.6		3.66 ms	3.7	ms
▲ I2S_Decode	SCK-A0 WS-A1 SD-A2																
	Max: 32 Min: -31 Max: 32	2569														300 100 	00 line 10 line
- 125 114				nghaghad			yljuul uul ugly,	, jugjududu	lan landar	dugbydfygfundinidugbydfygf	nlındırglaşdış	Judadagija	Jug Jund und 1			100 -100 -300	
2S AL Label	Min:-3: Introduction			nglogloglond			ylandan lagla	n find an		dagboolyydainidagboolyyd	nlanlaghadag		luuluuluulu 0.60 Bearch All F			100 -100 -300 -300	
2S AL Label	Min:-3		ndandand 200 <i>5</i> 6	D2	D3	nd nul	15, 100, 100, 100, 100, 100, 100, 100, 1	ningimining 005	D7	ASCII(20-D7)	nladag <u>hada</u> g		ing mind mind of the second se	ield 💌	ninglagingin	100 -100 -300 -300	
Label CH-00 CH-01 CH-02	Channel •	dag mindaig	D1 L:2E73	D2 R:127D	D3 L:0E01	D4 R:FD46	D5	D6 R:DC40	D7 L:CC95	ASCII.00-D7)			Search All F	a luna uu luna u	ninghodaya	100 -100 -300 -300	
Label CH-00 CH-01 CH-02	Channel Channel Status(16Bits)	DOSC	Contractory and		A 200.027	COLUMN STOCK		1		the second second second		luuluuluyby Q	Lug Juni mi i 0.00	ield V		100 -100 -300 -300	
25 11. 12. akiel CH-001 (Bus) CH-011 (Bus) CH-010 (Bus) 10. 10. 10. 10. 10. 10. 10. 10.	Channel Status(IGBits) Data	D0 R:3D9F	L:2E73	R:1E7D	L:0E01	R:FD46	L:EC99	R:DC40	L:CC85	=s}F@			Luu Juni minin 000	ield 💌	mhughughu Baasaa	100 -100 -300 -300	
25 1. 1. 1. abel CH-00 CH-00 	Channel 4 Channel 4 Statu(IGBit) Data Data	DO R:3D9F R:BDA9	L:2E73 L:AFF2	R:1E7D R:A397	L:0E01 L:98D3	R:FD46 R:8FD3	L:EC99 L:88BF	R:DC40 R:83B2	L:CC85 L:80C8	=s)F			iearch All F	ield 💌	minghooga	100 -100 -300 -300	
Label Timetamp 3.091060000 3.257565000 3.340815000	Channel (Statuc)(16)th) Data Data Data	D0 R:3D9F R:BDA9 R:800C	L:2E73 L:AFF2 L:817E	R:1E7D R:A397 R:851C	L:0E01 L:98D3 L:8AD3	R:FD46 R:8FD3 R:928C	L:EC99 L:88BF L:9C24	R:DC40 R:83B2 R:A772	L:CC85 L:80C8 L:B443	=s}F@			Lund und mid n	e luningind Coccession		100 -100 -300 -300	
Label	Channel Channel Status(16bits) Data Data Data	D0 R:3D9F R:BDA9 R:C260	L:2E73 L:AFF2 L:817E L:D18B	R:1E7D R:A397 R:851C R:E183	L:0E01 L:98D3 L:8AD3 L:F1FF	R:FD46 R:8FD3 R:928C R:02B9	L:EC99 L:88BF L:9C24 L:1366	R:DC40 R:83B2 R:A772 R:23C0	L:CC85 L:80C8 L:B443 L:337C	=s}F@ 			Lund und mil nu l 0.80	ield V	ul nglog Jug lu	100 -100 -300 -300	



I80

The I80 controls 3 or 4-pins (WR, RD, CS, D/C) data.

Settings

180 Settings	×	(
Channel		_
	Select Channel	
1	D0 A3 🜩 D8 A11 🜩 D16 A19 🌩	
	WR A0 + D1 A4 + D9 A12 + D17 A20 +	
	RD A1 🗘 D2 A5 🔷 D10 A13 🗘 D18 A21 🗘	
	CS A2 C3 A6 C D11 A14 D19 A22	
	D4 A7 🗘 D12 A15 🗘 D20 A23 🗘	
	On D/C D5 A8 🗘 D13 A16 🗘 D21 A24 🖨	
	D/C A27 🗘 D6 A9 🗘 D14 A17 🗘 D22 A25 🗘	
	D7 A10 🜩 D15 A18 🜩 D23 A26 🜩	
	Data Bus Bit Order Report Data	
	8 Bit V LSB First V 8 Column V	
Color		-
	Setting Color	
	Command Read	
	Data Vite	
Range		_
-	Decode Range	
л.	-	
6 - 9	From To	
	Buffer Head V Buffer Tail V	
	Default OK Cancel	

Select Channel: Show the selected channels (WR, RD, CS, D0, D1, D2, D3, D4, D5,

D6,...).

On D/C: Use the D/C pin as Command (Low) or Data (High).

Data Bus: Select 4 Bit, 8 Bit, 12 Bit, 16 Bit, 20 Bit, or 24 Bit.

Bit Order: Select LSB First or MSB First.



Report Data: Select 8 columns or 16 columns.

Result

Click **OK** to run the I80 decode and see the result on the Waveform Window below.

fime Div = 1 us	-	2.05 m		s 2.05 ms	2.05 ms 2.06 ms	2.06 ms	2.06 ms 2	.06 ms 2.06 ms	2.06 ms	2.06 ms
			command Write DE					Data Write:01		
	WR - A2	360 n			6.96 us			360 n		
	RD - A3									
	CS-A0				3.66 us		3.66 us			
	D0-A4									
	D1 - A5				7.32 us					
4 180	D2 - A6				7.32 us					
	D3 - A7				7.32 us					
	D4 - A8				7.32 us					
	D5 - A9									
	D6-A10									
	D7 - A11									
	D/C - A1									
Λť Λί										0
abel.	Channel	•								1
H-00 Bu	X 🛄 💾	1						Q Search All Field 💌		^
Sample	Data/Comma	nd Write/Read	Data	ASCII				•		
.051180000	0 Command	Write	DE	Þ						
.058500000	D Data	Write	01							
.066200000	D Data	Write	00							
.075840000	0 Command	Write	BB	»						
.083160000	0 Data	Write	0A							
		- second sources	1963							
3.090860000	0 Data	Write	00	•						



IDE

IDE (Integrated Device Electronics) is a computer hardware bus and has the following data bits:

General Channel (11 pins): DASP-, DIOR-:HDMARDY-:HSTROBE, DIOW-:STOP, DMACK-, DMARQ, INTRQ, IORDY:DDMARDY-:DSTROBE, PDIAG-:CBLID-, RESET-, CSEL, IOCS16-. Register Channel (5 pins): CS(0:1)-, DA(2:0). Data Bus (16 pins): DD(15:0)

We recommend that IDE bus of the target system to be connected to the instrument as

IDE Pin No.	IDE Pin name	IDE Pin Description	LA default Channel No.
Pin1	Reset-	Hardware reset	Channel 0
Pin2	Ground		
Pin3	DD7	Device data	Channel 1
Pin4	DD8	Device data	Channel 2
Pin5	DD6	Device data	Channel 3
Pin6	DD9	Device data	Channel 4
Pin7	DD5	Device data	Channel 5
Pin8	DD10	Device data	Channel 6
Pin9	DD4	Device data	Channel 7
Pin10	DD11	Device data	Channel 8
Pin11	DD3	Device data	Channel 9
Pin12	DD12	Device data	Channel 10
Pin13	DD2	Device data	Channel 11
Pin14	DD13	Device data	Channel 12
Pin15	DD1	Device data	Channel 13
Pin16	DD14	Device data	Channel 14

the following table:



Pin17	DD0	Device data	Channel 15
Pin18	DD15	Device data	Channel 16
Pin19	Ground		
Pin20	Key pin		
Pin21	DMARQ	DMA request	Channel 17
Pin22	Ground		
Pin23	DIOW-:STOP	Device I/O write: Stop Ultra DMA burst	Channel 18
Pin24	Ground		
Pin25	DIOR-:HDMAR DY- :HSTROBE	Device I/O read: Ultra DMA ready: Ultra DMA data strobe	Channel 19
Pin26	Ground		
Pin27	IORDY:DDMAR DY- :DSTROBE	I/O channel ready: Ultra DMA ready: Ultra DMA data strobe	Channel 20
Pin28	CSEL	Cable select	Channel 21
Pin29	DMACK-	DMA acknowledge	Channel 22
Pin30	Ground		
Pin31	INTRQ	Device interrupt	Channel 23
Pin32	Obsolete (see note)	Device 16-bit I/O in ATA-2	Channel 24
Pin33	DA1	Device address	Channel 25
Pin34	PDIAG-:CBLID-	Passed diagnostics: Cable assembly type identifier	Channel 26
Pin35	DA0	Device address	Channel 27
Pin36	DA2	Device address	Channel 28
Pin37	CS0-	Chip select	Channel 29
Pin38	CS1-	Chip select	Channel 30
Pin39	DASP-	Device active, device 1 present	Channel 31
Pin40	Ground		



Settings

1.1	el							
	General Register Data Bus							
:7	DIOR-:HDMARDY-:HSTROBE	A20	DIAG-:CB	LID-	A24	1		
	DIOW-:STOP	A17	DAS	p.	A28			
	DMARO	A10	RESI	ET-	A19			
	IORDY:DDMARDY-:DSTROBE	A 77	CSE	L F	A23			
			 ■ IOC 	516	A0	-		
	DMACK-				AU			
	INTRQ	A31	•					
Color a	ind Setting							
	Transferring Mode Reg	ister Color	Analysis R	eport				
	2							
u	Transferring Mode	Max Tra	ansferring Rate	Star	ndard	~		
	PIO Mode 4		16.7MBvte/sec		ATA-3			
	DMA Single word, Mode		lyte/sec	ATA		-		
	DMA Single word, Mode		vte/sec	ATA	8	-		
	DMA Single word, Mode		vte/sec	ATA	4			
	DMA Multiple word, Mod	4.17MB	yte/sec	ATA	4			
	DMA Multiple word, Mod	13.3MB	yte/sec	ATA	4-2			
	DMA Multiple word, Mod	16.7MB	lyte/sec	ATA	4-3			
	ULTRA DMA Mode 0	16.6MB	lyte/sec	ATA	4-4			
	ULTRA DMA Mode 1	25MBy	te/sec	ATA	4-4			
	ULTRA DMA Mode 2		33MByte/sec		ATA-4			
	ULTRA DMA Mode 3		44MByte/sec		ATA-5			
	ULTRA DMA Mode 4	66MBy	Charles and a second second	ATA				
	ULTRA DMA Mode 5	100MB	Contract of the second s	ATA				
	ULTRA DMA Mode 6		vte/sec	ATA	1.7			

Channel: Set channel number for General, Register, and Data Bus.

Transferring Mode: Select the target system.

Analysis Report: Filter the data in the Report Window.



Result

	F	2.07 us	2.5	1.00	3.07 us	3.57 us	4.07 us	4.67 us	5.07 us 5.57 us	8.07 us	6.67 us	7.07 us
ime Div = 500 ns		· · · ·	' 1 <mark>' '</mark>									• • • <u>+</u>
IDE	A31,A30,A29,	Device: Dev0			<u>.</u>		Sector ent 01	LBA Low:01	LBA MId:00	LBA High:00		Device: Dev0
	A19	300	ns 1.7 us				00 ns 300 ns	500 ns 300		500 ns 3		
	A18		1.7 US			10 ns 4	00 ns 300 ns) ns 400 ns 300 ns	500 ns _ 3	00 ns	
Data(015)	A16:A16							0				
Register	A29:A29	0		1	Ĭ	0	1 0	1	0	1	0	[1](
MARQ	A17			л <u></u>								
DRDY:DDMARD	A20	1										
MACK-	A22											
	A23											
	A26											
William .	A31		_									
and the second	A0 A21						_				_	
	A24					-		i				_
	Channel !											<u> </u>
CH-00 Bus										arch All Field 🔻		^
Sample	Event	Register	Data Hi	Data Lo	Command	Drive	Description	Time interval				
. 600000000	Wr Device	1F6		A0		0	DEV0	0 ns				
. 300000000	Rd Status	1F7		50		0	DRDY	700 ns				
8.600000000	Wr Sector	182		61		0		1.300 us				
1.300000000	LBA Low	1F3		01		0		700 ns				
	LBA Mid	1F4		00		0		800 ns				
.100000000	LBA Mid	111										
5.100000000 5.800000000	LBA Mid	1F5		00		0		700 ns				

Click **OK** to run the IDE decode and see the result on the Waveform Window below.



IrDA

The Infrared Data Association (IrDA) was formed in 1993. The IrDA is point to point user model for a wide range of appliances and devices.

Settings

IrDA Settin	gs		\times
Channel	LA channel A0	~ prm	
Color			
	Start	~ ~	
	Data	<u> </u>	
	STOP	~ ~	
	Addr	~	
	CRC	~	
Range			
	Decode Range		
	From	To	
	Buffer Head	∨ Buffer Tail ∨	
	Default	OK Cancel	

Channel: Show the selected channel.



Time Div= 200 us 3.84 = 3.84 = 3.85 = 3.85 ± 3.85 = 3.85 \$ 3.85 = 3.85 \$ Data: 04 Stop Starf Data: 01 Stop Start Stop NL NL QQ Label CH-00 Bus Bus Search All Field ∧ v D3 OB FF D4 D5 8E C1 D10 D11 D12 D13 D14 D15 ASCII D0 D1 D2 D6 D7 D8 D9 Information Sample 3.844607350s 01 CO 2D C0 C0 C0 CO 3.940492195s FF FF 3F FF FF 05 3.957131650s CO D3 97 C1 CO CO CO CO CO 4.052912500s 3F 2D F9 11 FF FF FF FF FF FF 00 4A 73 45 C0 4.069551950s 41 43 55 54 48 41 4E 47 \$.ACUTE_HANG..J. C8 5.096934155s CO CO CO CO CO :0 C0 A8s-2D 5.113573605# F9 40 82 3F?

Result



ITU656 (CCIR656)

ITU656 describes a simple digital video protocol for streaming uncompressed PAL or NTSC Standard Definition TV (525 or 625 lines) signals. The protocol builds upon the 4:2:2 digital video encoding parameters defined in ITU-R Recommendation BT.601, which provides interlaced video data, streaming each field separately, and uses the YCbCr color space and a 13.5 MHz sampling frequency for pixels.

Settings

P	Channel						Data Bi	ts
1	Clk	A0	-	Data 5	A6	-	8	→ Bit
	Data 0	A1	-	Data 6	A7	-	80	
	Data 1	A2		Data 7	A8	-	Channe	l number
	Data 2	A3	-	Data 8	A9		1	~
	Data 3	A4	-	Data 9	A10	-	1	
	Data 4	A5	- Internet		·			
olor —	SAV		-] ~ (CR		
olor —						ж [в [~
olor —	SAV					38		
olor —	SAV] ~ (38		
ange -	SAV	9] ~ (38		
	SAV EAV Blanking	9		To] ~ (38		

Channel: Show the selected channel (Clk, Data 0 – Data 9).



Data Bits: Show the number of data bits.

Result

	Ę	-6.12 ms	F	12 ms	-5.12	D.S.	-6.12 ms		-5.12 ms		6.12 ms	-5.12 ms	-6.12	ms	-5.12 m	e .	-6.12 ms		-6.12 ms
fime Div= 20 ns		SAV(80)		1		1 '	1	ri i i		<u>''</u>	1 .	CR: 80 Y: 01	1 1	-'I-		1 1	r – I – I	CR: 80 Y	
	CIK-A8	5 ns5 ns 5 ns	5 ns5 ns	5 ns 5 n	s 5 nst	ins 5	ns5 ns5 n	s 5 ns	5 ns 5 n	is 5 ns	ins5 ns5 ns	5 ns5 ns5	ns 5 ns 5 r	ns 5 n	IS5 ns 5 I	ns5 ns	5 ns5 ns	5 ns 5 n	ns5ns
	Data0 - A0		60	ns.				37.5 ns			27.5 ns	8.75 ns	28.75 n		8.75 ns		5 ns		
	Data1 - A1	22.5 ns	18	3.75 ns	18.75	ns		37.5 ns		8.75 ns	3.75 ns	L 28.75 ns	8.75 ns	6	[27.5 ns	10	ns		
	Data2 - A2		61.25					37.5 ns						-			-		
ITU656	Data3 - A3		60	Inis			18.75 ns	ŝ	20 ns										
	Data4 - A4	41	.25 ns		18.75	ns		38.75 ns	3				98.75	ns				8.75 ns	
	Data5 - A5	41	.25 ns			37.5 r	IS		20 ns										
	Data6 - A6	41	.25 ns		18.75	ns	18.75 ns		18.75 ns										
ITU65	Data7 - A7	15 ns	26.25	ns	18.75	ns		46.2	5 ns		10 ns 8.7	5 ns 8.75 ns 1	0 ns 8.75 ns	s 8.75 ns	10 ns 8	75 ns 10	ns 8.75		
₩,																		Q	Q
.abel	Channel													~ ~					
CH-00 Bus	X 💵 💾												(2 Se	arch All Field	1			^
Sample		SAV	CB	Y	CR	у	CB	Y	CR	у		E≜V		Info	nnation	_			
5.11574500.		l, elsewhere.	82	82		70		AF		C7									
5.11567125.			80	02		01		02	80	01									
-5.11559750.			80	02		11	2000	CA	75	E8									
5.11552375.	-		80	E5		E8		E7	2252	E8									
-5.11545000.			80	E8	80	E8	80	E8	80	E8									
-5.11537500.	-		7F	E 7	80	E8	80	E8	80	E7									
			80	E8	80	E7	80	E8	80	E7									



JTAG

Joint Test Action Group (JTAG) is the common name used for the IEEE 1149.1 standard entitled Standard Test Access Port and Boundary-Scan Architecture for test access ports used for testing printed circuit boards using boundary scan.

A JTAG interface is a special four/five-pins interface added to a chip, designed so that multiple chips on a board can have their JTAG lines daisy-chained together if specific conditions are met, and a test probe need only connect to a single "JTAG port" to have access to all chips on a circuit board.

Settin	g			
	Channel Setting Repor	t		
	Test Clock (TCK)	A0	€	
	Test Mode Select (TMS)	A1	Test Reset (TREST) A4	
	Test Data Input (TDI)	A2	*	
	Test Data Output (TDO)	A3	*	
Color				
	1			
TEST		~	EXIT1-IR	~
RUN	_TEST_IDLE	~	EXIT1-DR	~
	CT-IR	~	PAUSE-IR	-
SELE		~	PAUSE-IR	
SELE SELE	CT-IR	~	PAUSE-IR	
SELE SELE CAPT	CT-IR CT-DR	~	PAUSE-IR PAUSE-DR EXIT2-IR	
SELE SELE CAPT CAPT	CT-IR CT-DR		PAUSE-IR PAUSE-DR EXIT2-IR	
SELE SELE CAPT CAPT SHIF	CT-IR CT-DR		PAUSE-IR PAUSE-DR EXIT2-IR EXIT2-DR	
SELE CAPT CAPT SHIF SHIF	CT-IR CT-DR		PAUSE-IR PAUSE-DR PAUSE-DR EXIT2-IR PAUSE-IR PAU	
SELE SELE CAPT CAPT SHIF	CT-IR		PAUSE-IR PAUSE-DR PAUSE-DR EXIT2-IR PAUSE-IR PAU	

Settings



Settings: Includes Channel, Setting, and Report.

Channel: Set the channel number.

Show the test data is: The data is TDI or TDO.

Test Data Bit Order: LSB First or MSB First.

Show the test data is	Interpreter instruction	
🔿 Test Data Input (TDI)	ID Name	Len
Test Data Output (TDO)	000 ARM7~ARM9	4
	001 ARM10	4
Test Data Bit Order	002 ARM11	5
LSB First 🗸 🗸	003 ARM Cortex M1	4
	Refra	esh Edit

Interpreter instruction: Check the Interpreter Instruction and you will see a list of commands. The JTAG decode will display its updated commands in the Instruction Register, which is the temporary memory buffer for the commands. Click Edit to edit the commands in the Interpreter Instructions; then click Refresh to update the commands in the Interpreter Instructions.

Acute JTAG Instruction table (JtagInst.txt): This file is supported by the JTAG DLL and can be modified if needed. The JTAG Decode also supports the BSDL format. You can load the BSDL file in order to save time on editing commands. If you are interested in more details, please refer to the Acute JTAG Instruction table Syntax Description in the end of the JTAG Decode chapter.

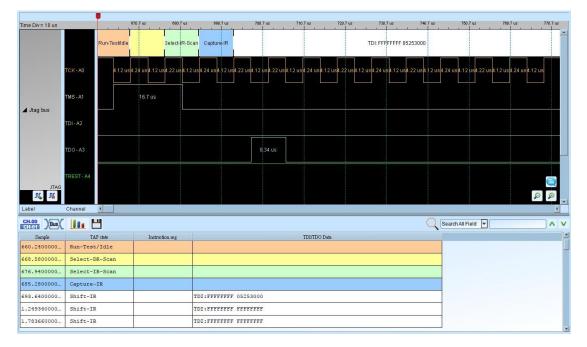
Report: You can filter the data you want to see on the Report Window.

Show the state in report		^
Test-Logic-Reset		
Run-Test/Idle		
Select-DR-Scan		
Select-IR-Scan		
Capture-DR		
Capture-IR		~
Show TDI or TDO	Show TDI and TDO	



Show TDI or/and TDO

Result



Acute JTAG Instruction table Syntax Description (JtagInst.txt):

The numbers used in this file are hexadecimal.

##: is comment.

#ID: Command list number; the range is 00 - FF and , MUST be entered in order or

will be seen as the end of commands.

#NAME: Command Name, 32 bytes most will be shown in the command list.

#LENGTH: Command length, unit in bits.

#CAPTURE: Command Capture Code, is stored in Instruction Register..

#INST: Command List, listed by Command Code and Command Name or will be

seen as the end of commands..

#TRST: Enter 1 if TREST is needed or enter 0 or nothing if TREST is not needed.

#BSDL: Load the BSDL file. Use the BSDL file as step 1-6.



Example:#ID:00

#NAME:ARM7-ARM9

#LENGTH:4

#CAPTURE:1

#INST:0, EXTEST

#INST:2, SCAN_N

#INST:3, SAMPLE/PRELOAD

#INST:4, RESTART

#INST:5, CLAMP

#INST:7, HIGHZ

#INST:9, CLAMPZ

#INST:C, INTEST

#INST:E, IDCODE

#INST:F, BYPASS

#INST:

#ID:01

#BSDL:C:\3256at144_1532.bsd



LCD1602

The Liquid Crystal Display 1602 (LCD1602) bus has 11 data bits: Instruction/Data Register Select (RS), Read/Write Select (RW), Enable Select (E) and 8 bits or 4 bits Data Input/Output lines (DB0~DB7/DB0~DB3).

Settings

LCD1602 9	Settings										×
Channel											
-8	Chan	nel									
:-/	RS	AO	+	DB7	A3		+	DB3	A7		-
	RW	A1	•	DB6	A4		*	DB2	A8		•
	E	A2	+	DB5	A5		+	DB1	A9		-
				DB4	A6		+	DB0	A10	6	÷
	Data	Mode						⊠ ⊺0	merce	a the i	eame
	(🖲 8 Lines		04	Lines				nmano		
Color –											
	Setting	Commands (Color								
	SCREE	N CLEAR				CGF	RAM	AD SE	г		
	CURSC	OR RETURN	[~	DDF	RAM	AD SE	т [
	INPUT	SET	E		- L	FUN	ICTI	ON SE	r [~
	DISPLA	AY SWITCH	[_ ~	DAT	ra n	RITE			~
	SHIFT					DAT	ra R	EAD			~
	BUSY/	AD READ CT			~						
Range -	Decode	Range									
森		om			1	То					
	В	uffer Head			~	Buffe	r Tai	l		~	
				Def	fault	I		ж	[Cano	el

Channel: Show the selected channels (RS: CH0, RW: CH1,..., DB0: CH10).

Data Mode: 8 lines or 4 lines.



To merge the same command: Merge data with its command.

Result

Click **OK** to run the LCD1602 decode and see the result on the Waveform Window

below.

ime Div= 50 us	12	8 ms 12.86 ms 12.7 ms	12.76 ms 12.8	ms 12.86 ms	12.0 ms 12.0	5 ms 13 m	s 13.06 ms 13.1 m:
	Cursor Retu	m:02 CGRAM/DDRAM Data V	wite:56 CGRAM/DE	RAM Data Write:69	CIGRAM/DDRAM Da	ta Write:6F	CGRAM/DDRAM Data Write:3A
	RS-A0						
	RW - A1						
	E - A2	61.5 us	32.4 us 61.4 us	62.4 us	61.41 us	62.4 us	61.51 us
	DB7 - A3						
LCD1602	DB6-A4		371.5 us				
	DB5 - A5	123.8 us					
	DB4 - A6	123.8 us		247.7 us			123.91 us
	DB3 - A7				371.6 us		
	DB2-A8	123.81 us	123.9 us		123.81 us		
	DB1 - A9	123.8 us	123.9 us			247.71 us	
LCD1602	DB0-A10			247.7 US			
Vî Vî							
abel	Channel •						
H-00 Bus	111 💾				(Search All Fie	Id 🔽 🔨 🔨
Sample	Command	Data		ASCII			
.638635000	Cursor Return	02		1			
2.62619500	CGRAM/DDRAM Data Writ	e 56 69 6F 3A 20 33 2E 33 38	20 56 20 20 20 20 20 V	io: 3.38 V			
3.02783000	Cursor Return	02		5			
.01539000		e 56 69 6F 3A 20 33 2E 33 38	20 56 20 20 20 20 20 V	io: 3.38 V			
L.41703000	Cursor Return	02					
9.40458500		e 56 69 6F 3A 20 33 2E 33 38	20 56 20 20 20 20 20 V	io: 3.38 V			
1.80622500	Cursor Return	02					



LED_Ctrl

LED Controls are made specifically for digital type LEDs. These LEDs contain a special IC chips that allow the user to control each LED or section of LEDs.

Settings

LED_CTR	L Settings	×
Channel		Color
	Channel	
• -3*	Data A0 \sim	
		C2
	Waveform display	Data 🗸
	Value O Color	Data2
	Chip setting	
	O Custom ○ TM1814 ○ WS281	1
	T0 min: 300 style="text-align: center;"> 10 min: 300 10 min: 300	T0 Max: 400 • ns
	T1 min: 600 ns	T1 Max: 1000 ns
	Reset: Auto \checkmark 20	0 • us
	Bit Size: 24-bit ~	
Range	Decode Range	
*	From To	
	游標A ~	~
		Default OK Cancel

Channel: Show the selected channels.

Waveform display: show value or RGB color in waveform area.



Chip setting: Custom, TM1814, WS2811

Condition: Idle high

If the time that waveform goes to low between T0 min and T0 max, the bit will

decode as zero. If it's between T1 min and T1 max, the bit will decode as one.

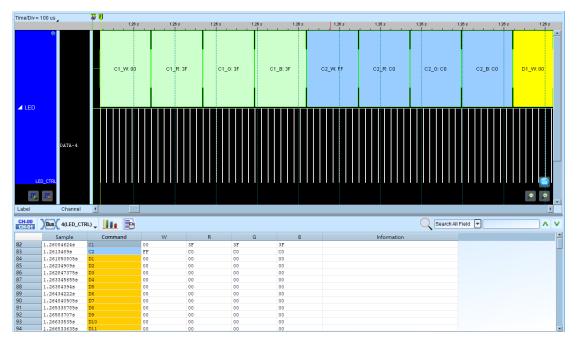
Reset: if the waveform keeps at high potential over the time, the decoder will reset the start bit.

Bit size: choose 32-bit (WRGB) or 24-bit (RGB).

Result

Click **OK** to run the LED_Ctrl decode and see the result on the Waveform Window

below.





LIN

The Local Interconnect Network (LIN) bus (version 2.1) has two message types: Header and Response.

- Header contains three data frames: Synchronization Break (Break),
 Synchronization Field (Sync) and Identifier Field (Identifier).
- (2) Response contains two data frames: Data Field (Data) and Checksum Field (Checksum). Checksum contains data and identifier (Enhanced mode), but version 1.3 or below (Classic mode) contains data only.

LIN bus has two states - Sleep mode and Active mode. While data is on the bus, all

LIN nodes are in active state; but after a specified timeout, the nodes enter Sleep

mode and will be released back to active state by a WAKEUP frame.

Settings

LIN Setting	S	\times
Channel -		
	Version	
	●LIN 2.2/2.1 ○LIN 2.0 ○LIN 1.2	
	Checksum mode	
	Classic Classic Chanced	
	LA Channel A0 Show scale	
	Baudinate AUTO V bps	
	Baud rate AUTO v bps	
Color —		
Color		
	Wake-up	_
	Wake-up	^
	Break	7
	Synch	4
	Synch	^
	Identifier	7
	Data	4
	Data	_
	Checksum	7
Range		
inn:	Decode Range	
	From To	
	Buffer Head V Buffer Tail V	
	burrer read	
	Default OK Cancel	



Version: Select LIN version.

Checksum Mode: Select Classic: data only or Enhanced: data and identifier.

LA Channel: Show the selected channel (CH0 for LIN).

Show Scale: Show scale on the waveform.

Baud rate: Show the selected baud rate.

Result

Click **OK** to run the Lin decode and see the result on the Waveform Window below.

		F								B
fime Div= 1 ms		2.11 ms	3.11 m	ns 4.11 ms	6.11 ms 6.11 ms	7.11 ms	8.11 ms	9.11 ms	10.11 ms 11.11 ms	12.11 ms
	Wa	keup	Break	Sync ID:31	EA 80 48	3F ED 90) B5 4	47 Br	eak Sync ID:25 -	- 31 B4
LN		1.04 ms	677 us	468.5	iu			72	9us	
л ц лц Label	Channel •									
CH-00 Bus	<u>III 💾</u>							📿 Sear	ch All Field 🚽	^
Timestamp	Event Type	PID(ID+P)	ID	Parity	Data	Checksum(h)	ASCII	Frame Duration		Informa
1.042500000	Wakeup							1.458 ms		
2.501000000	LIN Frame	B1	31	2	EA 8B 48 3F ED 9C B5 A7	1A	H?	6.822 ms		
9.376500000	LIN Frame	25	25	0	31 B4 2C 3F	AE	1.,?	4.791 ms		
14.16800000	Diagnostic Frame	3C	3C	0	00 FF FF FF FF FF FF FF	00		6.458 ms		
20.62650000	Wakeup							1.458 ms		
22.08500000	LIN Frame	B1	31	2	EA 8B 48 3F ED 9C B5 A7	la	H?	6.822 ms		
					31 B4 2C 3F					



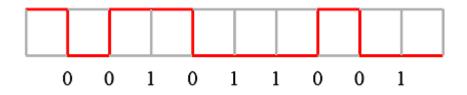
Line Decoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes:

NRZI (Transition occurs for a one): A 1 is represented by a transition of the physical level, a 0 has no transition.



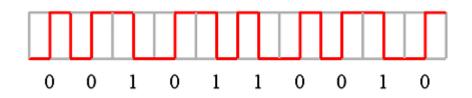
NRZI (Transition occurs for a zero): A 0 is represented by a transition of the physical level, a 1 has no transition.



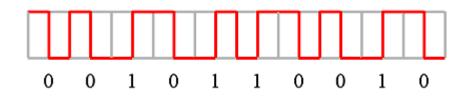
Manchester: In telecommunication, Manchester code is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. There are three modes:

Manchester (Thomas): A 0 is expressed by a low-to-high transition, a 1 by high-to-low transition.

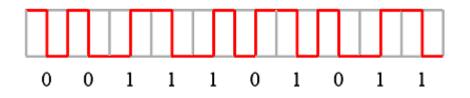




Manchester (IEEE802.3): A 1 is expressed by a low-to-high transition, a 0 by high-to-low transition.



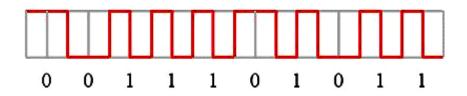
Differential Manchester: A 1 bit is indicated by making the first half of the signal equal to the last half of the previous bit's signal i.e. no transition at the start of the bit-time. A '0' bit is indicated by making the first half of the signal opposite to the last half of the previous bit's signal i.e. a zero bit is indicated by a transition at the beginning of the bit-time. In the middle of the bit-time there is always a transition, whether from high to low, or low to high. A reversed scheme is possible, and no advantage is given by using either scheme.



Bi-phase Mark: The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions which makes clock recovery and synchronization difficult. When



encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that together form a bit.



Miller: Delay encoding is also known as Miller encoding.

In telecommunications, delay encoding is the encoding of binary data to form a two-level signal such that (a) a "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period; and (b) a "1" causes a transition from one level to the other in the middle of the bit period.

Delay encoding is used primarily for encoding radio signals because

the frequency spectrum of the encoded signal contains less low-frequency energy than a conventional non-return-to-zero (NRZ) signal and less high-frequency energy than a bi-phase signal.

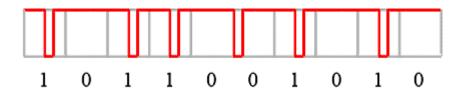


Modified Miller: The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation data demodulation circuit for producing NRZ - L data by utilizing the clock bits, data bits



and synchronizing clock pulses which are output from the data separation circuit.

This structure enables the M 2 modulation data which is input to the M 2 demodulation circuit to be easily demodulated to an NRZ - L type data signal by means of a very simple circuit structure. An example is as below:



Settings

Line Dec	oding Settings				×
Select Dec	Select wavefo And set the p	form format for decode, barameters, on occurs for a one) \checkmark	Channel	Data Channel A0 Decode Range	•
	Show Unkno Auto-Detec Data Rate			From Buffer Head To Buffer Tail	~
				ОК	Cancel

Select Decoding: Select the line code you want to decode.

Show Unknown: Display unknown data.

Show Bus: Display bus data.

Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Date Rate

is not selected.

Channel: Show the selected channel (CH 0).

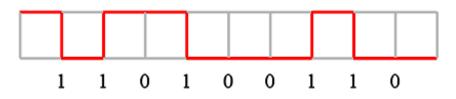
Range: Select the range within the waveform you want to decode.



Line Encoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes:

NRZI (Transition occurs for a one): A 1 is represented by a transition of the physical level, a 0 has no transition.

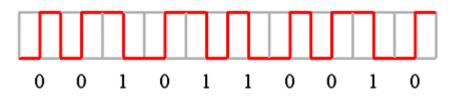


NRZI (Transition occurs for a zero): A 0 is represented by a transition of the physical level, a 1 has no transition.



Manchester: In telecommunication, Manchester code is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. There are three modes:

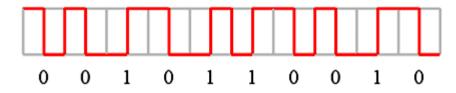
Manchester (Thomas): A 0 is expressed by a low-to-high transition, a 1 by high-to-low transition.





Manchester (IEEE802.3): A 1 is expressed by a low-to-high transition, a 0 by

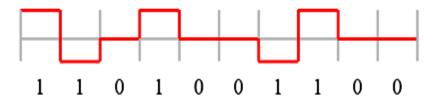
high-to-low transition.



Differential Manchester: A 1 bit is indicated by making the first half of the signal equal to the last half of the previous bit, i.e. no transition at the start of the bit-time. A '0' bit is indicated by making the first half of the signal opposite to the last half of the previous bit's signal i.e. a zero bit is indicated by a transition at the beginning of the bit-time. In the middle of the bit-time there is always a transition, whether from high to low, or low to high. A reversed scheme is possible, and no advantage is given by using either scheme.

AMI (Alternate Mark Inversion): There are four modes:

AMI (Standard): AMI (Alternate Mark Inversion) is a synchronous clock encoding technique that uses bipolar pulses to represent logical 1 value. It is therefore a three level system. A logical 0s is represented by no symbol, and a logical 1 is represented by alternating-polarity pulses.

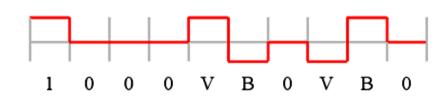


AMI (B8ZS): Bipolar-8-Zero Substitution

If 1 is +, 00000000 is represented to 000+-0-+

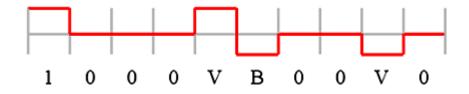
1 is -, 00000000 is represented to 000-+0+-

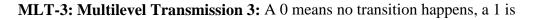




AMI (HDB3): High Density Bipolar 3

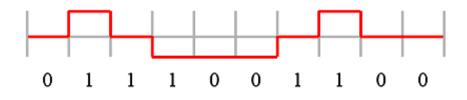
The HDB3 code is a bipolar signaling technique (i.e. relies on the transmission of both positive and negative pulses). It is based on Alternate Mark Inversion (AMI), but extends this by inserting violation codes whenever there is a run of 4 or more 0's. This and similar (more complex) codes have replaced AMI in modern distribution networks. The encoding rules follow those for AMI, except that sequences of four consecutive 0's are encoding using a special "violation" bit. This bit has the same polarity as the last 1-bit which was sent using the AMI encoding rule. The purpose of this is to prevent long runs of 0's in the data stream that may otherwise prevent a DPLL from tracking the center of each bit. Such a code is sometimes called a "run length limited" code, since it limits the runs of 0's that would otherwise be produced by AMI. One refinement is necessary, to prevent a dc voltage being introduced by excessive runs of zeros. This refinement is to encode any pattern of more than four bits as B00V, where B is a balancing pulse. The value of B is assigned as + or -, so as to make alternate "V"s of opposite polarity. The receiver removes all Violation pulses, but in addition a violation preceded by two zeros and a pulse is treated as the "B00V" pattern and both the violation and balancing pulse are removed from the received bit stream. This restores the original bit stream.







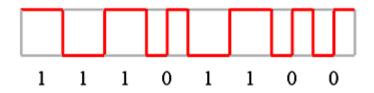
represented by a transition (0, +, 0, -).



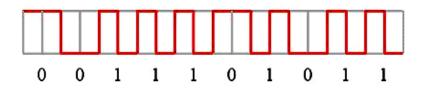
Pseudoternary: A 1 is always zero, a 0 is represented by a transition (+, -).



CMI (Coded Mark Inversion): A zero is sent a low to high [01] transition, while a one is sent as either a one [1] or zero [0] depending on the previous state. If the previous state was high the one is sent as a zero [0], if it was low the one is sent as a one [1].



Bi-phase Mark: The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions that make clock recovery and synchronization difficult. When encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that form a bit.



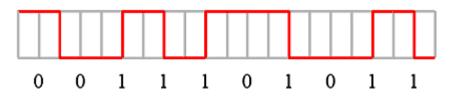


Miller: Delay encoding is also known as Miller encoding.

In telecommunications, delay encoding is the encoding of binary data to form a two-level signal such that (a) a "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period; and (b) a "1" causes a transition from one level to the other in the middle of the bit period.

Delay encoding is used primarily for encoding radio signals because

the frequency spectrum of the encoded signal contains less low-frequency energy than a conventional non-return-to-zero (NRZ) signal and less high-frequency energy than a bi-phase signal.



Modified Miller: The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation data demodulation circuit for producing NRZ - L data by utilizing the clock bits, data bits and synchronizing clock pulses which are output from the data separation circuit. This structure enables the M 2 modulation data which is input to the M 2 demodulation circuit to be easily demodulated to an NRZ - L type data signal by means of a very simple circuit structure. An example is as below:





Settings

Line Encoding Settings				×
Select Encoding	n occurs for a one) 🗸	Channel	Data Channel A0	
1	1 0 0 1 1 0		Decode Range From	
Auto-Detec	t Data Rate		Buffer Head	~
Data Rate	1 MHz		To Buffer Tail	~
			ОК	Cancel

Select Encoding: Select the line code you want to encode.

Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Date Rate

is not selected.

Channel: Show the selected channel (CH 0).

Range: Select the range within the waveforms you want to encode.



Low Pin Count (LPC)

The LPC bus, for the data transmissions, was developed by Intel to replace the ISA bus.

Settings

Channe	I	
	LFRAME# A1 A1 LAD[2] A4 CLCLK LAD[0] A2 LAD[3] A5 Data Edge LAD[1] A3 \checkmark	A0 × Rising ×
	Show the field in report START CYCLETYPE +DIR SIZE TAR ADDR	~
Color		
-	START ADDR CYCTYPE+DIR DATA	~
	TAR IDSEL	~
Range	Decode Range	
2	From To Buffer Head V Buffer Tail V	
	Butter Head	

Channel: Show the selected channels.

LFRAME#: Frame indicator.

LAD[0-3]: Data bits.



LCLK: Clock.

Filter the data in the report window: You can filter the data in the Report Window.

Result

Click **OK** to run the LPC decode and see the result on the Waveform Window below.

I/O Read Cycle.

		291 ns	341 1		391 ns	441 ns	401 n:		541 ns	691 ns		341 ns	691		741 ns		701 ns
lme Div= 50 ns	START	I/O RN		ADDR: 00			· · · ·	1 1/NC: 6 SYNC	- 		<u>۱</u>	r '	SYNC: 6	T	r	SYNC: 6	
	LCLK-A0	n 15 n 15 n 1	5 n 15 n 15 n	20 ns	20 ns	20 ns 20 ns	20 ns	20 ns 20	0 ns 15 n 15	5 n 15 n 15 n	15 n 15 n	15 n 15 n	15 n 15 r	15 n 15 n	15 n 15 n	15 n 15 n	15 1
	LFRAME# - A:																
LPC Bus	LAD[0] - A2																
	LAD[1] - A3			30 ns	30 ns												
	LAD[2] - A4																
LPC	LAD[3] - A5					60 ns											
Λ, Λ	Channel (P	ø
.abel CH.00 Bus(earch All Fi	eld 🔻			^ [
Sample	Field	#Clocks	LAD					Comment				•					
40ns	START	1	0	Used fo	or Memor	y or I/O or D	MA cycles.								-		
70ns	CYCLETYPE+DIR	1	0	I/O Rea	/O Read												
00ns	ADDR	4	0064														
25ns	TAR	2	FF														
185ns	SYNC	1	6	Long Wa	ait	-											
515ns	SYNC	1	6	Long Wa	ait												
545ns	SYNC	1	6	Long Wa	ait												



Line Printer Terminal Port (LPT)

LPT is a universal parallel interface that use in PC since 1980's. It was primarily designed to operate a line printer, but could also be used to adapt other peripherals. This decode only support EPP Mode.

Settings

LPT(EPP) Setting		×
Channel A0 Data0(LSB) A0 Data[7:0] => [A7: /nWrite /nWrite A8 /nWait A9 /nDStrb A10	Color Read Ad Write Ad Read Da Write Da	Idress
/nAStrb A11	Range Recoded From To	I Range Buffer Head V Buffer Tail V
	Default	OK Cancel

Data0(LSB): There are 8 data channel. Only set Data0(LSB) here, other channel will

be set automatically.

/nWrite: Indicates the direction of transfer.

/nWait: To acknowledge that a transfer has finished.

/nDStrb: Indicates the data cycle.

/nAStrb: Indicates the address cycle.

/nInit: Indicates a termination cycle in order to return the interface to the



Compatibility mode. User can option to use this channel or not.

/nIntr: This is an interrupt signal. User can option to use this channel or not.

Result

Click OK to run the LPT Decode and see result on the Waveform Windows below.

		Ģ																				
ime Div = 100 ns		-60	6.43 us	3.	06.33 us		-606.23	15	-606.	13 us	-606	3.03 us	-6	05.93 us		-605.83 0	15 1 1	-605.	73 us	-605.63 us	-606.53 us	-605.43
		R/D:	28			R/D:64				R/D:85			R/D	:88			R/D:B			R/D:00		R/D:07
	Data0 - A1		1	65 ns			165	ns			170 n:	6			165 ns			1	70 ns		165 ns	
	Data1 - A2		11	65 ns							500 n:	в				202		1	70 ns		165 ns	
	Data2 - A3								335	ns								5	00 ns			
	Data3 - A4		1	85 ns		[335	ns							335 ns					
	Data4 - A5						1222											1	70 ns			
Bus 1	Data5 - A6				330) ns	8						335 ns					1	85 ns			
	Data6 - A7																					
	Data7 - A8						8								505 ns							
	/nWrite - A0																					
	/nWait-A10	65	ns	100 n	is			105 ns		65 ns	1	100 ns	6	5 nis	10	0 ns		ns	105 ns	.65 n	s 100 ns	
	/nDStrb - A13	65 ns		100 ns		65 ns	1	05 ns	6	0 ns	105	ns	65 n	s	100 n	IS	65 ns		105 ns	60 ns	105 ns	65 ns
LPT	/nAStrb - A16																					
₩, ₩																						P
_abel	Channel	4																				
CH-00 Bus		1																(Q Search	All Field	-	~
Sample	R/W	Addr/Data	DO	D1	D2	D3	D4	D5	D6	D7	DØ	D9	D10	D11	D12	D13	D14	D15	AS	CII		
606.490000	Read	Data	2B	64	85	88	BB	00	07	FF	F3								+d			
-15ns	Write	Address	A5																×			
541.3200000	Write	Address	F2																•			
.074255000	Write	Address	F6																÷			
.615590000	Write	Address	FO																2			
						1					1										1	
2.197460000	Write	Address	A7																•			



M-Bus

M-Bus (Meter-Bus) is for remote reading of heat meters and other types of consumption meters.

Settings

MBus Settings					×
Channel	Channel Master Polarity Slave Polarity	A0 Auto A1 Idle low		Auto Detect Baud Rate 9600 Parity None MSB first Adv. report	~
Color	User can assi Start / Stop L Field C Field A Field	gn color for s	CI Field Data Check S		
Range	From Buffer Head	~	To Buffer T	ail 🗸	
		Def	fault	ОК	Cancel

Channel: Set the channel of the signal and Polarity.



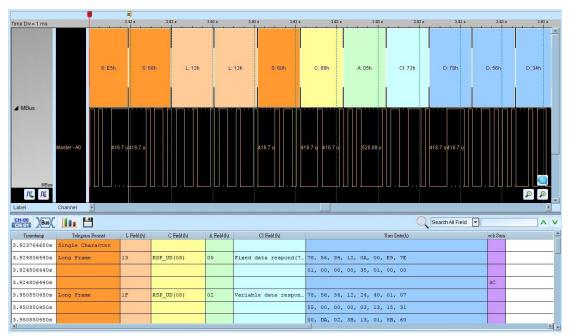
Baud rate: Set the specific data rate or auto detection.

Parity: Error detection.

MSB first: Set MSB format.

Adv. Report: Advanced report.

Result





Math

Math is used to conduct addition, subtraction, multiplication, division, AND, XOR,

OR,NAND, NOR, XNOR operation for the channel or combined channels.

Settings

te List Item
e

Operand: Select the channel(s) in the waveform window.

"+": Select "+", "-", "X", "/", "AND", "XOR", "OR", "NAND", "NOR", "XNOR" operator.

"=": Add operation type.

Add List Item to Operand: Add operation type to operand.

Delete List Item: Delete operation type from the list.

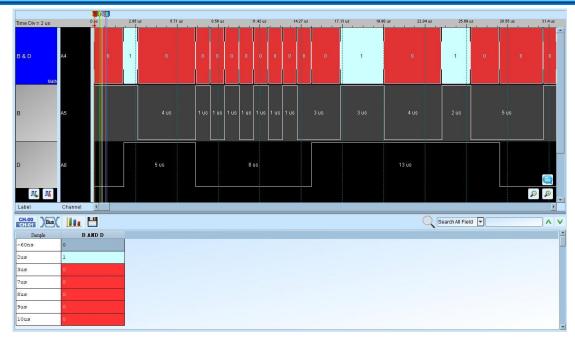
Color: Set the colors for the data bits.

Range: Select the range within the waveform you want to decode.

Case Settings: Select condition and frame color.

Result





Note: When the Math settings are finished, the settings will always be saved as an independent text file named as AqMath.txt, different from the waveform file, at work directory unless other name assigned. If you need the specific Math settings, please save it, so you can reload the settings next time you open the specific waveform file.



Mobile Display Digital Interface (MDDI)

The Mobile Display Digital Interface (MDDI) is a cost-effective low-power solution that enables high-speed short-range communication with a display device using a digital packet data link for connecting portable computing, communication, and entertainment devices to wearable micro displays. This decoder is based on VESA Mobile Display Digital Interface Standard Version 1.2, only Type I communication is supported in this decoder.

1. MDDI Parameter Settings

MDDI Set	ttings				×
Channel :	Settings	CH 2 •	⊂ MDI ● MDI	CLLO	•
Color —					
	Packet Length		•		
	Packet Header		•		
	Packet Data		•		
Range -					
2	Decode Range				
	From		То		
	Buffer Head	-	Buffer Tail	-	
			Default	ОК	Cancel

Channel Settings

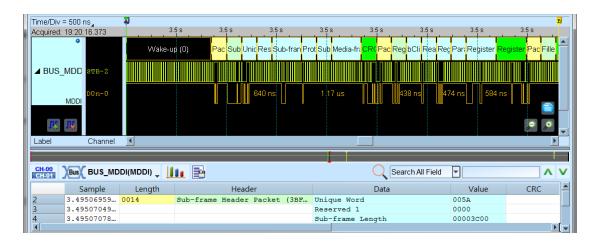
MDDI STB: MDDI Strobe MDDI D0+/-: MDDI Data 0 +/-

Configure the Channel setup for the decoder, and choose the data source



from Data 0+ or Data 0-.

2. Result





MDIO

MDIO, also known as Serial Management Interface (SMI), is a serial bus defined for the Ethernet IEEE 802.3 specification for Media Independent Interface, or MII.

Settings

MDIO S	ettings						×
Setting		Data Clock (MDC)	A0 •	Color	Preamble (PRE) Start of Frame (ST)		<u> </u>
	Management Preamble	Data Input/Output (MDIO)	A1 •		OP Code (OP) PHY Address (PHYADR) Register Address (REGADR)		
Range	Data Data Edge	Rising	○ Falling		Turnaround (TA) DeviceType (DEVTYPE) Address (ADDR)		
8	Decode Range From To	Buffer Head Buffer Tail	*		Data (DATA)		~
					Default	OK	Cancel

MDC: Clock.

MDIO: Data Input / Output.

Preamble: Set the MDIO preamble width, 32 bit default.

Data Edge: Set the MDC Rising/Falling edge to latch the data field, Rising Edge default.

Result

Click \mathbf{OK} to run the MDIO decode and see the result on the Waveform Window

below.



fime Div = 2 us		3.16 us	5.16 us	7.16 us 9.16 us	11.16 us 13.16 us	15.16 us 17.16 us	19.16 us 21.16 us 23.16 us
		ST. Clause22	OP	Read	PHYADR: 07	0	REGADR: 16
⊿ SMI	MDC-A1	970 ns 970 ns 971) ns 970 ns 970 n	s 965 ns 975 ns 965 ns 1	975 ns 965 ns 975 ns 965 ns 975 n	ns 965 ns 970 ns 970 ns 97	0 ns 970 ns 970 ns 970 ns 970 ns
	MDIO - A2	3.87 us					
MDIO						7.75 us	1.96 us
MDIO NL NL Label	Channel •	3.0/ US		5.83 us			ا م م
MDIO TL TL abel CH-00 CH-0	Channel) () ()
MDIO AL abel CH-00 CH-00 Sample	Channel 🗴	OP	PHYADR	REGADR	DATA DATA: 0382		الله الله الله الله الله الله الله الله
MDio AL AL abel CH-00 Bus Sample 61.0950000	Channel I	OP Read	PHYADR 07	REGADR	DATA: 03E2) ۾ ۾ ا
MDIO AL AL Abel Sample 61.0950000	Channel I ST Clause22 Clause22	OP Read Read	PHYADR 07 07	RE0ADR 16 16	DATA: 03E2 DATA: 03E2		ا م م م
MDIO AL AL Abel CHION (MARCHAR) CHION (MARCHAR) CHION (MARCHAR) Sample -61.0950000 25.0900000 25.0900000	Channel 4 ST Clause22 Clause22 Clause22 Clause22	OP Read Read Read	PHYADR 07 07 07	RE0ADR 16 16 17	DATA: 03E2 DATA: 03E2 DATA: 2040) ۾ ۾ ا
MD0 (1, 1, 1, Label CH-00 (Bus) Sample -61.0950000 125.090000 311.2750000 199.3950000	Channel Channel Chause22 Clause22 Clause22 Clause22 Clause22 Clause22	OP Read Read Read Read Read	PHYADR 07 07 07 07	RE0ADR 16 16 17 16	DATA: 03E2 DATA: 03E2 DATA: 2040 DATA: 03E2		ا م م م
MDIO I I I I I I I I I I I I I I I I I I I	Channel Channel Chause22 Clause22 Clause22 Clause22 Clause22 Clause22 Clause22 Clause22	OP Read Read Read	PHYADR 07 07 07	RE0ADR 16 16 17	DATA: 03E2 DATA: 03E2 DATA: 2040		ا م م م



MHL-CBUS

Mobile High-definition Link (MHL) is an HD audio and video interface, Control Bus (CBUS) is used to control it.

Settings

CBUS Setti	ngs		×
Channel	Channel CBUS A0 ~	Color SYNC	
Range	Decode Range	HEADER cPacket dPacket v	
H-H	From Buffer Head V To Buffer Tail V	CMD / DATA	
		Arbitration V Default OK Canc	cel

LA Channel: Show the selected channel (CH0).

Result

Click OK to run the MHL-CBUS Decode and see result on the Waveform Window below.



		1.5 :		.6 s	1.6 s	1.5 s 1.	Ss	1.6 s	1.6 s		5 5	1.6 s	1.6 s	1.5 s
Time Div = 2 us			· ·		1.0 5		<u> </u>					1.05		
CBUS		— AR	B_SRC		SYN	C DDC(00)	¢Packet			STOP(51)			P:OK	ACK
	MHL-CBUS-		1.2 us	1.15 us	1.55 us	1,05 us 1.05 us	1	.05 us	1.05 us	1.05 u	s 1.05 us 1.()5 ús	1.4 us	
MHL-CBUS														۵
ALABEI	Channel	4												<u>م</u> م
ur ur	Channel										C Search A	II Field 💌		
Λ, Λ.	Channel			SRC Pecket		SINK Packet			Information		Search A	II Field 💌		ŀ
ALABEI CH-00 CH-01 Sample	Channel	<u> </u>	STOP (51)	SRC Packet		SINK Packet			Information		Search A	II Field 💌		ŀ
Label CH-00 CH:01 Bus	Channel Channel Header DDC (00)	Сы	STOP (51) EOF (32)	SRC Packet		SINK Pecket			Information		Search A	II Field 💌		ŀ
AL ALE Label CH-00 CH-01 Sample 1.4988268505	Channel Header DDC (00) DDC (00)	Cttl CPacket	EOF (32)	SRC Packet		SINK Packet			Information		SearchA	II Field 💌		ŀ
M. M. Label Bus CH-00 Bus Sample 1.498826850s 1.498843800s 1.498936050s	Channel Header DDC (00) DDC (00)	Ctil CTacket CPacket	EOF (32)	ead SOF(30)		SINK Packet			Information		Search A	II Field 🔻		ŀ
AL AL Label Sample 1.498826850s 1.498936050s 1.498936050s 1.498930050s	Channel Header DDC (00) DDC (00) DDC (00)	Chil CPacket CPacket CPacket	EOF(32) Segment R	ead SOF(30)		SINK Packet			Information		Search A	II Field 💌		ŀ
M. M. Label Bus CH-00 Bus Sample 1.498826850s 1.498843800s 1.498936050s	Channel	Ctil CPacket CPacket CPacket dPacket dPacket	EOF(32) Segment R	ead SOF(30)					Information		Search A	II Field 💌		ŀ



MII/RMII

MII/RMII (Media Independent Interface/Reduced Media Independent Interface) is a protocol formulated by 802.3u that applied to Fast Ethernet, connecting MAC of Data Link Layer and PHY layer. Its clock frequency is either 25MHz or 2.5MHz (Ethernet); they are TX_CLK and RX_CLK. TX [0:3], RX [0:3] are 4-bit-width bus and TX_EN, RX_EN enable the IN/OUT; TX_ER, RX_ER can detect the errors on the bus; RX_DV inform bus the data received is valid or not; COL can detect the collision on the bus. Serial Management Interface (SMI), also known as MDIO, is also an important part of MII.

Settings

Proto			TK and DA	TA pins used (MII	Data Data Edge	Report Data Columns
Ori	•			TA pins used (GM	- 0	 8 columns 16 columns
Mode Tra		Receive	(Rx)	Duplex (Tx+Rx)	Decode Ethernet Packet (MA	c)
Chan	1171					
1.0	ata source from [DSO - Diff				12
	nsmit(Tx)		Receive		Data	
TD -	a service of the serv	÷	RD+	P50 1 €	Error	
TD-	DSO 2	*	RD-	DSO 2 ÷	Collision	
TX_I	D1 A2	1	RX_D1	A2 *		
TX	D2 A3	-	RX_D2	A3	Idle	
0.00				· ·	Carrier Extend / False Carri indication / Status	er 📃
TX_I		-	RX_D3	▼	Preamble / SFD	
TX_I	D4 A8	*	RX_D4	A7	Range	L
TX_I	D5 A9	*	RX_D5	A8 🔺		
TX	D6 A10		RX_D6	A9	Decode Range	
TX	D7 A11	-	RX_D7	A10	From Buffer Head	To Buffer Tail
TX			RX_DV	A5	builer head	
				_		
TX_I			RX_ER	A6		
TX_	COL A7	-				



MII / RMII: Select the MII / RMII bus decode

GMII / RGMII: Select the GMII / RGMII bus decode

Only CLK and Data pins used(M/G): Select MII / GMII the CLK and Data pins

only.

Transmit (Tx): Select TX mode

Receive (Rx): Select Rx mode

Duplex (**Tx**+**Rx**) : Select duplex mode

Channel: Set the channel number.

Rising: Select rising edge to latch data

Falling: Select falling edge to latch data

8 columns: show 8 columns data field in the report window

16 columns: show 16 columns data field in the report window

Result

Click **OK** to run the MII/RMII decode and see the result on the Waveform Window below.



ΛΠ																					
me Div = 200 ns	1			II	.49 ns		i73.89 ns	<mark>'T</mark> T	859.29 ns	1.14 us	1.43 us	1.72	u T	2 us	TT TT	2.29 us	ri ri	2.57 us	пп	2.86 us	3.14 u
	RXCLK	- A0	inn	Pre	eamble		SFI									40001		7288		A 2 0 C	8 A 1 0 7
	RX_D0	- A2				1	.12 us			80 n 115 n	s 75 n	315 n	s		435 ns		80 n 80 i	n 115 ns	75 n	235 ns	
I PBus1	RX_D1	- A3							485 ns	75 n 85 n 75	n 85 n 125	ns 75 n	3	55 ns		355 ns	8	5 n 75 n	85 n 12	5 ns 115 n:	s 75 n
FIDUST	RX_D2	- A4				1	.12 us			80 n	440 ns		3	360 ns		240 n	s 80 I	1	400 ns		160 ns
	RX_D3	- A5		6	i00 ns				520 ns	80 n 80	n 80 n		280 ns		48	0 ns		0 n 80 n	80 n	80 n 120) ns
	RX_DV	-A1																			
MI / RMI	RX_ER	- A6																			Q
₩, W	Chann																				QQ
abel				_	_	_	_	_				_	_	_		0	Search	All Field	T		^
Sample	DO	D1	D2	D3	D4	D5	D6	D7			Information					~					
65ns	F	F	F	F	F	F	F	F]						
85ns	F	F	F	F	0	D	7	2													
.305000000	8	8	3	2	8	3	A	2													
.625000000	8	0	6	0	0	0	1	0													
.945000000	8	0	0	0	6	0	4	0													
		0	1	0	0	D	7	2	1												
.265000000	0	0	+	0																	



Microwire

The Microwire bus has four data bits: Chip Select (CS), Serial Clock (SK), Data Input (DI), and Data Output (DO).

Settings

MICROW	/IRE Settings			×
Channel	Channel	Color		
	Chip Select Channel (CS) A0 Clock Channel (SK) A1 Data In Channel (DI) A2 Data Out Channel (DO) A3 Data Chip Select Edge Data Edge(DI) Data Edge(DO) Rising Fall		ERASE/WRITE ENABLE ERASE/WRITE DISABLE ERASE WRITE READ ERASE ALL WRITE ALL	
	EEPROMs 93xx46A or 93xx46C, 8 Bits Report Show data in report 8 Column	Range	Decode Range From Buffer Head ~	To Buffer Tail V
2			D	efault Ok Cancel

Channel: Show the selected channels.

Chip Select Edge: Active Low or Active High.

Data Edge: Rising or Falling.

EEPROMs: Select EEPROMs.

Report: Show data in report.

Result

Click **OK** to run the Microwire decode and see the result on the Waveform Window

below.

Read



1me Div = 5 us		7.05 us	12.05 u	s	17.05 us		22.05 us	2	.05 us	32.05 us	37.05	ius 42.05	us 47.0	06 us 62.	.05 us 67.06 us
		Read	A=000	2	9	6	8	D6	T I	EB	2C	A9	03	21	BB EF
	Chip Select-														
Microwire	CLK-A1		2.5 us	3.3 us		2.2 us		2.3 us	2.2	us 2.3	us	2.2 us	2.3 us	2.2 us	2.3 us
	Data In - A2		2.3 us 2.7 us	3.1 us					2 u	is 2.7 us 2.1	us	7,4 us	2.1 us		
	Data Out - A3			4.1 us		2.4 us		3.4 us	Π.,	us 1 u 2.8 I					
MICROWIRE		_		4.1.US		2.4 05		3.4 US				2.7 us	2.5 us 1.9 us	2.8 05	2.8 us 1 u
Λ L abel	Channel (4.1 US		2.4 05		3.4 US	2.14			2.7 us	2.5 US 1.9 US		
ALL ALL	Channel (bd	Address	4.1 US		D3	D4	D5 D0		ASCHIDO-		(9 9
abel	Channel <	nd 000	Address 25	D0 D1		D3						(9 9
Abel H-00 Bus Timestamp . 900000000	Channel 🛃			D0 D1 9 6B	D2	D3 EB	2C #	D5 D6	D7	ASCII(D0-1					9 9
M. M. .abel	Channel 🛃		29	D0 D1 9 6B 8 EF	D2 D6	D3 EB 5F	2C 7 4C F	D5 D6	D7 21	ASCII(D0-1		(9 9
Image: CH-00 Image: CH-00<	Channel 🛃		25 BE	D0 D1 9 6B 3 EF 5 D4	D2 D6 5F	D3 EB 5F 51	2C A 4C F 06 4	D5 D6 A9 03 FC 10	D7 21 EC	ASCH(D0-))k,! L		(<u>۹</u> ۹
Image: CH-00 Image: CH-00<	Channel 🛃		25 BE BE	D0 D1 9 6B 3 EF 5 D4 5 8E	D2 D6 5F ED	D3 EB 5F 51 65	2C 7 4C F 06 4 53 0	D5 D 49 03 7C 10 15 4D	D7 21 EC 99	ASCII(D0-)) k,! L Q.EM.		(9 9
ALAbel	Channel 🛃		25 BE 25	D0 D1 9 6B 3 EF 5 D4 5 8E 5 3F	D2 D6 5F ED 51	D3 EB 5F 51 65 16	2C A 4C E 06 4 53 0 A7 2	D5 D4 49 03 7C 10 15 5C	D7 21 EC 99 33	ASCII(D0-))k,! L Q.EM. \$.QeS.\3		(9 9

Write

me Div = 2 us	7	01.63 ms 701	.63 ms	70	01.63 ms		701.64 m		701.64	ms	701.64 ms	701.64	ms 70	1.64 ms	701.6	i6 m s	701.66 ms	701.66 m
				Write						A=01	21				E6			
	Chip Select - 2.3 u										19 us							
Microwire	CLK-A1								2.7 us				2.6 us					
	Data in - A2								3.2	us	1.6 us		3.9 us		70	00 n		
MICROWIRE	Data Out - A3																	
abel	Channel 4																	
H-00 Bus														Qs	earch All Fi	ield 💌		^
Sample	Command	Address	DO	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7							
01.6314000	Write	0C1	E6								•							
05.2044000	Write	0C2	02															
08.7775000	Write	0C3	32								2							
12.3505000	Write	0C4	D7								•							
15.9236000	Write	0C5	SD								1							
19.4966000	Write	0C6	5E								*							



MIPI DSI

MIPI Display Serial Interface (DSI) designed by MIPI alliance for the protocols between a host processor and peripheral devices using a D-PHY physical interface. The operation mode includes High Speed Mode and Low Power Mode (LPM).

Settings

MIPI DSI Setti	ngs	×
:1	LP Mode Channel Dp A0 + Dn A1 +	HS Mode ChannelData Lane1 \square D0+ \square
 Init Color		Show DCS Command Always goes to HS Mode
Transi	of Transmission mission Mode e Mode Action	Vord Count V Data Frame V End of Transmittion
Data I	Identifier	DC5 Command
Range — Di	ecode Range From	То
	Buffer Head	Buffer Tail Default OK Cancel

Dp, Dn: DSI-LP signal lines

Data Lane: DSI-HS mode Data Lane number

Clock+, D0+, D1+, D2+, D3+: DSI-HS signal lines

Advanced Decode: Enable DSI format decode and display.

Show DCS Command: Enable DCS Command decode and display.



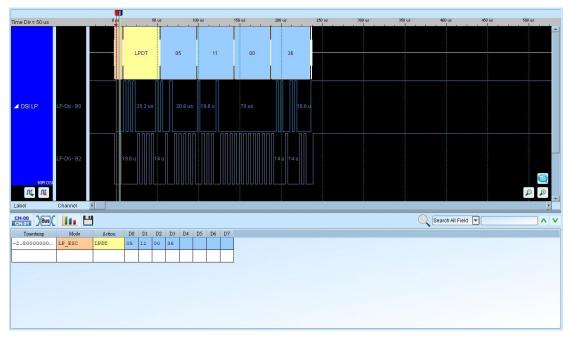
Always goes to HS Mode: Ignore the Dp and Dn status and decode all the data frame

in HS mode

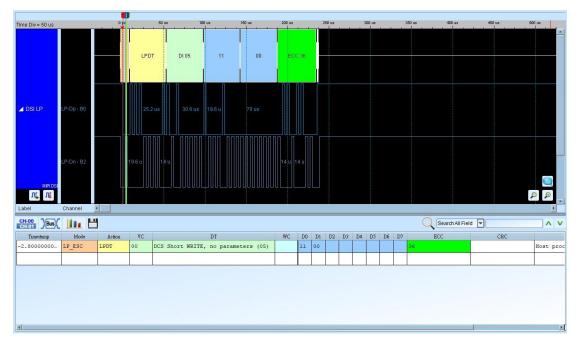
Initial Bus Direction: Select the Initial direction of the bus transmission.

Result

Advanced Decode Disabled:



Advanced Decode Enabled:





MIPI RFFE

MIPI RFFE (RF Front-End Control Interface) designed by MIPI alliance is for controlling RF front-end devices including Power Amplifiers, Low-Noise Amplifiers, filters, switches, power management modules, antenna tuners and sensors.

Settings

IPI RFFE S	ettings						>
Channel	CLK DATA	A0 •	Color	SSC SA Command BC		 Address Data P BP 	
Range	ecode Range Buffer H		то	Bu	ffer Tail	~	
					Default	ОК	Cancel

Channel: Set the channels of SCLK and SDATA.



Result



MIPI SPMI

MIPI SPMI(System Power Management Interface) designed by MIPI alliance. SPMI is a serial interface that connects the integrated Power Controller(PC) with Power management Integrated Circuits(PMIC).

Settings

MIPI SPMI Configuration	×
Channel	SDATA
Version v1.0	~
Color	
Start 📃 🗸	SSC
C-bit	Command Frame
A-bit	Data Frame
SR-bit	Parity bit
Master Arbitration	Bus Park
Slave Arbitration	No Response Frame
Range	
From Buffer Head V To	Buffer Tail 🛛 🗸
Default	t OK Cancel

Channel: Set the channels of SCLK and SDATA.

Result

Click OK to run the MIPI SPMI Decode and see result on the Waveform Windows



			0 ps	F) 600 ns	1 us	1.5 us	2 us	2.	ius 3us	3.5 us	4 us	4.6 us	ő us
ime Div = 500 ns			Start	MPL3 -	A:00	CMD:38	56	46	P 00				
d Bus 1	SCLK-A0			440 ns									
	SDAT- A1		265 ns	315 ns									
MIPI SPMI		4	205 115	313115	520 ns	160 n 260 n	s	155 n	685 ns				
W M			203 115		520 ns	160 n 260 n	s	155 n	685 ns				Q
AL AL	Channel	8	200 115		52UNS	160 n 260 n	s	155 n	685 ns				
AL AL	Channel	•			52Uns	160 n 260 n	s	155 n	685 ns	Q Searc	th All Field		
International Action of the second se	c	H A	SR	Device Address(Hex)		Comm	nand (Hex)		Dem Address - High(Hex)	Data Address - Low(Hex)	Data Frame (He		<u>.</u>
ALE I	c	Н	SR	Device Address(Hex)		Comm							<u>.</u>
Abel H-00 Bus Timestamp Cons	c	H A	SR	Device Address(Hex) Sh=00	38 (Extend	Comm ed Registe	nand (Hex)	1Bytes)	Dem Address - High(Hex)	Data Address - Low(Hex)	Data Frame (He		<u>.</u>
AL AL	c	A MPL3	SR	Device Address(Hex) SA=00 SA=00	38 (Extend 30 (Extend	Comm ed Registe	nand(Hex)	1Bytes) : 1Bytes)	Data Address - High(Hex) S6	Data Address - Low(Hex) 46	Data Frame (He		<u>.</u>
NL NL abel	c	A MPL3 MPL3	SR	Device Address(Hex) SA=00 SA=00 SA=00	38 (Extend 30 (Extend 38 (Extend	Comm ed Registe ed Registe ed Registe	nand(Hex) er Read Long: er Write Long	1Bytes) : 1Bytes) 1Bytes)	Data Address - High(Hex) S6 S6	Data Address - Low(Hex) 46 46	Data Frame (He		<u>.</u>
AL AL abel Bus (H-00 Bus (Timestamp Cons .64500000 18.4450000 28.0300000 Cons	c	A MPL3 MPL3 MPL3	SR	Device Address(Hex) SA=00 SA=00 SA=00 SA=00 SA=00 SA=00	38 (Extend 30 (Extend 38 (Extend 30 (Extend	Comm ed Registe ed Registe ed Registe	and(Hex) er Read Long: er Write Long er Read Long:	lBytes) : lBytes) lBytes) : lBytes)	Data Address - High(Hex) 56 56 57	Data Address - Low (Hex) 46 46 46	Data Frame (He 00 80 00		
AL AL	c	A MPL3 MPL3 MPL3 MPL3	SR	Device Address(Hex) SA=00 SA=00 SA=00 SA=00 SA=00 SA=00 SA=00	 38 (Extend 30 (Extend 30 (Extend 33 (Extend 33 (Extend 	Comm ed Registe ed Registe ed Registe ed Registe ed Registe	aand(Hex) er Read Long: er Write Long er Read Long: er Write Long	lBytes) : lBytes) : lBytes) : lBytes) 1Bytes)	Dah Addren - High(Hex) 56 57 57 57	Data Address - Low(Hex) 46 46 46 46 46	Data Frame (He 00 80 00 80		<u>.</u>

below.



MMC

The Multi Media Card (MMC) or the Embedded Multi Media Card (eMMC) version 5.1 is a flash memory card standard.

Settings

MMC Set	tings								×
Channel						Color			
1	Channel				Analysis				
:	CLK	A0	∼ Data3	A5 🗸	 Command only Data only Command + Data 		Start bit		
	CMD	A1	✓ Data4	A6 💛	Command + Data Command		Host		
	Data0	A2	Uata5	A7 ~	Adv. Report		CMD/Resp		
	Data1	A3	Data6	A8 ~	Data 8-bit Data		Argument CRC check		~
	Data2	A4	Data7	A9 🗸	 4-bit Data 1-bit Data DDR mode 		End bit		~
	DS	A10	~		Non-interleaved		Data 📃 📃		
	Data leng	ith					Busy		~
	513	2	Bytes (Min:	1, Max: 16384)					
Range	Decode F	Range From		То					
		Buffer H	ead 🗸	Buffer Tail	~				
						[Default (DK Cance	3

Channel: Show the selected channels.

Command only: Analyze the command.

Data only: Analyze the data

Command + Data: Analyze Command and Data in the report window.

Ref. DAT0: To help analyze the R1/R1b of the response.

Adv. Report: To analyze the command argument.

Don't care clock: To decode only depend on the CMD channel without the CLK

channel.



Data: 1/4/8 bits or DDR mode, check "DDR mode" and " "Non-interleaved" to analyze data without interleaved. Check "Data Strobe" to analyze data with the DQS channel.

Data length: Set the number of data bits.

Result

Command:



Adv. Report:



lme Div= 20 ns			4.96 s	4.96 s	4.98 s	4.96 s	4.96 s	4.98 s	4.96 s	4.96 s	4.96 :		4.96 s	4.96 :
		- ci	WD23'SET_BLC	ICK_COUNT		Data:00h		Data:00h			Data:00h		Data:	08h
■ BUS_MMC	CLK- B7													
	CMD - 823			18.33 ns				16	7.9 ns					
ммс	0													
MMC TL TL	Channel	¢.												<mark>ا</mark> ۹ ۹
ммс Л. Л.	Channel										Search All Fiel	dv		
ммс Л. Л.	Channel				Response		 Δη	gument (h)		Q CRC7 (id 💌	Timing	
MMC M abel H-00 Bus(Timestamp	Channel	L Command			Response	00 01				CRC7 (equency		
AMC Abel abel Timestamp 06.7101046	Channel	L Command			Response			gument (h)			h) Fre	equency	Timing	
MMG Abel Heol Timestamp 06.7101046 06.7101046	Channel	L Command		R2 :Check b	-	Bit [31	00 00	gument (h)			h) Fre	equency z	Timing	
Mile Abel Timestamp 06.7101046 06.8553872	Channel	L Command			-	Bit[3] D0 OF	00 00 :16] RCA: 000:	gument (λ) Lh 7 81 85 11 95	4D 49 5B .	Fl	h) Fra 384KH	equency z	Timing Nrc: 74	
ADD ADD ADD ADD ADD ADD ADD ADD	Channel	L Command			-	Bit[31 D0 OF [127:1	00 00 :16] RCA: 000: 00 32 OF AD A	rument (b) Lb 7 81 85 11 95 TURE: Version	4D 49 5B . 1s coded .	Fl	h) Fra 384KH	equency z	Timing Nrc: 74	
MMC TL TL Label CH-00 CH-01 CH-0	Channel	L Command			-	Bit[31 D0 0F [127:1 [125:1	00 00 :16] RCA: 000: 00 32 OF AD A 26] CSD_STRUCT	gument ()) ib 7 81 85 11 95 UURE: Version : Version 4.1	4D 49 5B . 1s coded .	Fl	h) Fra 384KH	equency z	Timing Nrc: 74	

Data:

Tme Div = 5 ns		4.95	s	4.95 =		4.95 s		4.95 =	4.9	5 5	4.95 =		4.95 =	4.92	5 5 1 1	4.95 =		4.95 s	4.95
			Start	Ris	e:B1h Fa	ill:A9h Ri	se:EEh F	all 5Dh	Rise:A0h	Fall:19h Ri	se:C4h Fa	II:A2h Ri	se:5Fh F	all:EDh F	Rise:D5h I	all 2Bh F	Rise:3Fh	Fall:E8h	Rise:95h
	CLK- 87	3.33 ns 2	92 ns 2	.92 ns 2	.92 ns	2.92 ns	2.92 ns	3.33 ns	2.92 ns	2.92 ns	2.92 ns	2.92 ns	3.33 ns	2.92 ns	2.92 ns	2.92 ns	3.33 ns	2.92 hs	2.92 ns
	CMD - 823								_			,							
	Data0 - B16 📒			5,83	ns		3.33 ns		3.33 n	5.1				15 ns				s	
	Data1 - B21		12.08	Bins		2.92 ns		11	.66 ns		5.83	ns		5 ns	6	25 ns	5.	42 ns	
4 500 400	Data2 - B22		12.00	8 ns		5.	83 ns	5	83 ns	2.92 ns	3.39 ns		8.75 ns		3.33 ns	2.5 ns			_
▲ BUS_MMC	Data3 - B6		8.75 ns			9.17 ns		2.92 ns	3.33 n	5.1	83 ns	5.8	33 ns	2.92 ns		9.17 ns		٦.	6.25 ns
	Data4 - B17	6.25	ns	2.5 ns	5.83		3.33 ns	2.92 ns	3.33 n	s 5.1	83 ns	2.5 ns	3.33 ns	2.92 ns	2.92 ns	3.33 ns	2.92 n	s 2.92 n	3
	Data5 - B18	5.83	ns [8.75 ns		3.33 ns	2.5 ns	6.2	5 ns	2.92 ns	2.92 ns	3.33 ns	2.5 ns		9.58 ns			
	Data6 - B19		11.67			6.2	5 ns	5	83 ns	2.92 ns	3.33 ns		8.75 ns		5		3.33 ns	2.5 ns	3.33 ns
	Data7 - B20	5.83			9.17 ns			2.92 ns	2.92 ns	6.2	5 ns	2.5 ns		5 ns	5,1	33 ns		25 ns	
MMC	DS - 84	2.92 ns	2.92 ns	2.92 n	2.92 ns	2.92 ns		2.92 ns	2.92 ns	2.92 ns	3.33 ns	2.92 ns		2.92 ns	2.92 ns	2.92 ns		2.92 n	3,33
JL JL																			PP
Label	Channel 4																		
CH-00 Bus														() Sear	ch All Field	T		
Sample	Data	D000	D1(h)	D2(h)	D3(h)	D4(h)	D5(h)	D6(h)	D700			Information			-	ASCII			
.946205516s	Jun	2000	5100	2200	2500	Digg	2500	2000		RCIE OR!		morman				noon			
.946205829s	D[0:7]	Bl	A9	EE	5D	A0	19	C4	A2 I	lac: 14,	Read dat	a block	: 114]		_		
1.946205852s	D[8:15]	5F	ED	D5	2B	3F	E8	95	47	DLY: Dat	[0:7]=[]	.0,10,10	,11,10,	10,10,1	0]+	?G			
.946205877s	D[16:23]	OF	3B	F3	6A	6F	16	A4	C6							»			
.946205901s	D[24:31]	44	53	A7	5F	ED	9D	A9	94						DS.				
	D[32:39]	78	5F	ED	B5	FO	F4	08	AO						x				
4.946205925s																			



ModBus

Modbus is a serial communications protocol published by Modicon in 1979 for use with its programmable logic controllers (PLCs). Simple and robust, it has since become one of the standard communications protocols in the industry, and it is now amongst the most commonly available means of connecting industrial electronic devices.

Settings

Modbu	is Settings				×
Setting	Channel Modbus (Tx)	A0 •	Header Start Address		> > >
	Transmission Mode	Ortu	Function Data LRC		~
	Protocol Setting Polarity Baud Rate Auto Parity	Auto ~ 9600 ~ None ~	CRC Parity Stop Trailer		> > > > >
Range	Show scale in the way				
	From Buffer Head V	To Buffer Tail V	 Default	OK Car	ncel

Channel: Modbus (Tx) or Modbus (Rx).

Transmission Mode: ASCII and RTU mode.

Auto: Auto detection idle polarity.



Idle high: Idle condition shows High.

Idle low: Idle condition shows Low.

Auto Detect: Set the Baud Rate manually if not selected.

Baud Rate: Data rate (bits per second), and the range is 110 ~ 2M (bps).

Parity: N-None Parity, O-Odd Parity, E-Even Parity.

MSB First: The default is LSB first; click it to change to MSB first.

Show scale in the waveform: Display the waveforms with scales.



Result



NAND Flash

NAND flash uses tunnel injection for writing and tunnel release for erasing. NAND flash memory forms the core of the removable USB storage devices known as USB flash drives, as well as most memory card formats and solid-state drives available today.

Settings

NAND	Flash Settings					×
Setting	Channel Device Width () I/O Quick Sett I/O User Defin I/O0 (LSB) I/O [A	up ned A0 • 77:A0]	#CE/RB x1 x2 CE#0 A12 CE#1 A0 CE#2 A0 CE#3 A0	x4 R/B#0 A13 ▼ R/B#1 A0 ▼ R/B#2 A0 ▼ R/B#3 A0	Model HY HY HY HY HY	on nix 275F081G2A 275F161G2A 275F162G2B 27JC984G2M 27JG088G5M 27JG088G5M 27JG088G5M
	CLE ALE RE# WE# DQS Command Latch C tDS >= 5.0ns	A8 A9 A10 A11 A0	The Flash Startup n Toggle / ONFI Data Out Cycles tREA >= 20.0ns		Color Commar Address Busy Data In Data Out	
	Don't care R/B#	ata Output / Input	Timing Rever	rse RE#(W/R#) rse DQS care CE# signal care ALE signal	Decode Ra From To Default	Buffer Head V Buffer Tail V

Channel:

Async	Ssync	Description
I/Ox	DQx	NAND Flash data channels
CLE	CLE	Command Latch Enable channel
ALE	ALE	Address Latch Enable channel
RE	W/R	Read Enable and Write/Read channel



WE	CLK	Write Enable and Clock channel
RB#	RB#	Ready/Busy channel
CE#	CE#	Chip Enable channel
	DQS	Data Strobe channel

Device Width: Select 8/16 bits device width.

The Flash Startup mode: Check Toggle /ONFI DDR Mode to run synchronous data interface.

I/O Quick Setup / I/O User Defined: Only set I/O0 (LSB) when select the I/O Quick Setup, other channels will be set automatically. when check the I/O User Defined and press the button will show the dialog below:

I/00	A0	•	I/08	A14	+
I/01	A1	-	I/O9	A16	*
I/02	A2	-	I/O 10	A19	*
I/O3	A3		I/011	A18	+
I/04	A4		I/O12	A17	÷
I/O5	A5	•	I/013	A20	*
I/06	A6		I/014	A14	*
I/07	A7		I/O15	A15	-

User can set NAND I/O channel by channel.

The Flash Startup mode: Check Toggle /ONFI DDR Mode to run synchronous data interface.

tREA / tDQSQ: Set the delay time to access the NAND data under SDR / DDR.

To adjust the tREA/tDQSQ when the data out value of NAND Flash is invalid.

Save the NAND Flash Data: Save the read/write data. Program will save the NAND

Flash read/write data as a file when check Save the NAND Flash Data. It will be

saved into the LA work directory.



mode.

Reduced Report: Only show NAND Flash command in the Report window when check it.

Show the DDR Data Output/Input Timing: Only show timing information under

DDR mode.

Reduced Command in the waveform window: Only show NAND Command value

in the waveform window.

Reverse RE# (W/R#) / Reverse DQS: Check this when connect the RE / DQS#

under DDR mode.

Don't care ALE/RB#/CE# signal: Ignore the signal selected when decode.

Description of file name as following:

File Name	Description
NF_DI/NF_DO	NAND Flash Data In / Data Out
_Rowxxxxxh	Row Address
_Colxxxxh	Column Address
CEx	Active CEx
_1, _2, _3	File Order

Ex:NF_DI_Row017821h_Col0000h_CE1_1.bin

NF_DO_Row017821h_Col0000h_CE1_2.bin

NF_DO_Row_Col_CE1_3.bin

Compare the content of file with the one of report.



DO	Dl	D2	D3	D4	D5	D6	D7
5A	A6	6F	36	B2	38	B8	B7
06	8A	B7	0B	Bl	19	C8	21
7E	CE	58	EF	BD	18	47	70
5E	DD	9A	E3	A5	E4	02	11
E9	2D	96	14	86	32	CE	F4
53	10	60	79	EA	B6	D6	CE
5A	22	53	A5	Fl	9E	DB	58
8A	73	B3	B1	82	19	B9	46
92	25	76	EA	E4	CE	74	A7
10	E5	20	ЗD	9F	74	BB	E5
55	54	68	4C	69	86	AC	OF

000000	5A	A6	6F	36	B2	38	B8	B7	06	8A	B7	ØB	B1	19	C8	21
000010	7E	CE	58	EF	BD	18	47	7C	5E	DD	9A	E3	A5	E4	02	11
000020	E9	2D	96	14	86	32	CE	F4	53	10	60	79	EA	B6	D6	CE
000030	5A	22	53	A5	F1	9E	DB	58	8A	73	B 3	B1	82	19	B9	46
000040	92	25	76	EA	E4	CE	74	A7	10	E5	20	3D	9F	74	BB	E5
000050	55	54	68	4C	69	86	AC	ØF	F1	A2	47	FA	37	4B	04	ØD

Device information

Vendors: Select the NAND Flash Vendor. Please refer to the

following details when select the **Custom** item.

Model: Select the NAND Flash device type.

Custom: Users create a AqNFCustom.txt file into the LA work directory when

select the **Custom** vendor item and edit NAND Flash Command set.

```
Manufacturer=Samsung
PartNo=K9XXXXXXXX
#CE/RB=1
X16=N
SyncMode=Y
Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30
Cmd=Read Status, Read Stat., , , , , Y, N, Y, 70
Cmd=Two-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000, N, Y, N, 80, 11, 81, 10
```

Manufacturer, PartNo, #CE/RB, X16, SyncMode, Cmd are keywords.

Keyword	Description
Manufacturer	NAND Flash Vendor.
PartNo	NAND Flash IC Model.
#CE/RB	Number of targets, only 1/2/4 acceptable.
X16	8/16 bits device width, only Y/N acceptable.
SyncMode	Only Y/N acceptable, Y: Synchronous data interface supported; N:



	Not supported.						
	Cmd is composed of several parts, it's divided with comma.						
	1. Complete command name.						
	2. Abbreviation of command.						
	3. Name of first busy time check. Put a space and add a comma if unused.						
	4. Value of first busy time check. Its unit is micro seconds. Put a space and add a comma if unused.						
Cmd	5. Name of second busy time check. Put a space and add a comma if unused.						
	6. Value of second busy time check. Its unit is micro mseconds.Put a space and add a comma if unused.						
	7. First flag. It's acceptable command during busy.						
	8. Second flag. It can be inserted by some command or not.						
	9. Third flag. It can insert into some multi plane command or not.						
	10. Command.						

Ex: Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30

Cmd=Read Status, Read Stat., , , , , Y, N, Y ,70

Cmd=Two-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000,

N, Y, N, 80, 11, 81, 10

Read Status / Two-Plane Page Program : complete command.

Read Stat. / TPP Prog. : abbreviation of command.

Busy Time Check(tDBSY, 1, tPROG, 5000) : tDBSY is 1us; tPROG is

5000 us. It will show some information when violation of busy time.

3 Flags: 1st flag of "Read Status" is Y means it's acceptable command

During busy; 2nd flag of "Two-Plane Page Program" and 3rd flag of "Read

Status" means any command between 11h and 81h is prohibited except



"Read Status (70h)".

Result

		2.61 ms	2.61 ms 2.61	1 ms	2.61		2.61 r		0.01	2 ms	2.65		2.62		2.62 r		2.62 m	200	
ne Div = 1 us				11-1		1 1 1		1 -	-1'	<u> </u>	· · · · ·	1					<u> </u>		2.62
		DO: CO	Col. 00 Col. 1	UU Row 54	4 Row 2E		DI: 8	E DE 34	4 DI:8		_	1			1		R	I: E0 DI: 1	11
	1/OD - A7				715 ns	005		705	745	700	1.44		1.44 0					ns 720 ns	
	1/01 - A8 1/02 - A9			1.44	4	965 ns 965 ns	1	2.15 us	715 hs	1	2.16 us		715 ns A.	0 ns 720		5 ns /1: 0 ns	sins 7201		
	1/02 - A9			-			- D	725 ns	715 nc		2.16 us		720 ns	1.44 US		u ns			
	1/04 - A11			715 ns		2.4 us		720 ns		2.16 us		720 ns		6 us	72	0 ns	2.16	115	Ħ
	V05-A12				720 ns	1.68		L	2.16 us			_	720 ns 7				ô us	720 ns	
CLE	I/06 - A13	1.54 us	2,65 us	715 ns		3.12			1.4	i	-	2.16 us			1.44 us		1.44 us		
	V07-A14	2.74 us		3.85 us			715 ns	1.44		720 ns	1.44	us [2.	6 us		1.44 us		.44 US	1
	CLE - A0	1.07 us																	
	ALE - A1		3.8	4 us															
	WE#-A5	565 n			a - 1	an a			a 90							82 6		90 - 13 - 18	
	RE# - A2	605 ns 7	15 ns 485 n 485 n 48	5 n 485	n 485 r	n475 n48	5 n 48:	5 n 485	5 n 48	5 n 48	5 n 485	m 485	n 485 n	485 n	485 n	485 n	485 n	485 n 48	15 n
	CE#1 - A6	605 ns 7	15 ns 485 n 485 n 48	5n 485	n 485 r	n475 n48	5 n 48:	5 n 485	5 n 48	15 n 48	5n 485	n 485	n 485 n	485 n	485 n	485 n	485 n	485 n 48	15 n
NAND Flast	CE#1 - A6	605 ns 7	15 ns <mark>485 n</mark> 485 n 48	5n 485	n 485,r	n475 n48	5 n 48:	5 n 485	5 n 48	15 n 48	5 n 485	(n) <u>485</u>	n 485 n	485 n	485 n	485 n	485 n	485 n 48	(5 n
NAND Flash	CE#1 - A6	605 ns 7	15 ns <u>485 n</u> <u>485 n</u> <u>48</u>	5 n 485	n 485'r	n475 n48	5 n 48	5 n 4 85	5 n 48	<u>5 n</u> 48	5 n 485	(n) <u>485</u>	n <u>485 n</u>	485 n	485 n	485 n	485 n	485 n 48	C
W M	CE#1 - A6	605 ns 7	15 ns <u>485 n</u> <u>485 n</u> <u>48</u>	5n 485	n 485 <i>:</i>	n475 n48	5 n 48:	5 n 485	5n 48	5n 48	5 n 48:	(n) <u>485</u>	n <u>485 n</u>	485 n	485 n	485 n	485 n		C
n , n abel	CE#1 - A6 R/B#1 - A4 Channel		15 ns <u>#85 n</u> <u>#88 n</u> <u>#8</u>	5 n 485	n <u>485</u> r	n475 n48	5 n 48:	5 n 485	5n 48	5n 48	5 n 489	(n) <u>485</u>		485 n	485 n	485 n	485 n		(
abel	CE#1 - A6 R/B#1 - A4 Channel					n 475 n 48 Feature Add			5 n 48	5 n 48	5 n 483	(n) <u>485</u>			485 n				
ALE OLIVITATION	CE#1 - A6 R/B#1 - A4 Channel		15 ns <u>#85 n</u> <u>#85 n</u> <u>49</u> Row Address(h)									С	Search	All Field				Q	
Abel H-00 Bus Timestamp . 527695000.	CE#1-A8 R/B#1-A4 Channel (UUL C	Command ram \$2(10)							DO			С	Search	All Field				Q	
Image: Non-State Image: Non-State Timestamp .527695000 .606515000	CE#1-A6 R/B#1-A4 Channel	Command ram \$2(10)							DO			С	Search	All Field			· A	Q	
M. M. abel	CE#1-A8 R/B#1-A4 Channel Channel Page Prog Read Stat	 ≤ Command Command Use (70) 	Rov åddress(i)						DO	D1	D2	D3	D4	All Field	D6		· A	SCII(D0-D7)	
M. M. abel	CE#1-A8 R/B#1-A4 Channel Channel Page Prog Read Stat	 ≤ Command Command Use (70) 	Row &ddress(h)	0000				C0 8E	D0	D1	D2 6E	D3	V Search D4 03	All Field D5 31	D6	E0	· · · · · · · · · · · · · · · · · · ·	SCII(D0-D7)	
abel	CE#1-A8 R/B#1-A4 Channel Channel Page Prog Read Stat Page Prog	 ≤ Command Command Use (70) 	Rov Address(i) 002E54 002E54	0000 0008				C0 82 83	D0	D1 34 34	D2 6E 63	D3 E0 E0	D4 D4 03 83	All Field D5 31 30	D6 BE BE		× A .4n. .4c. .2	SCII(D0-D7)	
Image: Control of the second	CE#1-A6 RD#1-A4 Channel Page Prog Read Statt Page Prog	 ≤ Command Command Use (70) 	Row Address(0) 002E54 002E54 002E54	0000 0000 0008 0010				C0 82 83 83	D0	D1 34 32 31	D2 6E 63 83	D3 E0 E0 E0	Search D4 03 83 03	All Field D5 31 30 31	D6 8E 8E 6E	E0 E0 E0	× A .4n. .4c. .2	.1	



NEC IR

It needs only one channel to analysis NEC signals.

Settings

NEC Sett	ings			?	×
Channel	NEC Channel	Color	Leader Address Address Command Command Repeat Stop		
Range	Decoded Range From Buffer Head V	To Buffer Tail	~		
		Defau	lt OK	Cancel]

Channel: Display the channel (CH 0).

Extended Mode: It integrates /Address and Address into 16 Bits Address, /Command

and Command into 16 Bits Command.

Display without idle in report: It will not idle on the Report Window for the user to

observe and analyze data.

Swap Bits: Switch LSB First to MSB First.

Auto: Shows High or Low when auto detection Idle.

Idle high: Idle condition shows High.

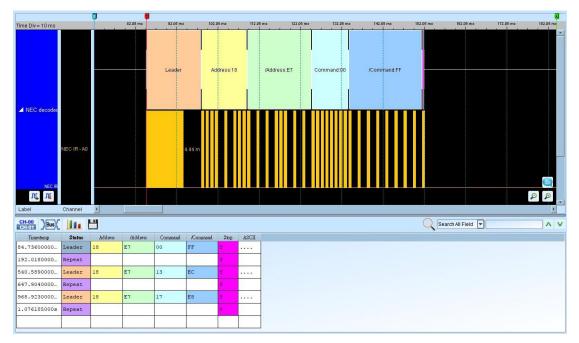
Idle low: Idle condition shows Low.



Result

Click \mathbf{OK} to run the NEC IR decode and see the result on the Waveform Window

below.





PECI

Platform Environment Control Interface, Platform management include thermal, power and electrical error monitoring.

Settings

PECI Settin	ngs	×
Channel	Channel Report mo Data A0	
Color		
	Sync	~
	Address	~
	WL/RL	` ~
	FCS	~
	Data	~
Range		
2	Decode range	
	From To	
	Buffer Head V Buffer Tail	~
	Default OK	Cancel

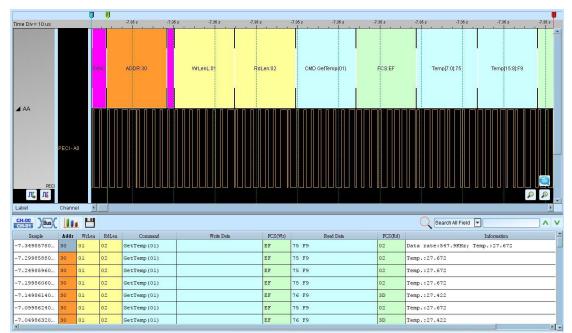
Channel: Show the selected channels.

Report mode: Normal or Advance

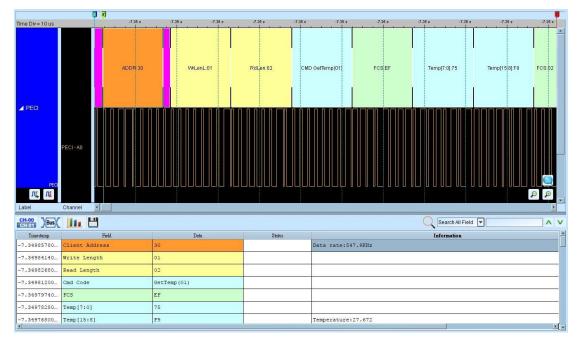


Result

Normal mode



Advance mode





PMBus

The Power Management Bus ("PMBus") is an open standard protocol that defines a means of communicating with power conversion and other devices.

Settings

PMBus S	ettings					?	×
Channel	Clock Channel (Data Channel (Decode Wit	SDA) h PEC	A0 A1 Jude R/W ir	Address)	Start Address Write		
Range	☑ Ignore glitc				Command Data PEC		
₩	From To	Buffer I Buffer		~	 ACK Stop		 ✓ ✓
					Default OK	c	ancel

Channel: Show the selected channels.

Decode With PEC: Group command protocol with PEC.

7-bit addressing (Include R/W in address): Show 8-bit addressing (include 7-bit

addressing and 1-bit R/W).

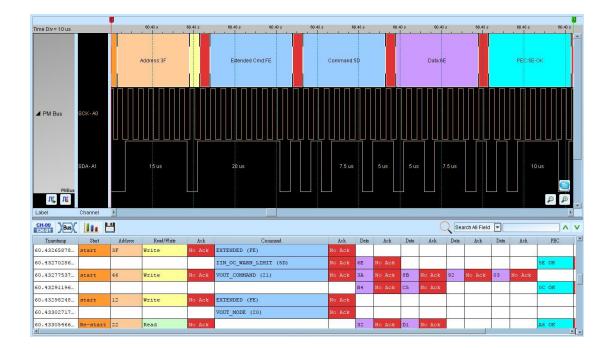
Ignore glitch: Ignore the glitch when the slow transitions.

Result

Click \mathbf{OK} to run the PMBus decode and see the result on the Waveform Window

below.







ProfiBus

ProfiBus (PROcess Field Bus) is implemented by RS485. It includes PROFIBUS DP, PROFIBUS PA and PROFIBUS FMS.

Settings

ProfiBus Settings					×
Parameters			Color		
Channel ProfiBus Chan	nel 🗛	Polarity Idle high		↓ SD	~
			SA	V DA	~
Auto Det			DSAP		
Baud Rate	9600	bps	DU	↓ SSAP	
MSB first			ED [FCS	~
Show scale i	n the waveform				
Range					
Decode Range					
From	То				
Buffer Head	∼ Buffer	Tail 🗸 🗸			
			Defau	ılt OK	Cancel

Channel: Set the ProfiBus Channel

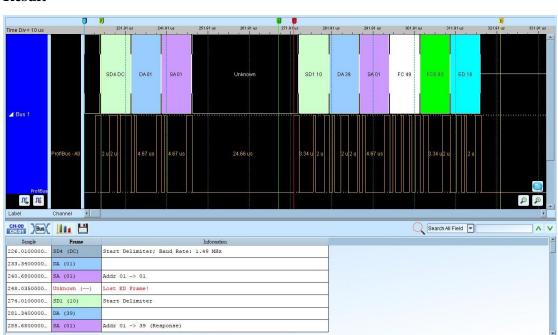
Polarity: Set the polarity Idle high / Idle low

Baud Rate/Auto Detect: Set the baud rate manually or auto detect

MSB First: The default is LSB first; click it to change to MSB first.

Show scale in the waveform: Show the scale in the waveform section





Result



PS/2

The Personal System/2 (PS/2) protocol has 6 data bits, but only the first bit (Data) and the fifth bit (Clock) need to be analyzed.

PS/2 Settings

PS/2 Setti	ngs X
Channel	
	General Analysis Report
	Clock A0 Data A1
	Convert scancode to keycode
	Export Matlab file
	Ignore glitch
Color -	
	Host V Device V
Range -	
A	Decode Range From To
	Buffer Head V Buffer Tail V
	Default OK Cancel
	Carter

Channel: Show the selected channels.

Convert scan code to key code: Transform data into keyboard characters.

Export MATLAB file: Export the data with MATLAB format as the following:

Time = [25.78484 25.785985 ...]

Description = [DH DH ...] DH = Device to Host, HD = Host to Device

Data = [58 FA 02 FA C4 ...]



The file (PS2_Matlab.m) will be saved at work directory

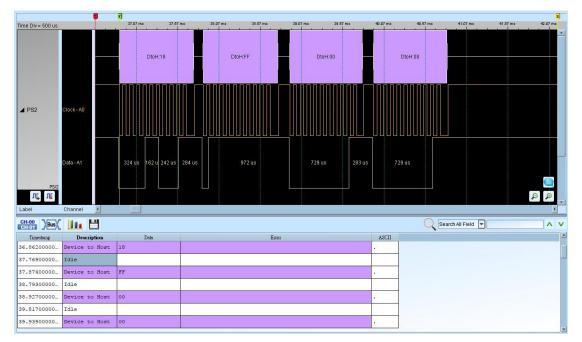
Ignore glitch: Ignore the glitch when the slow transitions.

Analysis Report: Show the selected status in report.

General	Analysis Report	
Show	the status in report	
🗹 De	scription	
🗹 Da	ta	
🗹 Err	or	
🗹 AS	CII	
Id Id	e	

Result

Click **OK** to run the PS/2 decode and see the result on the Waveform Window below.





PWM

Pulse-width modulation (PWM) is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches.

Settings

PWM Settings	×
Setting	Color
PWM Channel A0 Draw PWM curve Source Oracle Oracl	Duty Cyde 90%~100% 80%~89% 70%~79% 60%~69% 50%~59% 40%~49% 30%~39% 20%~29%
Time (X) Draw 0% and 100% Draw 0 Hz Speed Curve	10%~19% 0%~9% Range Decode Range From Buffer Head
Color Color	To Buffer Tail V Default OK Cancel

Channel: Show the selected channel.

Draw PWM curve:

Source: Show the source waveform of the PWM.

Time(X)-Duty(Y): Show the curve diagram with Time(X) and Duty(Y)

Time(X)-Freq.(Y): Show the curve diagram with Time(X) and Freq.(Y)

Time(X)-RPM(Y): Show the curve diagram with Time(X) and RPM(Y)



Draw 0% and 100%: When select the Time(X)-Duty(Y) drawing and check Draw 0% and 100%, the program will draw this duty curve of 0% or 100%; it will draw this duty curve of 0% or 100% when uncheck Draw 0% and 100%.

Draw 0 Hz: When select the Time(X)-Freq.(Y) drawing and check the item Draw 0 Hz, will show the Frequency from 0 Hz at Y axis.

Result

Click \mathbf{OK} to run the PWM decode and see the result on the Waveform Window

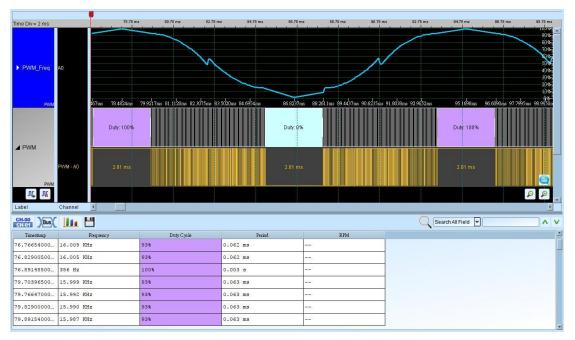
below.

FF Time Div = 5 us Duty: 63 PWM_Ch0 4.75 us 2 us 7.2 us ντ ντ Channel 🔍 Search All Field 💌 CH-00 Bus Use H A V Sample -4.75500000... Duty Cycle RPM Frequ 132.363 KHz 63% .008 ms 2.800000000... 100.000 KHz 0.010 ms 12.80000000... 100.000 KHz 0.010 ms 22.80000000... 100.000 KHz .010 ms 32.80000000... 100.000 KHz 0.010 ms 42.80000000... 100.050 KHz 0.010 ms 52.79500000... 99.950 KHz 0.010 ms

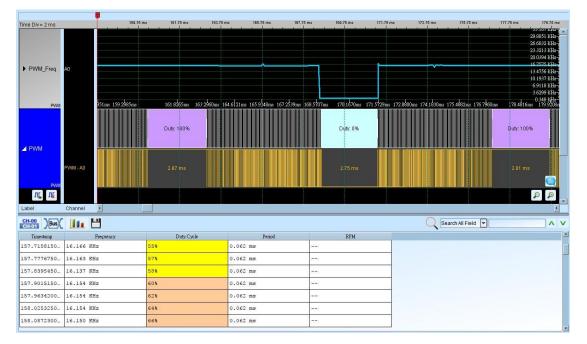
Select "Source"



Select Time(X)-Duty(Y)

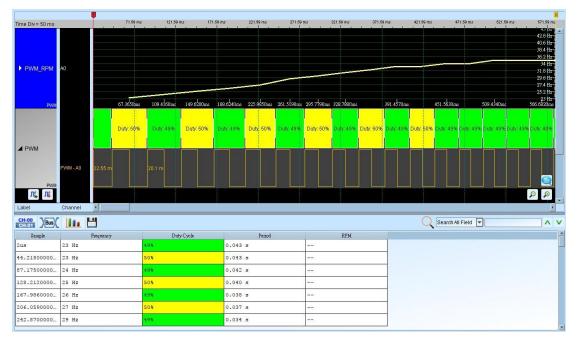


Select Time(X)-Freq.(Y)





Select Time(X)-RPM(Y)





QI

QI is a contactless power transfer protocol published by Wireless Power Consortium (WPC). It is a method of contactless power transfer from a Base Station to a Mobile Device, which is based on near field magnetic induction between coils.

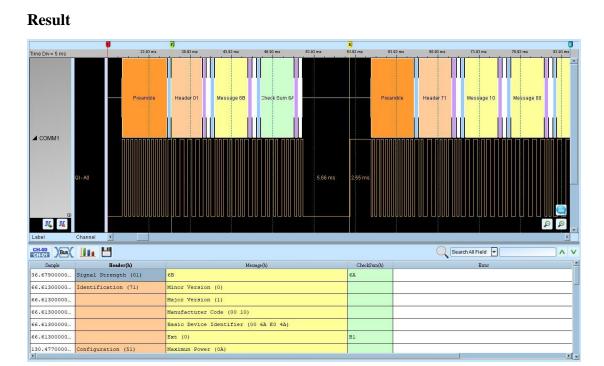
Settings

QI Param	eter Settings X
Paramet	er Setting
, P	QI Channel A0 Advanced Decode
Color —	
	Preamble Start
	Head V Parity V
	Message Stop V
	CheckSum 🗸
Range -	
L.L	Decode Range
* *	From To
	Buffer Head \sim Buffer Head \sim
	Default OK Cancel

QI Channel: Show the selected channel.

Advance Decode: show detail message decode





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RC-5

The RC-5 code from Philips is possibly the most used protocol by hobbyists, probably because of the wide availability of cheap remote controls. The protocol is well defined for different device types ensuring compatibility with your whole entertainment system.

Settings

RC-5 Set	tings			?	×	
Channel	RC-5 Channel A0 □ Extended m ☑ Display with	•	Encoding Method Auto Detect Mancherster Mancherster 1 1	• •	_	
Color	S1 S2 Toggle 0 Toggle 1 Address Command		Range Decode Range From To Buffer Head V Buffer Tail Default OK Cancel	~		

Channel: Show the selected channel (CH 0).

Extended mode: When the Extended enabled, the S2 will be converted into seventh

bit of the Command. There is an Extend Command on the Waveform Window.

Display without idle in report: It will not idle on the Report Window for the user to observe and analyze data.

Encoding Method: Auto Detect mode, Mancherster mode and Mancherster with carrier mode.

S1/S2: Start bit.

Toggle 0/Toggle 1: The difference is that has been used while sending the message to



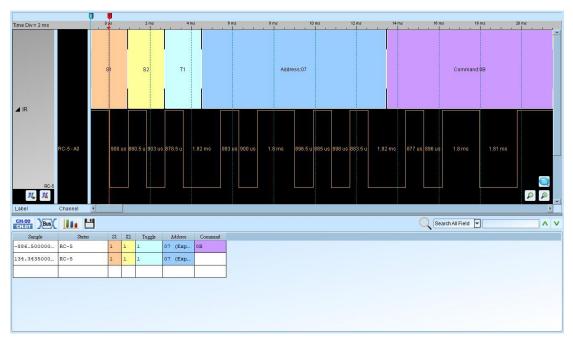
repeat, or send a new message.

Address: To represent different device addresses.

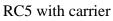
Command: To represent the different button commands.

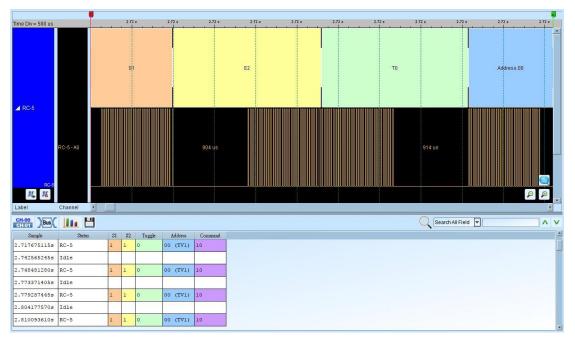
Result

Click **OK** to run the RC-5 decode and see the result on the Waveform Window below.



RC5 without carrier







RC-6

RC-6, like RC-5, is also developed by Philips. But, RC-6 has more features of remote controls than RC-5.

Settings

RC-6 Set	tings		?	×	
Channel	RC-6 Channel A0 Addr&Cmd Bits 8 Bits Display without idle in report	Encoding Method Auto Detect Mancherster Mancherster with carrier			
Color	Leader Start Bit Mode Bits Toggle Bit Control Information V	Range Decode Range From To Buffer Head V Buffer Tail Default OK Cancel	~		

Channel: Show the selected channel (CH 0).

Add & Cmd Bits: Show commands in 8 bits or 16 bits of address and information in the control label.

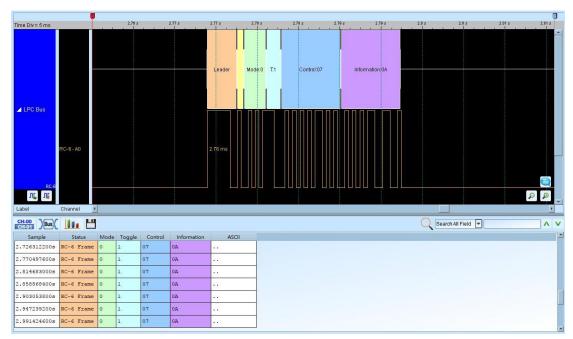
Display without idle in report: Do not display any idle in the Report Window.

Encoding Method: Auto detect mode, Mancherster mode, Mancherster with carrier mode.



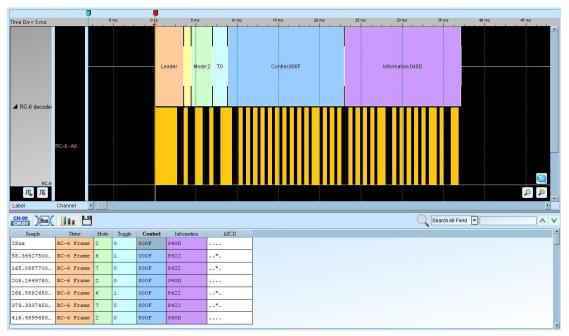
Result

Click **OK** to run the RC-6 decode and see the result on the Waveform Window below.



RC6 without carrier

RC6 with carrier





RGB Interface

RGB Interface is for data transmission between MCU and LCD. LCD Panel can be driven by LCD controller. RGB data would be written in memory and can be transmitted to LCD controller. It is able to show the picture of LCD Panel by reading the data from the interface.

Settings

RGB_IF Settings			×
Channel			
SCLK A0 DE A1 HSYNC A2 VSYNC A3 VSYNC SYNC A3 VSYNC A3 VSYNC SYNC A3 VSYNC SYNC SYNC SYNC SYNC SYNC SYNC SYNC	R0 A4 R1 A5 R2 A6 R3 A7 R4 A8 R5 A9 R6 A10 R7 A11	G0 A12 ● B0 G1 A13 ● B1 G2 A14 ● B2 G3 A15 ● B3 G4 A16 ● B4 G5 A17 ● B5 G6 A18 ● B6 G7 A19 ● B7	A21 A22 A23 A24 A25 A26 A27
Format RGB888 V A (Alpha) R (Red) 0 bits V 8 bits		(Blue) L (Luminar 8 bits V 0 bits	nce)
Color HSYNC		DATA	~
Range Decoded Range From Buffer Head	√ To	Buffer Tail	~
	Defa	ult OK	Cancel



SCLK: The Clock pin.

DE: The Data Enable pin.

Hsync: The Horizontal synchronization pin.

Vsync: The Vertical synchronization pin.

R0 – 7, G0 – 7, B0 – 7: RGB data pins.

Format: Select one of RGB formats or User defined.

Save as JPG file: Generate the JPG file with RGB data in the work directory of LA.

ime Div = 100 ns		73.57 ms	73.67 ms	73.67 ms	73.57 n	ns 73.6	i7 m s 7:	3.67 ms	73.67 ms	73.67 ms	73.67 ms	73.57 ms	73.57 m
		R: 0C. G: 0F. B: 2A.	R: OD. G	0E. B: 2B.	R: 0A. G:	16. B: 28.	R: 0B. G: 0F	. B : 27.	R 08. G: 0F. B:	27.	R: 0B. G. 1A. B. 2B.	R: 12. G: 1	2. B: 3B.
	SCLK - A24	85 ns	85 ns	80 ns	85 ns	85 ns	80 ns	85 ns	85 ns	BO ns	85 ns 85 ns	80 ns	
	HSYNC - A12												
	R0 - A14		10	5 ns	170) ns		-	500 ns			_	
	R2-A3												
	R3 - A4 R4 - A6												
Bus 1	R5-A23 G0-A2			33	5 ns			330 n	s				
	G1 - A25 G2 - A9						1			-			
	G3 - A10 G4 - A13)ns)ns		330 n	495 ns s				
	G5-A15		18	5 ns	1 17()ns							
	B1 - A26 B2 - A27				1			330 n	\$				
	83 - A0 84 - A7							<u>330 n</u>					
RGB_IF													-9
W IN													e e
Label	Channel 💽												1
CH-00 Bus										Q	Search All Field 💌		^
Timestamp	Field	D0 (RGB)	D1 (RGB)	D2 (RGB)	D3 (RGB)	D4 (RGB)	D5 (RGB)	D6 (RGB)	D7 (RGB)				
3.57077000	Ln36, D[16:23	DC OF 2A	OD OE 2B	0A 16 28	OB OF 27	0B 0F 27	0B 1A 2B	12 12 3B	13 13 3C				
3.57210000	Ln36, D[24:31	.] 13 13 3C	OF OF 32	07 08 1B	13 13 3C	13 13 3C	08 09 1E	0A 09 24	07 08 1A				
3.57343500	Ln36, D[32:39] 11 11 37	13 11 36	07 08 1B	0B 0B 25	07 08 1C	13 13 3C	13 13 3C	13 1A 3D				
3.57477000	Ln36, D[40:47	D OD OE 2E	06 08 19	02 01 38	OB OC 26	08 09 1D	02 01 3C	08 09 1C	0B 0C 27				
3.57 <mark>6</mark> 10000	Ln36, D[48:55) 05 07 18	09 0A 20	09 0A 20	05 07 18	OD OE 2D	05 07 18	13 13 3C	11 13 3D				
THE REAL PROPERTY AND ADDRESS OF	Ln36, D[56:63	06 08 1A	13 13 3C	13 1A 3C	13 13 3C	05 07 18	09 0A 20	09 0A 20	07 08 1B				
73.57743500	Linot, D[00.00	, 00 00 m		and the second second									

Result



S/PDIF

The Sony/Philips Digital Interconnect Format (S/PDIF) is a digital audio transmission

interface with the detailed specifications below:

Data format: Default is 16 bits, up to 24 bits.

Sampling frequency:

44.1Khz from CD \rightarrow Bit Rate 2.8224 Mbit/s

48 Khz from DAT →Bit Rate 3.072 Mbit/s

32 Khz from DSR \rightarrow Bit Rate 2.048 Mbit/s

Deliver method: One way.

V (Validity) bit: Audio samples to confirm effectiveness, if this bit is 0, the receiver

should ignore this sub-frame.

U (User) bit: User log information.

C (Channel status) bit: Channel state information.

P (**Parity**) **bit:** Parity bit check for the error.

The basic principle is to split the data bits into two parts. If the data is 1, split it into

01 or 10 or if the data is 0, split it into 00 or 11.

Settings



<u></u>	Block		Data Bits
Channel A0	192 (3	2 ~192) frames	
Auto detect Bit Rate			16 ~
→ Mb/s	Bit Order		Parity mode
	Aux.	LSB first 🗸 🗸	Even parity $~~$
(384Kb/s~12.288Mb/s)	Audio Data	LSB first \sim	Playback
🗹 Display the audio waveform			
Color Preamble		ser bit	
Preamble Aux Data Audio Data Validity bit	a	ser bit nannel Status bit arity Bit	
Preamble Aux Data Audio Data Validity bit Range		hannel Status bit	
Preamble Aux Data Audio Data Validity bit Range Decode Range		hannel Status bit	
Preamble Aux Data Audio Data Validity bit Range Decode Range		hannel Status bit	

Channel: The default is Channel 0.

Auto detect Bit Rate: Turned on by default.

Num of frame: 192 frames within each block by default, used to analyze each

sub-frame order User bit and Channel status bit.

Bit Order (Aux. Data): The default is the LSB first for the Aux. data.

Bit Order (Audio Data): The default is the LSB first for Audio data.

Data format: The default is 16 bits.

Parity mode: The default is even parity.

Display the audio waveform: Click to display the audio waveform in the Waveform

Window.

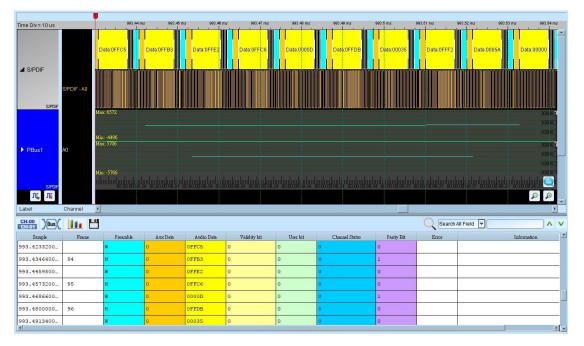
Result

Click **OK** to run the S/PDIF Decode and see the result on the Waveform Window





Show wave:





SDIO

The SD3.0/SDIO3.0 Protocol is a high speed serial protocol used primarily for interfacing with SD (Secure Digital) Flash memory cards.

Settings

SDIO/SD	3.0 Settings		×
Channel	Channel DATA1 A3 ✓ CLK A0 ✓ DATA1 A3 ✓ CMD A1 ✓ DATA2 A4 ✓ DATA0 A2 ✓ DATA3 A5 ✓	Analysis Command only Data only Command + Data SPI mode Command	olor Start bit Host Device CMD/Resp
	Data length: Bytes (Min: 1, Max: 2048)	Adv. Report	ArgumentImage: CRC checkEnd bitImage: CRC statusDataImage: CRC statusBusyImage: CRC status
Range	Decode Range From To Buffer Head V Buffer Tail	~	Default OK Cancel

Channel: Show the selected channels.

Command only: Analyze the command.

Data only: Analyze the data.

Command + Data: Analyze Command and Data in the report window.

Adv. Report: Analyze the command argument

Don't care clock: decode only depend on the CMD channel.

Data: 1/4/8 bits or DDR mode, check "IO interrupt" when SDIO 1 bit mode and

support the IO interrupt decode via DATA1 channel, check "DDR mode" and "

"Non-interleaved" to analyze data without interleaved.



Data length: Set the length of data.

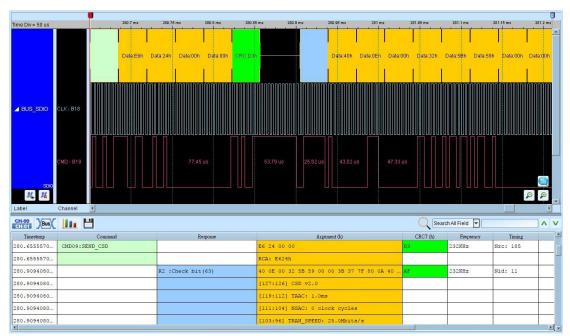
Result

Click OK to run the SDI/O decode and see the result on the Waveform Window

below.

CMD mode





Adv. Report

Data mode



Ime Div = 20 ns		448.67	ms	448.67 m		448.67 ms	4	48.67 ms	448.6	37 ms	448.67 ms	448.6	7 ms	448.6	7 ms	448.0	67 ms	448.6	7 ms	448.67
	сцк- в18	81h	l oon	l ooh		82H	oon o		Jh 83h		00h	00h 84h	ooh	00h	OOh	85h	00h	oon	ooh	86h 0
	CMD - B19																			
BUS_SDIO	Data0 - B16	7 ns 6.5 n				1.5 ns			6.5 n			71.5 ns				6 ns				
	Data1 - B17		47	ns		6.5 n	38	3 ns	6 ns					111 ns						6 ns
	Data2 - B21						124.5 ns					6.5 n		32.5 ns		6 ns		33 ns		6 ns
SDIO	Data3 - B20	7 ns			6.5 (6.5 n	32.51		6 ns			6	ns			6.5 n	
NLabel	Channel •																			
CH-00 V-V	III 💾													(arch All F	ield 💌			^
CH-01 BUS					D3(h)	Dida	D5(h)	D6(h)	D7(h)			Information				ASC	31			
Sample	Data	D0(h)	D1(h)	D2(h)	DS(n)	D4(h)	05(1)	DO(II)				monnation								
Sample	Data	D0(h)	D1(h)	D2(h)	D3(h)	U4(h)	05(1)	D0(II)	1	CRC16 OK		mornation								
Sample 148.6667415	Data	D0(h)	D1(h)	D2(h)	00	82		00	1	CRC16 OK		momadon			- 			-		
Sample 148.6667415 148.6668975										CRC16 OK		monnation						-		
Sample 148.6667415 148.6668975 148.6669755	D[27600:27607]	81	00	00	00	82	00	00	00	CRC16 OK		mombion						-		
Sample 148.6667415 148.6668975 148.6669755 148.6670535	D[27600:27607] D[27608:27615]	81 83	00 00	00	00	82 84	00	00 00	00 00	CRC16 OK										
	D[27600:27607] D[27608:27615] D[27616:27623]	81 83 85	00 00 00	00 00 00	00	82 84 86	00	00 00 00	00 00 00	CRC16 OK					•••					



Serial Flash

SPI Serial Flash is small, low-power flash memory that features Serial Peripheral Interface (SPI) and pin-for-pin compatibility with industry-standard SPI EEPROM devices.

Settings

5								
1	CS#	A0		SCLK	A1	-	Manufacturer EON	
	SI/SIO0	A2	•	SO/SIO1	A3	•	Device	~
	WP#/SIO2	A4	* *	Hold#/SIO3	A5	-	EN25(L)F10 EN25(L)F20	^
	SIO4	A6		SIO5	A7	*	EN25(L)F40 EN25864	
	5106	A8	•	5107	A9	- -	EN25B64T EN25F05	
	DQS	A10						
Dun Wra QE	rtup in PEM m nmy Cycles ap Around bit set rtup in Octal n STR ① DTF	2 Clk 8 B	-	When Comma Decode S Reduced Re	SI OD			
nge	Decode Rang Begin			End				
	Buffer Head		1	Buffer Tail		\sim		

Channel: Show the selected channels (CH0 – CH5).

Manufacturer/Device: Select the Serial Flash device type, tCLQV and tSHSL.



QPI mode: Quad Peripheral Interface Mode/Quad SPI Mode

4-Byte mode: 4-Byte Address Mode

PEM mode: Performance Enhance Mode

Dummy Cycles: Clock buffers between read command and data.

Wrap Around: Wrap number

QE bit: Enable or disable the QPI mode.

Decode SI Only: Single mode, 3-wire \rightarrow CS#, SCLK, SI.

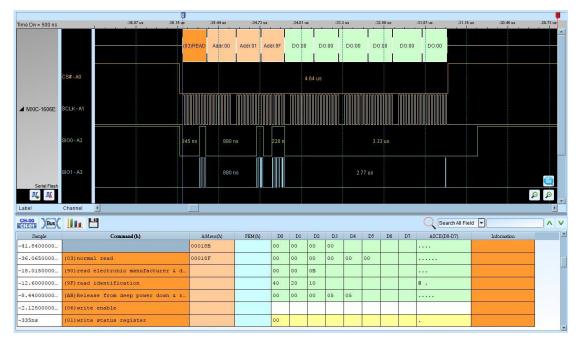
Decode Single Mode Only: Single mode, 4-wire \rightarrow CS, Clock, SI, SO.

The LA viewer will choose 4-wire or 6-wire to analyze according to the Serial Flash device type.

Result

Click **OK** to run the Serial Flash decode and see the result on the Waveform Window

below.



Serial Flash decode within SPI mode.

Serial Flash decode within QPI mode.



me Div = 10 us		33.08 ms	33.00 ms	33.1 ms	33.11 ms		33.12 ms		33.13 m	s	33.14	ms	33	1.15 ms 33.16 ms	33.17 ms	33.18
		(6B)FRQO Addr:0	0 Addr.00	Addr:00 D	MY:00				(6B)F	RQO	Addr:0	00	Addr:00) Addr.20 DI	WY:00	
	CS#-A19															
	SCLK-A18							2 u								
Winbond-SFI:	SIO0 - A20	2 u 2 u	33	01 us	4		2 4 3		IS 2 U	2 U				13.01 u	s 4 us 4 us	24
	SIO1 - A21						2 u						5.51 us			3 us
	SIO2 - A22						2 u						40.51 us		3 us 2 u 2 u	
Serial Flash	SIO3 - A23					16.57	'us							55.51 us		
VÊ VÎ																e e
abel H-00 Bus(Channel	<u> </u>												Q Search All Field		
Timestamp		Command (h)		Address(h)	PEM(h)	DO	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Information	
3.067080000m	s (6B)Qua	d Output Fast Read	d	000000		41	43	55	54	45	20	53	50	ACUTE SP		
		d Output Fast Read	a	000020		51	75	61	64	20	50	72	6F	Quad Pro		
3.124580000m	s (6B)Qua	a output rabt neu	.			-	1.00	55	54	45	20	53	50	ACUTE SP		
		d Input / Output		000000	00(reset)	41	43	00	12.25							
3.182080000m	s (EB) Qua		FAST_READ	000000	00(reset) 00(reset)	41 51	43 75	61	64	20	50	72	6F	Quad Pro		
3.182080000m; 3.219580000m;	s (EB) Qua	d Input / Output	FAST_READ			1000	Sector Sector	61	10000	20	50	72	6F	Quad Pro ACUT		
33.124580000m 33.182080000m 33.219580000m 33.257080000m 33.256580000m	s (EB) Quan s (EB) Quan s (EB) Quan	d Input / Output) d Input / Output)	FAST_READ	000020	00(reset)	51	75	61	64	20	50	72	6F	100000000000000000000000000000000000000		

Serial Flash data Comparison : Compare the Serial Flash data by the waveform files.

Method: Create a file by text editor and save it as SFCmp.cfg in order to compare

with the real Serial Flash waveform to find the bug, the default path is "My

Documents\Acute"

Acute	J×
G Documents VAcute Search	2
🔄 Organize 🔻 就 Views 👻	0
Name 🔺 🕶 Date modified 💌 Type 💌 Size 💌 Tags 💌	
SFCmp.cfg	
1 item	

SFCmp.cfg information:



III SFCmp.cfg - Notepad									
File Edit Format View Help									
<pre>;; comment OrgFile=C:\Documents and Settings\Liu\My Documents\Acute\SF.bin OutFile=C:\Documents and Settings\Liu\My Documents\Acute\SD_cmp.bin OutLstFile=C:\Documents and Settings\Liu\My Documents\Acute\SF.lst CheckCmd=03, EB</pre>	<pre>;;Original file ;;LA output serial flash file ;;Compare result ;;The HEX command need to check.</pre>								

OrgFile=File_Path: Key in the file path of the original Serial Flash data file (.bin).

OutFile=File_Path: Key in the file path of the Serial Flash output file.

OutLstFile=File_Path: Key in the file path of the comparison result. The file name

will has extension ".lst".

CheckCmd=Serial Flash command: Key in the command in Hex that are separated

by commas.

Save the OrgFile to the OrgFile file path.

Acute	
G Documents Acute	
Organize 🔻 ங Views 👻	•
Name 🔺 🔻 Date modified 💌 Type 💌 Size 💌 Tags 💌	
SF.bin SFCmp.cfg	
2 items	

Run the Serial Flash Bus Decode to capture the Serial Flash signal.



R Acute	e TravelLogic										14	- (×
File	Capture Adv. C	anture C	ursor											
Conne	 Bus	Trigger Free Run	Sample Rate 200MHz (5ns)	Memory 2000 Mb - 32CH	A⊻ Threshold	Run R	b tepeat	Zoo		~~	Demo Phase De 0 ns			
Time/Div	= 2 us	N 🖸	916.6 us	918.6 us	920.6 us	922.6 us	924.6 us	*	926.6 us		28.6 us		930.6 us	
	C-1606E 3:0		3 Add Ad(Ad(DO: D			94.0 US 1			T	c Ad+ DO: E		ŤŤ		
CH-00 CH-01	Bus L						C	Searc	All Field	•			~	v
	Sample		Command(h)	Addres	s(h) PFI	M(h) D0	D1	D2 [D3 D4	D5	D6	D7	1-
478	915.175us	(03) normal			000078	-0.9	21	L BERNART I	0 48	Name and Address of States	OF	00	01	
479	925.92us	(03) normal	l read		000ADA		00	00 0	0 03	00	00	00	09	
480	931.425us				000AE2		C1		8 20					
481	937.52us	(03) normal	l read		000AE6		01		1 02		01	09	02	
482	943.02us	(00)			000AEE		79		1 01			~~		
483 484	949.115us 954.62us	(03)normal	1 read		000AF2 000AFA		00		D 00 6 50		04	00	00	
								_						- 1
Connected	SN:TLP32340002 (U	ISB 3.0)		Analys	is Finished!!			8 1.22	OMHZ <mark>B</mark> 9	2.980KHz	o 95.785	KHz 🕻	N (m
\ M Logic	: Analyzer-AqSFlash_M	XIC_TL2 X	< / 🗐 🛄											

If the OutFile does not exit, it will copy the OrgFile to the OutFile and write the data to it according to the CheckCmd.

Compare result:

Acute	<u> </u>
G Documents Acute	2
🕘 Organize 👻 📷 Views 💌	(?)
Name 🔺 🗣 Date modified 🔽 Type 🗣 Size 🗣 Tags 🗣	
SF.bin SF.Jst SF_cmp.bin SFCmp.cfg	
4 items	

The OutLstFile:



J SF.Ist - Notepad	
File Edit Format View Help	
OrgFile=C:\Documents and Settings\Liu\My Documents\Acute\2Mbit_o OutFile=C:\Documents and Settings\Liu\My Documents\Acute\2Mbit_o	
00001321 00001399: E2 E0 00001321 000013A1: 52 50	
0000143C 00001461: 73 71 0000143C 0000148F: D3 D1	
0000143C 00001499: C3 C1 0000143C 000014BB: E3 E1 000014D5 000014DB: F3 F1	
0000159C 000015C8: F3 F1 0000159C 000015E2: 32 30	
0000159C 000015E6: 42 40	_
T	V N

The first column is the compared address from OrgFile, the second column is the

different address from OutFile.



Serial IRQ

The IRQ/Data serializer is a Wired-OR structure that simply passes the state of one or more device's IRQ(s) and/or Data to the host controller. The transfer can be initiated by either a device or the host controller. A transfer, called an IRQSER Cycle, consists of three frame types: one Start Frame, several IRQ/Data Frames, and one Stop Frame. This protocol uses the PCI Clock as its clock source and conforms to the PCI bus electrical specification.

Settings

Serialized	IRQ Setting	×
Channel		
1	CLOCK A0 • IRQSER A1 •	
1.000000	Report format	
	Normal OAdvance	
	Show Repeat Frame	
Color —		
	Start Frame	
	Stop Frame	
	Assert Frame	
	Dessert Frame	
Range		
	Decode Range	
The second	From To	
	Buffer Head 🛛 🗸 Buffer Tail 🗸	
	Default Ok Cancel	-
	Default OK Cancel	

CLOCK: PCI Clock channel

IRQSER; IRQSER channel

Normal: Not show repeat frame



Clock	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IRQ
10286946	22830	Continue mode		Α					Α						Α				
10291906	22841	Continue mode		Α											Α				
10404663	23091	Continue mode		Α					Α						Α				
10415039	23114	Continue mode		Α											Α				
10459240	23212	Continue mode		Α					Α						Α				
10461943	23218	Continue mode		Α											Α				
10580112	23480	Continue mode		Α					Α						Α				
10590037	23502	Continue mode		Α											Α				
10634238	23600	Continue mode		Α					Α						Α				
10636941	23606	Continue mode		Α											Α				

Show repeat frame

Clock	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IRQ
10457887	23209	Continue mode		А											А				
10458338	23210	Continue mode		Α											Α				
10458789	23211	Continue mode		Α											Α				
10459240	23212	Continue mode		Α					Α						Α				
10459690	23213	Continue mode		Α					Α						Α				
10460140	23214	Continue mode		Α					Α						Α				
10460590	23215	Continue mode		Α					Α						Α				
10461041	23216	Continue mode		Α					Α						Α				
10461492	23217	Continue mode		Α					Α						Α				
10461943	23218	Continue mode		Α											Α				
10462394	23219	Continue mode		Α											Α				
10462846	23220	Continue mode		Α											Α				
10463298	23221	Continue mode		Α											Α				

Advance:

Clock	IRQ/Data Frame	Signal Sampled	# of clocks past Start
-9470	1	IRQO	2
-9452	2	IRQ1	5
-9434	3	SMI#	8
-9416	4	IRQ3	11
-9398	5	IRQ4	14
-9380	6	IRQ5	17
-9362	7	IRQ6	20
-9344	8	IRQ7	23
-9326	9	IRQ8	26
-9308	10	IRQ9	29
-9290	11	IRQ10	32
-9272	12	IRQ11	35
-9254	13	IRQ12	38
-9236	14	IRQ13	41
-9217	15	IRQ14	44
-9199	16	IRQ15	47
-9181	17	IOCHCK#	50
-9163	18	INTA#	53
-9145	19	INTB#	56
-9127	20	INTC#	59
-9109	21	INTD#	62
-9019	1	IRQO	2
-9001	2	IRQ1	5

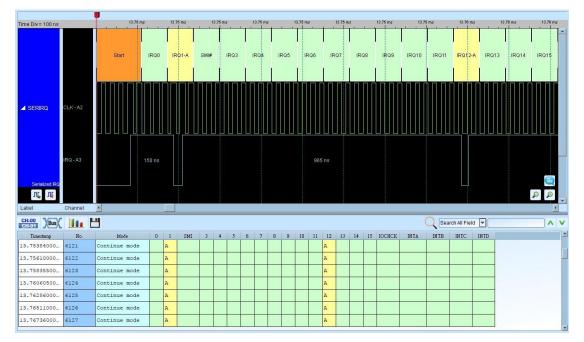
Result

Normal mode



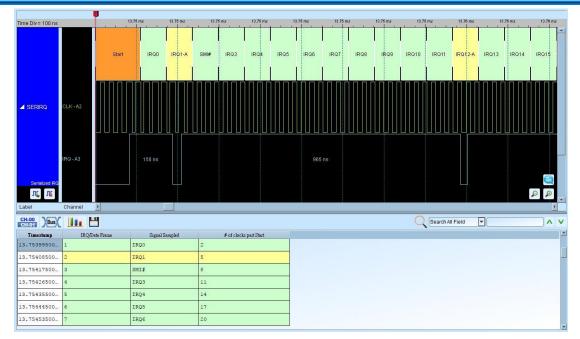
fime Div = 200 ns		13.76 ms		13.76	5 ms	13.7	5 ms	13.	76 ms	1	3.76 ms		13.76 ms		13.76 ms	13	.76 ms	13.78	ms	13.3	76 ms	13.76 r
		Start IRG	10 IRC	01-A SI	M⊯ IRI	23 IRG	4 IRG	15 IRQI	5 IRQ7	IRQS	3 IRQ9	IRQ10	IRQ11		IRQ13	IRQ14 IRG	215	INTA#	INTB#	INTC#	INTD≠	Stop
✓ SERIRQ	CLK-A2																					
	IRQ - A3	120 ns 150 r	15						35 ns								78	5 ns				90 ns
Serialized IRQ																						
	Channel																					<mark>ال</mark> م
ντΩ γι																		arch All Fi	eld 💌			
л ц Лц Label	in the second second		0		SMI	3	4 5	6	7 8	9	10 1	. 12	13 1	4 1.	5 IOCHCI	K INTA		arch All Fi				
Л, Л, Label CH-00 CHOT)Bus Timestamp		9	0		SMI	3	4 5	6	7 8	9	10 1	. 12 A	13 1	4 11	5 IOCHCI	K INTA	~					
Label	No.		0		SMI	3	4 5	6 A	7 8	9	10 1	Est 1	13 1	4 11	5 IOCHC	K INTA	~					
Interstamp	No.	Mode Continue mode	0	A	SMI	3	4 5		7 8	9	10 1	A	13 1	14 11	5 IOCHCI	K INTA	~					
Л. Л. Label CH.00 CH.01) Вих Timestamp 13.75384000 14.37173000	No. 6121 6395	Made Continue mode Continue mode	0	A A	SMI	3	4 5		7 8	9	10 1	A A	13 1	14 11	5 IOCHCI	K INTA	~					
AL AL Label CH-00 Yess Timestump 13.75384000 14.37173000 14.40782000 14.40782000 14.63334000	No. 6121 6395 6411	Mode Continue mode Continue mode Continue mode	0	A A A	SMI	3	4 5	A	7 8	9	10 1	A A A		4 1.	5 IOCHCI	K INTA	~					
M. M. Label CH-00 Timestamp 13.75384000 14.37173000 14.40782000	No. 6121 6395 6411 6511	Mode Continue mode Continue mode Continue mode Continue mode	0	A A A A	SMI	3	4 5	A	7 8	9		A A A A	13 1		5 IOCHCI	K INTA	~					

Normal mode(Show repeat frame)



Advance mode







Serial General Purpose Input Output (SGPIO)

The SGPIO is a method to serialize general purpose IO signals. SGPIO defines the communication between an initiator and a target.

Settings

SGPIO Sett	ings				e de la companya	×
Channel	Channel Clock Load DO	A0 A1 A2 A3	> > >	Color	Load Data Data Decode Range From To Buffer Head Buffer Tail	
					Default OK Cancel	

Channel: Show the selected channels (Clock, Load and Data), it can only use data out or date in or both.

Result:

Click OK to run the Smart Card decode and see the result on the Waveform Window below.



ime Div = 2 us				1.04 ms	-1.04 ms	-1.04 r	ns -1.1	04 ms - 1	.04 ms -1	.03 ms -1	.03 ms	-1.03 ms	-1.	03 ms	-1.03 ms	-1.02 m
	Cik - A0	DI: 7	DI: 0	JINKNOWE	DI: 3	DI: 6	DI: 1	DI: 2 I	DI: 3 DI: 7	DI: 0	Jinknowr	DI: 3	DI: 6	DI: 1	DI 2	DI: 3
PBus1	Load - A1							9.04 us] [] [] []
	D0 - A2	1	.55 us	95	5 ns 1 06 u	s 1.51 us	1.52 us	985 ns	1.48 us	1.55 us	960 ns	1.06 us	1.52 us	1.52 us		990 ns
											<u> </u>			<u> </u>	┛━┡┯	
SGPIO	DI-A3 Channel		7	5 n 1.56 us	1.7	us	3.21 us		3.7 us	735 n	1.56 us	1.77 us		3.21 us		
ALE I	Channel		7	5 n 1.56 us	1.7	us	3.21 us		3.7 us	735 n	1.56 us	1.77 us	Search All I			
A N	Channel	-	LOAD	5 n 1.56 us Activity(OD		us		Dn.2) A	3.7 us	Coste ([Dn.1])		1.77 us				Q
ALL	Channel	-			n0)			12/2000	ctivity(IDn0)			Q				Q
J J abel H-00 H-01 Bus Timestamp 1.04615000	Channel	-	LOAD	Activity(OD	n0) 7	Locate(ODn.1)	Feil(C	No A	ctivity(IDn0)	Locate([Dn.1)	Fail	Q				Q Q
M. M. abel Bus Timestamp 1.04465000	Channel Channel Device Device 5 Device 6		LOAD	Activity(OD Activit;	n0) 47	Locate(ODn.1) Locate	Fail	No A	ctivity(DnO) ctivity 1 ctivity	Looste([Dn.1) No locate	Feil	Q				Q Q
NL NL abel	Channel Channel Device Device 5 Device 6 Device 0		LOAD	Activity(OD Activit; To Activit;	n0) 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	Locate(ODn.1) Locate locate	Fail	No Au No Au Au	otivity(Da0) ctivity 2 ctivity 1	Locate([Dn.1) No locate Locate	Feil OK OK	Q				Q
Image: Control of the second	Channel Channel Device 5 Device 6 Device 0 Device 1		LOAD	Activity(OD Activit: Activit: Activit:	n.0)	Locate(ODn.1) Locate locate Locate	Pail(C Fail OK OK	No Au No Au Au No Au	otivity(DaO) ctivity 2 ctivity 2 ctivity 2	Locate(Dn.1) No locate Locate No locate	Feil OK OK OK	Q				Q
abel	Channel Channel Device Device 5 Device 6 Device 0 Device 1 Device 2		LOAD	Activity(OD Activit; No Activit; Activit; No Activit;	n 0)	Locate(ODn.1) Locate locate Locate	Fail Fail OK OK Fail	No A No A A No A	otivity(Dn0) Stivity 2 Stivity 1 Stivity 2 Stivity 2	Looobe(IDn.1) No locate Locate No locate No locate	Feil OK OK OK Fail	Q				Q



Smart Card (ISO7816)

The card is made of plastic and provides strong security authentication for single sign-on within large organizations.

Settings

Smart Card	d (ISO781	16) Settir	ngs					×
Channel					Color			
Range	CLK DATA ETU Decode	A0 A1 372		lock (16~2048)		Start Data Parity Stop		> > > >
	From	Head	~	To Buffer Tail	∽ Defau	ılt	ОК	Cancel

Channel: Show the selected channels (CLK and DATA) and the number of clocks within the bit (ETU).

Result

Click **OK** to run the Smart Card decode and see the result on the Waveform Window below.



		Start	16 ms 6.16 ms	6.36 ms	0.58 ms	STOP Start	7.36 ms 7.86 ms	7.78 ms 7.98 ms
Smart Card	CLK-A5							
Smart Card	DATA-A1	92.38 u		92.37 u	369.5 us	185.25 us	75 us	185.24 us
	Channel	4						
abel.	Channer							
		1					Q Search All Field	·
Timestamp	Data	Parity	ETU Tolerance				Search All Field	×^
Timestamp	Data	•	ETU Tolerance				Search All Field	
H-00 Bus Timestamp .754510000	Data	Parity		_			Q Search All Field	×
H-00 Bus Bus Timestamp	Data	Parity 0 (OK)	0	_			Search All Field	× ^
CH-00 Bus Timestamp 754510000 	Dota 11 00	Parity 0 (OK) 0 (OK)	0 0				Search All Field	×



System Management Bus (SMBus)

The SMBus (SMB) is a two-wire bus.

Settings

SMBus Settings			×
Parameter		Color	
Channel SMBCLK A0 • SMBDATA A1 •	Decode PEC DDR4 DDR3 DDR2 DDR SPD SDRAM	Command Address Write / Read Start / Stop / Sr ACK / NACK	
Address	ndude R/W in Address)	PEC / Word / Byte Count Data / Content	
Report SMBus Show SBS(Smart E Show SPD(Serial F SPD Filter		Word Address	· · ·
☑ Ignore glitch Range Decode Range			
From To Buffer Head V	ıffer Tail 🛛 🗸 🗸		
		Default	Ok Cancel

Clock: Show the selected channels (SMBCLK CH0 and SMBDATA CH1).

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit

addressing and 1-bit R/W).

Show SBS (Smart Battery System): Show the Smart Battery System: voltage,

electric current and the manufacturer.

Show SPD(Serial Presence Detect) : Report window show the configuration of

memory module(DDR3, DDR2, DDR, SPD SDRAM) in EEPROM.

SBS/SPD Filter: Report window only show SBS/SPD packet.



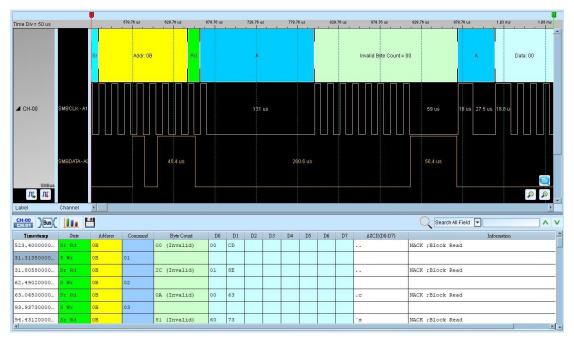
Ignore glitch: Ignore the glitch when the slow transitions.

Result

Click **OK** to run the SMBus Decode and see the result on the Waveform Window

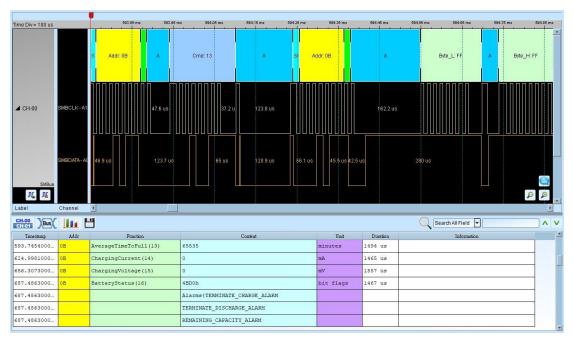
below.

SMBus

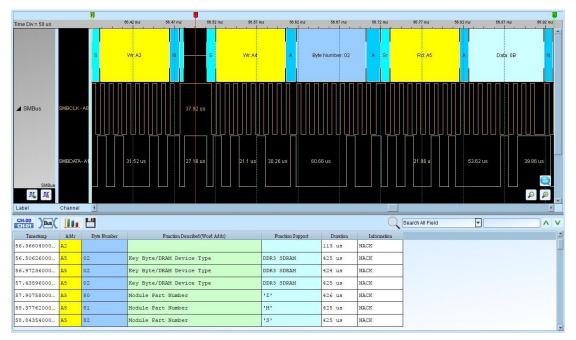




Show SBS (Smart Battery System)



Show SPD (Serial Presence Detect)





Serial Microprocessor Interface (SMI)

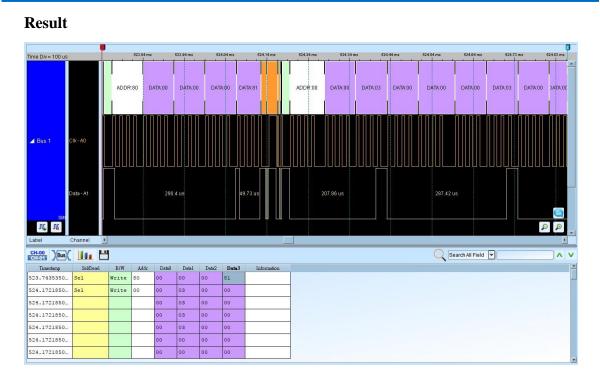
The SMI is a two-wire bus.

Settings

SMI Settings		×
Channel —		
: Clk	Data	
A0	✓ A1 ✓	
Color		
Attn	~ ~	
Sel/Desel		
R/W		
Address		
Data		
Attn desel		
Range —		
Decode Ra	ange	
From	То	
Buffer H	lead 🗸 Buffer Tail	~
		- I
	Default OK	Cancel

Channel: Show the selected channels (Clk and Data)







Serial Peripheral Interface (SPI)

The SPI, is one kind of 4-wires synchronous serial data link. The SPI bus can be 4

wires, 3 wires, or 2 wires.

Settings

Type: The default is 3 Wire-SPI.

SPI Settings	×
Setting	3 Wire-SPI
Type	Chip Select Channel (CS) A0
3 Wire-SPI	Data Channel (SDA) A2
Use External dock	Chip Select Edge Data Edge
Clock Channel(SCK) A1	Active Low \checkmark Rising \checkmark
Bit Order MSB First	SDI(Write)-Latency-SDO(Read)
Word Size 8 bit (4~40)	Write Length 0 Latency 2
Data valid from SCK 0	Read Length 32776 (Bits)
Range Decode Range From To Buffer Head V Bu	o uffer Tail V Default OK Cancel

4 Wire-SPI dialog box →CS, SCK, SDI, SDO



Chip Select Channel (C	:S) A0		+
Data Channel (SDI)	A2	•	
Data Channel (SDO)	A1		•
Chip Select Edge	Active Low	\sim	
SDI Edge	Rising		
SDO Edge	Rising		
Show Data Channel	SDI only		

3 Wire-SPI dialog box → CS, SCK, SDA

nip Select Char ata Channel (S		A2
Chip Select Edg	e D	ata Edge
Active Low	~ F	Rising 🗸 🗸
SDI(Write)	-Latency-	SDO(Read)
Write Length	0	Latency 2
Read Length	32776	(Bits)

Click the SDI(Write)-Latency-SDO(Read) to show the dialog below.

The maximum length is 65535 (Bits)

Write Length	8	Latency	8					
Read Length	8	(Bits)	(Bits)					
ics								
ics — Ц scк — П			НЦГ					
				1				

3 Wire-SPI (Unused Chip Slave) dialog box → SCK, SDI, SDO



Data Channel (SDI)	A0	-				
Data Channel (SDO)	A2	•				
SDI Edge	Rising ~]				
SDO Edge	Rising ~					
Frame guard time	0	ns				
Show Data Channel	Both ~]				
scк		<u> </u>				
	<u> </u>	X_				

2 Wire-SPI (Unused Chip Slave) dialog box → SCK, SDA

- 1	SDO(Rea	Jul atency	
ncy 2		e)-Latency	SDI(Writ
	Later	0	Write Length
	(Bits)	32776	Read Length
	(Bits)	32776	Read Length

If the chip slave is not used and the interval between frames is not 0. You can set the

interval as 6us, any data bit higher than 6us will be seen as Idle.

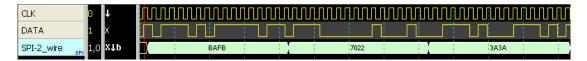
CLK D	ţ	ЛЛ	LUΠ	UUU		ЛЛ		Ш		UU	ՄՄՄ	U	ПЛЛ	JUU	ΓL	hur	nn	
DATA 2	x			_						٦								
SPI 2,0	х↑р		00		Idle		AA		Idle		84	Idle		00	Idle		00	Idle



Батуре	2 Wire-SPI(Un	used Chip S	Glave)	
2 Wire-SPI(Unused Chip Slave)	Data Channel	(SDA)	A0	
Use External dock	Data Edge	Rising	~	hannad
Clock Channel(SCK) A1	SDI(Write)-Latency-	SDO(Read)	
	Write Length	0	Latency 2	2
Bit Order MSB First \checkmark	Read Length	32776	(Bits)	
	-40) Frame guard	time	300	ns
Report ✓ Show Idle state in report windov Reduce report	N SCK			
Show Idle state in report window	SDA			
Show Idle state in report window Reduce report Show data in report (Column)	SDA			
Show Idle state in report window Reduce report Show data in report (Column) 16	SDA			
Show Idle state in report windov Reduce report Show data in report (Column) 16 or SDI/SDA/Write Channel	SDA			
Show Idle state in report window Reduce report Show data in report (Column) 16	SDA			
Show Idle state in report windov Reduce report Show data in report (Column) Solor SDI/SDA/Write Channel SDO/Read Channel	SDA			
Show Idle state in report windov Reduce report Show data in report (Column) 16 SDI/SDA/Write Channel SDO/Read Channel	SDA			

If the chip slave is not used and the interval between frames is 0. You can see the data

continuous as the dialog below.





SPI Settings	×
Setting Type 2 Wire-SPI(Unused Chip Slave) Use External clock Clock Channel(SCK) A1	2 Wire-SPI(Unused Chip Slave) Data Channel (SDA) A0 Data Edge Rising SDI(Write)-Latency-SDO(Read) Write Length 8 Latency 2
Bit Order MSB First ✓ Word Size 8 bit (4~40) Data valid from SCK 0 ✓ S/R Clk Report ✓ Show Idle state in report window Reduce report Show data in report (Column) 8 ✓	Read Length 8 (Bits) Frame guard time 300 ns SCK
Color SDI/SDA/Write Channel SDO/Read Channel Range Decode Range From To Buffer Head V Bu	iffer Tail
	Default OK Cancel

We also offer bi-direction mode as the dialog below.

SDI (Write)	Latency-SD	D(Read)		
Write Length	8	Latency	2	
Read Length	8	(Bits)		
Frame guard tin	ne 30	D		ns
SCK 1 SDA XV	Vrite		Read	

C heck the SDI(Write)-Latency-SDO(Read)to set the bit numbers for the 3 columns;

Write and Read (1~65535), Latency (0~65535).

Bit Order: MSB first or LSB first.



Word size: Default is 8 bits, minimum is 4 and maximum is 32.

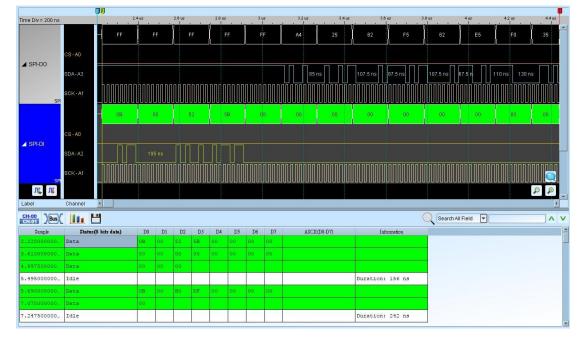
Report: Show Idle state in report window, You can disable this default for not to display the idle state on the Report Window.

Show data in report: Display the ASCII code with default 16 columns on the Report Window.

Data Valid from SCK: In some SPI devices, the data is not valid right after the data output or the clock edge. You can set the data valid after 0-3 units of the sampling rate in Data valid from SCK; if the unit is 1 and the sampling rate is 200MHz, the delay time is 5 ns.

Result

Click **OK** to run the SPI decode and see the result on the Waveform Window below.



3-Wire SPI, Internal clock mode

3-Wire SPI, External clock mode



fime Div= 5 us		140.67 us	164.6	7 us	169.67 us	164.57 us		169.57 u	s 1 1	174.5	7 us	170	9.57 us		184.67 us	189.57 us	s 1 1	194.57 us	109.5
		(20)SE		Addr:00		Addr:00			Addr.0	00	-		(05)RI	DSR1		D0:03			(35)RDSR2
	CS#-A19										1.u				18.5 us			1 u	
	SCLK-A18										2 ut	•						2 us	
Winbond-SFI:	SIO0 - A20																2 us	2.5 us	5 2 us 1 u
	SIO1 - A21																2 us		
	SIO2 - A22																		
Serial Flash	SIO3 - A23															8.94 us	3	a na na na ma	e
Serial Flash		(8.94 us	3		<u>)</u> ۹ ۹
Serial Flash																8.94 us h All Field			<u>)</u> ۹ ۹ ۸
Serial Flash	Channel			bà	liress(h)	PEM(h)	D0	D1	D2	D3	D4	D5	D6	D7	Searc	h All Field		formation	
Serial Flash A. M. Abel CH-00 CH-00 Timestsmp	Channel	1		6A 00000		PEM(h)	DO	D1	D2	D3	D4	D5	D6	D7		h All Field		formation	
Serial Flash Abel CH-00	Channel	Command (h)	1			PEMØI)	D0 03	DI	D2	D3	D4	D5	Dé	D7		h All Field		tormation	
Serial Flash A. M. .abel CH-00 Bus (Timestamp .44us .77.5000000	Channel (20) Sector (05) Read S	Command(h) Erase (4KB)				PEM(h)		DI	D2	D3	D4	D5	Dé	D7		h All Field		formation	
Serial Flash AL AL abel CH-00 Bus (Timestwap 44us 1.77.5000000 .95us	Channel (20) Sector (05) Read S (35) Read S	Command(h) Erase (4KB) tatus Register-	2			PEM(h)	03	Di	D2	D3	D4	D5	D6	D7		h All Field		ionmation	
Serial Flash 	Channel (20) Sector (05) Read S (05) Read S (05) Read S	Command(h) Erase (4KB) tatus Register- tatus Register-	2			PEM(h)	03 02	Di	D2	D3	D4	D5	D6	D7		h All Field		tomation	
Serial Flash	Channel (20) Sector (05) Read S (05) Read S (05) Read S (35) Read S	Command(h) Erase (4KB) tatus Register- tatus Register- tatus Register-	2 1 2			ΡΕΜΦ.)	03 02 03	D1	D2	D3	D4	D5	Dé	D7		h All Field		ionnation	



Serial Peripheral Interface NAND (SPI NAND)

SPI NAND Flash is a SPI/QPI interfaced NAND flash memory. The decoder translates the bus signal to command/address/data field to provide an easier way to exam the SPI NAND waveform.

Settings

SPI NAND Sett	ings						×
Parameter Settin	ngs —			1.5			
	A0	•	SCK	A1	-	Micron	~
SI/SO0	A2	-	SO/SO1	A3	-	MT29FXG01AAA	ADD .
WP/SO2	A4	-	HOLD#/SO3	A5	-		
Refer	to #Hold	status	5				
Start up r	rea <mark>d</mark> ing m	ode	Continuo	us Read	\sim		
Command	l deselec	t time			50ns		
Clock LOV	N to outp	ut vali	d 📕		15ns		
Color							
	e 📃		_ ~	Dumn	ny [~
Addres	s			Data	In [-
Data Ou	+					·	
Range			~				
Decod	e Range						
Fr Fr	om			То			
Bu	uffer Hea	d	~	Buffer T	ail	~	
			Defa	ult I		OK Can	cel
			Dela				CEI

CS#: Chip select

SCLK: Clock

SIO0 – SIO3: Data

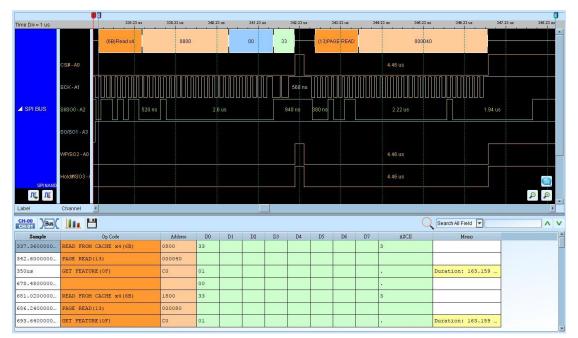
Start up reading mode: The initial setting of the reading mode for the decoder.

Command deselect time: The minimum required time for #CS deselecting. Clock



LOW to output valid: The data probe time after clock falling.

Result





SSI

The Synchronous Serial Interface (SSI) protocol has four kinds of signals: Serial Clock (SCK), Transmit Data, Receive Data and Transmit/Receive Frame Synchronous (FS). The SSI protocol supports either the Normal or Network mode that is independent of whether the transmitter and the receiver are synchronous or asynchronous.

Settings

5	Select Ch	nannel		Mode
1	SCK	A0		
	FS	A1	- 🚔	Normal
	DATA	A2	-	ONetwork
	Line Of D	ata		
		Transmit	C	Receive
	Merge	continuous	unknow	n
or —	nerge	011010000	CI IN ION	
D	Set color o	of data		
–	0	Hex		
	11	Hex		
	0	Hex		
	33	Hex		
ige —	-	-18 - L		
n.	Decode Ra	nge		
-	From		Το	() () () () () () () () () ()
	1000	Head		iffer Tail

Select Channel: Show the selected channels.



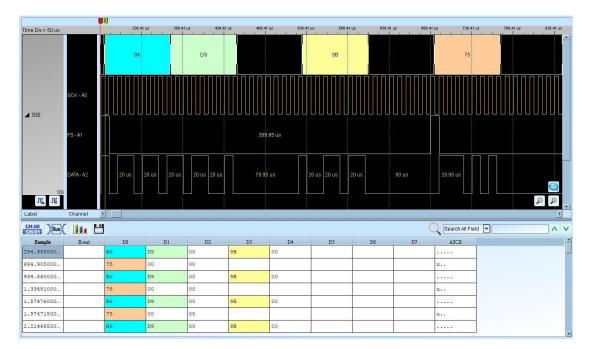
Mode: Normal or Network.

Line Of Data: Transmit or Receive.

Merge continuous unknown: Combine the unknown data only in Network mode.

Result

Click **OK** to run SSI decode and see the result on the Report Window below.





ST7669

ST76669 was developed by Sitronix to interface with the LCD module.

Settings

ST7669 9	Settings							?	×
Paramete	Type Channel Chip Selec Clock Cha	3 Wire-ST7669 ct Channel (/CS) annel (SCL)	A0 A1		Color	D/C Command Data Read			
		ta Input (MPU SI) ta Input (LCD SI)	A2 A3 A4						
Range	Decode Ran From Buffer Head		To Buffer Tail	~]				
							Default	OK	Cancel

Channel: Show the selected channels.

Result

Click OK to run the LCD1602 decode and see the result on the Waveform Window

below.



Time Div = 2 us					1		100		1		1		1		12		1						
	D/C	0x01								0									D/C	0x00		44	
	Chip Select-																						
▲ ST7669	SCL-A1	995 ns 1	us 🤅	990 ns	1.01 us	990 ns	1.01 us	990 ns	1.01 us	990 ns	1 us	995 ns	1 us	995 ns	1 us	995 ns	1 us	995 ns	1 us	995 ns	1 us	995 ns	
	MPU SI-A2								11.9	9 us							4	us					
	LCD SI - A3																						
ST7669	LCD SI-A3																						
ST7669																Sear	ch All Fie	Id		•			ø
ST7669	Channel •			Data	or Param	neter&Comm	rand		ID De	ta(Read)		ASCI	I		(Sean	ch All Fie	ld	5	•			ø
ST7669 A A A abel CH-00 Bus A Timestamp	Channel	Paramete	03	Dəta	or Param	neter/Comm	rand		ID De	ta(Read)		ASCI	I		(Sear	ch All Fie	ld	5				ø
ST7669 Abel CH-00 Bus Timestamp 3.47000000	Channel I		03	Dota	or Param	ueter/Commo	rand		ID De	ta(Read)			I		(Sear	ch All Fie	id	5	•			ø
ST7669 	Channel		_	Dəta	or Param	ueter/Comm	rand		ID De	ta(Read)			I		(Sear	ch All Fie	ld	5	•			ø
ST7669 A (A) abel CH-00 (Bus) Timestamp 3.47000000 19.4600000	Channel (DKC 0x01 (Data or 0x00 (Command)	Paramete	44	Dəta	or Param	reter/Comm	uand		ID De	ta(Read)			I		(Sear	ch All Fie	Id					ø
ST7669 A. A. A. Label CH.00 (Restance) Timestamp 33.47000000 L01.4600000 L19.4600000	Channel S D/C D/C D/C D/C D/C D/C D/C D/C	Paramete	44 05	Dota	or Param	veter/Comm	vand		ID De	ta(Read)	- - - - - -		I		(Sear	ch All Fie	ld					ø
ST7669 A. A. Label CH.00 S. 4700000 119.460000 217.490000 233.480000	Channel DC DXC1 (Data or 0x00 (Command) 0x01 (Data or 0x00 (Command)	Paramete	44 05 21 23	Dəta	or Param	veter/Comm	rand		ID De	ta(Read)			I			Sear	ch All Fie	Id		•			



Serial VID Interface 2.0 (SVI2)

The SVI2 protocol is an interface for power management and developed by AMD. The SVI2 working voltage is between 1V to 1.6V and its maximum frequency is at 20MHz with 3 bits : SVC/SVD/SVT.

Settings

Setting Image: SVI2.x SVI1.x SVC A0 SVD A1 Image: SVT A2 Image: SVT Color Image: Svid A1 Image: Svid A2 Image: Svid A1 Image: Svid A1 Image: Svid A1 Image: Svid A2 Image: Svid A1 Image: Svid A2 Image: Sv	SVI2 Settin	ngs			×
Color Start / Stop VDD Selector Acknowledge VDD Selector Acknowledge VDD Selector SVT0 SVT0 VDD Voltage VDD Voltage VDD Voltage VDD Voltage VDD NB Voltage VDD NB Current VDDNB Voltage From Example Decode Range From To Buffer Head Example	Setting	€ SVI2.x	⊖svI1.x		
Start / Stop PSI1_L VDD Selector TFN VDDNB Selector Icoad Line Slope Trim Acknowledge Offset Trim PSI0_L SVT0 VID Code SVT1 VDD Voltage VDDNB Current VDDNB Voltage VDDNB Current Decode Range To From To Buffer Head Market Trial		SVC A0	SVD A1		
Start / Stop > PSI1_L > VDD Selector > TFN > VDDNB Selector > Load Line Slope Trim > Acknowledge > Offset Trim > PSI0_L > SVT0 > VID Code > SVT1 > VDD Voltage > VDD Current > VDD NB Voltage > VDDNB Current > VDDNB Voltage > VDDNB Current > Decode Range To Buffer Head Suffer Tail >		-			
VDDNB Selector Acknowledge PSI0_L VID Code VDD Voltage VDD Voltage VDD NB Voltage VDDNB Voltage VDDNB Current VDDNB Voltage Decode Range From From Buffer Head					
Acknowledge PSI0_L VID Code VID Code VDD Voltage VDD NB Voltage VDDNB Voltage VDDNB Current VDNB Current Decode Range From From Buffer Head To			×	an and and and	<u> </u>
PSI0_L SVT0 VID Code SVT1 VDD Voltage VDD Current VDDNB Voltage VDDNB Current Pecode Range From To Buffer Head Buffer Tail			~	Load Line Slope Trim	×
VID Code SVT1 VDD Voltage VDD Current VDDNB Voltage VDDNB Current Pecode Range From To Buffer Head Buffer Tail		Acknowledge	×	Offset Trim	 ~
VDD Voltage VDD Current VDDNB Voltage VDD Current VDDNB Current VDDNB Current Decode Range To From To Buffer Head Buffer Tail		PSI0_L	~	SVTO	 ~
VDDNB Voltage VDDNB Current Range Decode Range From To Buffer Head Buffer Tail		VID Code		SVT1	— ~
Range Decode Range From To Buffer Head		VDD Voltage	~	VDD Current	 ~
Decode Range From To Buffer Head V Buffer Tail V		VDDNB Voltage	~	VDDNB Current	~
Decode Range From To Buffer Head \checkmark Buffer Tail \checkmark	Range	-			<u> </u>
	S			То	
		Buffer Head	~	Buffer Tail	~
Detault UK Cancel	- <u>1</u>			Default OK	Cancel



SVD: SVI2 data.

SVT: SVI2 telemetry data line. Telemetry will not be decoded if the SVT is not



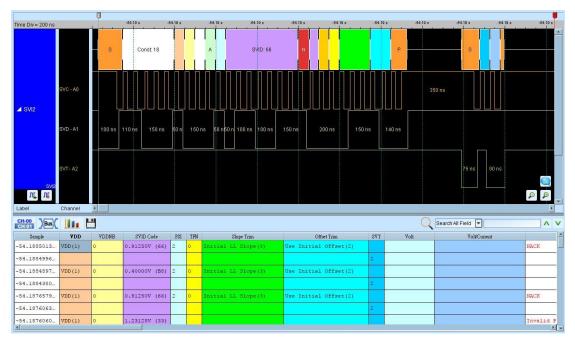
checked.

SVI2.x / SVI1.x: Select SVI2 / SVI protocol to decode.

Reduced Report: Only show SVD / VOTFC packet in the report window.

Result

Click **OK** to run the SVI2 decode and see the result on the Waveform Window below.





Serial VID (SVID) (Upon Request)

Serial VID (SVID) protocol is for power management and developed by Intel. SVID

voltage is between 1.0V to 1.1V, maximum frequency at 26.25MHz and is 3 wires :

SCLK/ SDATA/ ALERT.

Supported version:

IMVP7/VR12, VR12.1, VR12.5, VR12.6

IMVP8/VR13

IMVP9/VR14

If you have any issues with SVID protocol features, please contact your Intel Field Representative.

Settings

			1 🛓		2	
	VR Controller		Startup			-
	● Single ○ M	lultiple	PWM Spec.	VR12.0	~	
	Not to decode the fram		Fast slew rate	10	√ mV/us	
	Clock duty cycle is o Spec. range	ut of the	Slow slew rate	Fast/2		
Color						
U	Start	~	, End			~
	Address	~	Turn around			~
				1.0		
	Command	<u> </u>	ACK			- V
	Command MA. Payload	· · · · · · · · · · · · · · · · · · ·				
Range	MA. Payload		SL. Payload			
Range	MA. Payload		SL. Payload			



SClk: SVID clock.

SData: SVID data.

Alert: Alert, optional reminder.

VR Controller: Set single or multiple controllers in current VR. Set different address. **Not to decode the frame when its stop pattern wrong or clock duty cycle is out of**

range.

Result

Click OK to run the SVID decode and see the result on the Waveform Window

below.

		II)									
ime Div = 200 ns		2.08 ms	2.09 ms	2.09 ms 21	09 ms 2.09	ms 2.09 ms	2.0) ms 2.0	ims 2.09 m.	s 2.09 ms	2.09 ms
		Stait Addr.0	Cmd GetReg(7)	MA.PL:Protocol ID(0	5) End	Turn ACK(2)	SL.PL:01				
SVID	SCIK-AU								380	ns	
	SData - A1	280 n:	s 120 ns	200 ns	80 ns 170	ns 321) ns				
	Alert - A2										
SVD											
SVD N. N.		4									(
n, n,									Q Search All Fiel	d 💌	
ibel	Channel		MA. P.	syload (h)	SL. Payload	h) ACK		Emor	Search All Fiel	d ¥	
hbel Bus Sample	Channel	3	MA.P Protocol ID(05)		SL. Payload VR12.0/IMVP7			Enor	Search All Fiel	d V	
	Channel	Command(h)	Teles de la contraction de la		and the second second second second		3)	Error	Search All Fiel		
M. M. H-00 Bus Sample 084845000 087245000 087245000	Channel Channel Address(th) 0 0	Command(h) GetReg(7)	Protocol ID(05)		and the second second second second	(01) ACK(2)		Error	Search All Fiel	d	
M. M. abel Bus (Sample 084845000 087245000 093355000	Channel Address(h) 0 0 0	Command(h) GetReg(7) GetReg(7)	Protocol ID(05) Lot Code(04)		and the second second second second	(01) ACK(2) Reject(3	3)	Error	Search All Fiel	d ¥	
AL AL abel	Channel Address()) 0 0 0	Command(h) GetReg(7) GetReg(7) GetReg(7)	Protocol ID(05) Lot Code(04) Lot Code(04)		and the second second second second	(01) ACK(2) Reject(3 Reject(3	s) s)	Error	Search All Fiel	d ¥	
Abel	Channel Address(h) 0 0 0 0 0 0	Command(h) GetReg(7) GetReg(7) GetReg(7) GetReg(7) GetReg(7)	Protocol ID(05) Lot Code(04) Lot Code(04) Lot Code(04)	ode (03)	and the second second second second	(01) ACK(2) Reject(3 Reject(3	8) 8) 8)	Error	Search All Field	u a	•



Serial Wire Debug (SWD)

The SWD is a 2-pin electrical alternative JTAG interface that has the same JTAG protocol on top. It uses the existing GND connection. SWD uses an ARM CPU standard bi-directional wire protocol, defined in the ARM Debug Interface v5.

Settings

Parame	eter Settings Channel S			Sho	ow DP I	Reg bit assi	gnments	
:	SWDIO	A1	-	AP Se	etting	Filter Sett	ing	
	SWDCLK	A0	•	1000	ther	p		
	AP Select	Reg Start	up		EM-AP			
	Bar	k 0				AP Reg bit AP Startup	assignments	
	Ctrl	Sel 0	-		En	ndian	Big 🗸 😪	
	Bit Order				TAR /	Auto-Inc	Off 🗸 🗸	
	© LSI ○ MS	3 First 8 First			Acces	ss Size	32 Bits 🛛 🗸	
Color	-			10				
	Start			~	Par	k [-
	DP / AP] ~	Tur	n [7
	RnW				AC	< [7
	Addr				Dat	ta		1
	Stop				Par	ity		1
Range						L	1.0	
and the second	Decode Ra	ange						
***			. 1	Го				
	From Buffer He			Buffer T				

SWDIO: I/O data.

SWDCLK: Clock.

AP Select Reg Startup: When the AP Select Reg Startup is not assigned, only the



address information will be shown. You may input the Bank and Ctrl/Select initial values manually.

- AP Select Reg Startup						
Bank = 0	Time	Select	RnW	Address (h)	ACK	Data
	-0.0003 ms	AP	Write	0	OK	23 00 00 52
CtrlSel = 0						
- AP Select Reg Startup						
Bank = 0	ime Sel	ect RnW	Address	(h)	ACK	Data
	.0003 ms AP	Write	e Bank O	Register 0 (0)	OK	23 00 00 52
CtrlSel = 0						

Bit Order: LSB or MSB.

Show DP Reg bit assignments: Show the DP register information.

Select	RnW	Address (h)	ACK	Data	
DP	Write	SELECT Register (8)	OK	00 00 00 00	
				APSEL [31:24]	00
				APBANKSEL [7:4]	0
				CTRLSEL [0]	0

AP Setting:

JTAG-AP: Show the JTAG AP decode.

MEM-AP: Show the MEM AP decode.

Other: Show Bank X Register X.

Other	Time	Select	RnW	Address (h)		ACK	Data
○ JTAG-AP	-0.0003 ms	AP	Write	Bank 0 Register 0 (0)	OK	23 00 00 52
C MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (0	C)	OK	00 00 00 00
	2.9998 ms	AP	Write	Bank 0 Register 1 (4	4)	OK	00 00 02 68
O Other	Time	Select	RnW	Address (h)		ACK	Data
• JTAG-AP	-0.0003 ms	AP	Write	CSW Register (0)	OK	23 00 00 52
C MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (0	C)	OK	00 00 00 00
	2.9998 ms	AP	Write	PSEL Register (*	4)	OK	00 00 02 68
O Other	Time	Select	RnW	Address (h)		ACK	Data
○ JTAG-AP	-0.0003 ms	AP	Write	CSW Register (0)	OK	23 00 00 52
MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (0	C)	OK	00 00 00 00
- HEPFAF	2.9998 ms	AP	Write	TAR Register (*	4)	OK	00 00 02 68

Show AP Reg bit assignments: Display the AP register information if JTAG-AP or

MEM-AP checked.



MEM-AP	Select	RnW	Address (h)		ACK	Data	
Show AP Reg bit assignments	AP	Read	BASE Register	(8)	OK	00 00 00 00	
						BASEADDR [31:12]	EOOFF
						Format [1]	1
						Entry present [0]	1

MEM AP Startup: Assign the initial MEM-AP value.

۰ ا	MEM-AP		AP	Read	DRW Register	(C)	OK	00 00 00 0D	TAR Address = E000EFF0
	Show AP Reg bit	assignments						Big-Endian	
	FMEM AP Startup							000D Access to E000EFF0	
	🔽 Endian	Big 💌						0000 Access to E000EFF2	
			AP	Read	DRW Register	(C)	OK	00 00 00 E0	TAR Address = E000EFF2
	TAR Auto-Inc	Single 💌						Big-Endian	
	Access Size	16 Bits 💌						00E0 Access to E000EFF2	
								0000 Access to E000EFF4	

Filter Setting: Filter the unwanted Registers.

AP Setting Filter Setting
Register Display List
DP - ABORT Register
DP - IDCODE Register
DP - CTRL/STAT Register
DP - WCR Register
DP - SELECT Register
DP - RESEND Register
DP - ROUTESEL Register
DP - RDBLIEF Register

Result

Time Div = 500 ns		T	18.01 ms	18.01 ms 18.01 m	s 16	3.01 ms 18.01 ms	18.01 ms	18.01 ms	18.01 ms	18.01 ms	18.01 ms	18.01 ms
		STA	RT SELECT	:DP MODE : Read	ADDF	R: IDCODE Register	PARITY	STOP	PARK		TURN	ACK
⊿ SWCLK	SWCLK-A1		200 ns 300 ns	300 ns 200 ns 300 ns	300 ns	300 ns 200 ns 300 ns	300 ns 300 ns	200 ns 300 ns	300 ns 5	500 ns 200	ns 300 ns	300 ns
SWD	SWDIO - AO		600 r	ns 500 ns		1.1.us	600 ns	500 ns				
			4									
Label	Channel	•										
JLabel		•							Q Sea	arch All Field 💌][
N, N Label				Address (h)	ACK	Deta	En	TOT Message	Q Sea	arch All Field 💌]	<u>}</u>
AL AL	Select	<u> </u>	IDCODE Registe		ACK	Deta 05 B1 14 77	En	tor Message	Q Sea	arch All Field 💌][<u>}</u>
Label CH-00 CH-00 CH-01 Sample 18.00790000	Select DP	RnW Read	and a second	er (0)	1.0.0	A REAL AND A REAL	En	TOT Message		arch All Field 💌] [<u>}</u>
Label CH-00 CH-01 Sample 18.00790000	Select DP DP	RnW Read Write	IDCODE Registe	er (0) c (0)	OK	OB B1 14 77	Err	tor Message		arch All Field 💌)[<u>}</u>
M. M. Label CH-00 Bus (CH00 Bus (Sample 18.00790000 36.000900000 36.000900000	Select DP DP DP	RnW Read Write	IDCODE Registe ABORT Register	er (0) c (0) er (8)	OK OK	0B B1 14 77 00 00 00 1E	En	ror Message	Q Sea	arch All Field 💌		<u>}</u>
M. M. Label Bus CH-00 Bus Sample 18.00790000 36.000900000 39.000900000	Select DP DP DP DP DP	RnW Read Write Write	IDCODE Registe ABORT Register SELECT Registe	er (0) c (0) er (8) Lster (4)	OK OK OK	0B B1 14 77 00 00 00 1E 00 00 00 00	En	TOT Message	Q Sea	arch All Field 💌		<u>}</u>
M M Label Sample 18.00750000 36.00090000 39.00090000 42.00090000 45.00130000 45.00130000	Select DP DP DP DP DP DP DP	RnW Read Write Write	IDCODE Registe ABORT Register SELECT Registe CTRL/STAT Regi	er (0) : (0) er (8) 	OK OK OK OK	0B B1 14 77 00 00 00 1E 00 00 00 00 50 00 00 00	En	TOT Message		arch All Field 💌		<u>}</u>



SWP

The Single Wire Protocol (SWP) is a single-wire connection between the SIM card and a NFC chip in a cell phone.

Settings

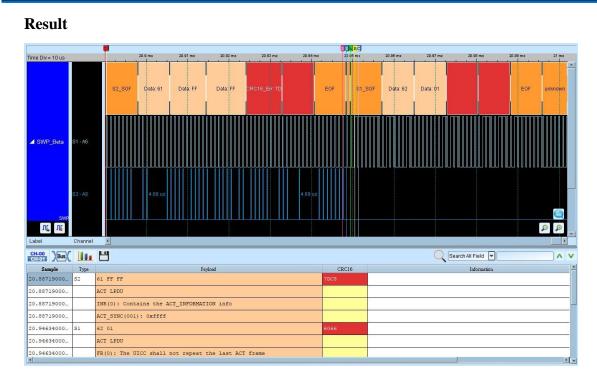
SWP Settin	gs			×
Channel	Channel S1 CH 0 V S2 None V Data Link Layer: O MAC O LLC	Range	Decode Range From Buffer Head V To Buffer Tail V	
Color	SOF/EOF Payload CRC16 V			
		Default	OK Cance	el

S1: I/O data.

S2: I/O data in current domain and it need convert to voltage domain.

Data Link Layer: Supported MAC and LLC layers







Universal Asynchronous Receiver/Transmitter (UART)

The UART (RS-232 or RS-485) protocol has two message types: Transmitter (TX) and Receiver (RX); you can measure the UART protocol in one signal or two signals. RS-485 need convert to logic signal, because LA can not capture differential signal.

Settings

arameter	Settings		Line Wrap	Data	and the second
	Channel Tx A0			Users can assign Line Wra Default setting is 0A. (Hex Line Wrap Data	p Data as header of data. kadecimal)
	Auto Detect			1st Pattern C	Color
	Baud Rate	Data Bits		0A	
	9600 ~	8 ~		2nd Pattern	
	Parity	Stop Bits		0A	
	None 🗸 🗸	1 ~			
	—		Range	1 S.	
		Show scale in the waveform	M	Decode Range	
	Show Idle state in r	report window		From	То
				Buffer Head 🛛 🗸 🗸	Buffer Tail 🛛 🗸 🗸

Data: Show the selected channel (CH0).

Rx: Show Rx data in report window.

Auto: Shows High or Low when auto detection Idle.

Idle high: Idle condition shows High.

Idle low: Idle condition shows Low.

Auto Detect: Set the Baud Rate manually if not selected.

Baud Rate: Data rate (bits per second), and the range is 110 ~ 2M (bps).

Protocol: (Parity - Data Bits - Stop Bits)

Parity: N (None), O (Odd), or E (Even).



Data Bits: 5 to 10 bits.

Stop Bits: 1 to 2 bits.

MSB first: The default is LSB first; click it to change to MSB first.

Report Unknown and Idle: Display the unknown and idle data in the Report

Window.

Show scale in the waveform: Display the waveforms with scales.

Line Wrap Data: Use 1-2 value (hex) as header of data.



Result

lime Div = 100 us		ľ		4	48.61 us		H) 548.6	1 us		348.61 us		748	.61 us		848.61 u	us	0	48.61 us	1.05 ms	1.16	ms	1.26 ms	1.36 ms	1.45	5 ms
								70		AC	T	61		2	3		D0	43	70		AC				
CH-00	Tx - A0						44 us	26 u	26 u			36 us				44 u	s 2	17 u 35 us	44 us 27 (1 27 1	,				
UART(RS232)																									
JL JL	Channel																							<u>و</u>	€
abel		Ľ																				arch All Field 💌		<u>و</u>	E.
abel		D0	D1	D2	D3	D4	D5	D6	D7	DØ	D9	D10	D11	D12	D13	D14		ASCI	1	(Information		<u>و</u>	€
ALL		D0	D1 AC	61	2B	DO	43	70	AC	DØ	D9	D10	D11	D12	D13	D14		p.a+.Cp.	1	(<u>و</u>	€
AL AL		70 70	D1 AC AC	61 61	2B 2B	D0 D0	43 43	70 70	AC AC	D8	D9	D10	D11	D12	D13	D14		p.a+.Cp. p.a+.Cp.	1	(Information		<u>و</u>	€
AL AL		D0	D1 AC	61	2B	DO	43	70 70 70	AC AC AC	De	D9	D10	D11	D12	D13	D14		p.a+.Cp.	1	(Information		<u>و</u>	€
M. M. Label Bus Sample 512us 2.446000000 4.380000000		70 70	D1 AC AC	61 61	2B 2B	D0 D0	43 43	70 70 70	AC AC	D8	D9	D10	D11	D12	D13	D14		p.a+.Cp. p.a+.Cp.	1	Gaud r		Information		<u>و</u>	€
N. N. Label Sample S12us 4.38000000 5.314000000 5.314000000		70 70 70 70	D1 AC AC AC	61 61 61	2B 2B 2B	D0 D0 D0	43 43 43	70 70 70 70	AC AC AC	D8	D9	D10	D11	D12	D13	D14		p.a+.Cp. p.a+.Cp. p.a+.Cp.	1	(Information		<u>و</u>	€
Л <u>,</u> Л <u>,</u> Label CH-00 CH01)Bus (70 70 70 70 70 70	D1 AC AC AC AC	61 61 61 61	2B 2B 2B 2B	D0 D0 D0 D0	43 43 43 43	70 70 70 70 70	AC AC AC AC	D8	D9	D10	D11	D12	D13	D14		p.a+.Cp. p.a+.Cp. p.a+.Cp. p.a+.Cp.	1	(Information		<u>و</u>	€

Click **OK** to run UART Decode and see result on the Waveform Window below.



UNI/O

The UNI/O interface was developed by Microchip. The data transfer rate is 10Kbps to 100Kbps.

Settings

UNI/O Settings			×
Parameter Channel SCIO Device Address 8 bits Tolerance	A0	Color Start Head MAK/NoMA SAK/NoSAk Unknown Device Add Command	к с~
Input Edge Jitter To Output Edge Jitter T Report Setting	±10% ~	Address Data Hold Standby Pu	
	8 Columns V To Buffer Tail V		
			Default OK Cancel

Channel: Show the selected channels (SCIO CH0).

Device Address: Set data bits for the device address.

Tolerance: Set the Input / Output Edge Jitter Tolerance, $\pm 10\%$ / $\pm 25\%$ default.

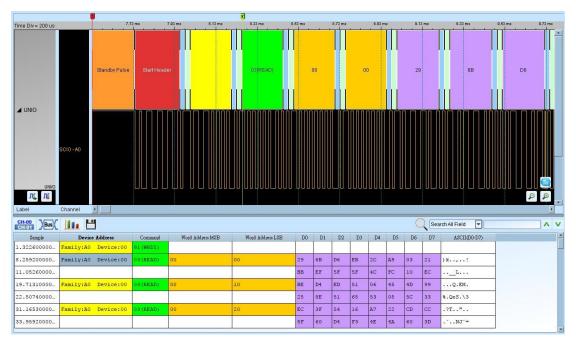
Report Setting: To show the data by 8 or 16 columns in the Report Window.

Result



Click **OK** to run the UNI/O decode and see the result on the Waveform Window

below.





USB1.1

The USB 1.0 specification was introduced in 1994. USB signals are transmitted on a twisted pair data cable with 90 Ohm $\pm 15\%$ impedance, labeled D+ and D-.

Settings

USB1.1 Se	ettings				?	×
Parameter	Channel D+ A0 D- A1 USB 1.1 Setting	• • •	Range	Decode Range From Buffer Head V	To Buffer Tail	~
	Auto Detect O Low speed Decode USB standard req			Sync Packet ID Frame No. / Address /		- ~ - ~
	Report Setting Mark PID Show Data	SOF × 8 Column ×		Endpoint/ Data CRC5/CRC16 EOP Host To Device /		
	PID Filter			Device To Host Type Recipient		 ✓ ✓ ✓ ✓
	IN NACK			bRequest wValue wIndex		- ~ - ~ - ~
[Show scale in the waveform			wLength Descriptor		- ~ - ~
					Default Ok	Cancel

Channel: Show the selected channels (D+ CH0 and D- CH1).

USB1.1 Setting: Select USB state (low speed or full speed) and decode the USB

standard request and descriptor.

Result

Click **OK** to run the USB1.1 decode and see the result on the Waveform Window.



		.73 ms	7.93 ms 8.13 ms	8.33 ms 8	63 ms	8.73 ms		8.93 ms	9.13	ms ,	9.33 ms	9.63 ms	0.73 ms
	Standby Puls	Start Head	er	03(READ)	00		00		29		6B	D6	
	SCIO - A0												
UNVO													
Λ Γ Λ Γ	Channel 🕚												Q Q
JL JL	Channel ·									C Sea	rch All Field		
ALL ALL		Command	Word Address MSB	Word Address LSB	DO	D1 D2	D3	D4 D5	D6	Seal	ch All Field 💌		
ALE	. <u>III.</u> 💾		Word Address MSB	Word Address LSB	DO	D1 D2	D3	D4 D5	D6				
AL AL .abel Bus CH-00 Bus Sample .322600000	Device Address	91(WRDI)	Word Address MSB	Word Address LSB	D0 29 61			D4 D5	D6				
N. N. .abel	Device Address Family:A0 Device:00	91(WRDI)				3 D6	EB :			D7	ASCII(D0-D7)		
Λ[Λ[.abel Bus Sample .322600000	Device Address Family:A0 Device:00	91 (WRDI) 03 (READ)			29 61	3 D6 F 5F	EB :	2C A9	03	D7 21	ASCII(D0-D7)		
N. N. Label Sample 1.322600000 1.05260000 1.105260000 9.71310000	Device Address Family:A0 Device:00 Family:A0 Device:00	91 (WRDI) 03 (READ)	00	00	29 61 BB E1	3 D6 7 5F 1 ED	EB 2 5F 4 51 (2C A9 8C FC	03	D7 21 EC 99	ASCII(D0-D7)		
Label	Device Address Family:A0 Device:00 Family:A0 Device:00	91 (WRDI) 03 (READ) 03 (READ)	00	00	29 61 BB E1 BE D-	3 D6 5 5F 4 ED 5 1	EB 2 5F 4 51 0 65 9	2C A9 4C FC 06 45	03 10 4D	D7 21 EC 99	ASCII(D0-D7)		



USB PD 2.0/3.0

USB PD (Power Delivery) 2.0 is the protocol based on BMC (Biphase Mark Coding) and can be applied to Laptops / Tablets / Mobile phones / Power banks or other devices with USB Type-C for power supplying or charging. The maximum power offered by USB Type-C can be 100W, and the users can charge the device by supporting USB Type-C connector.

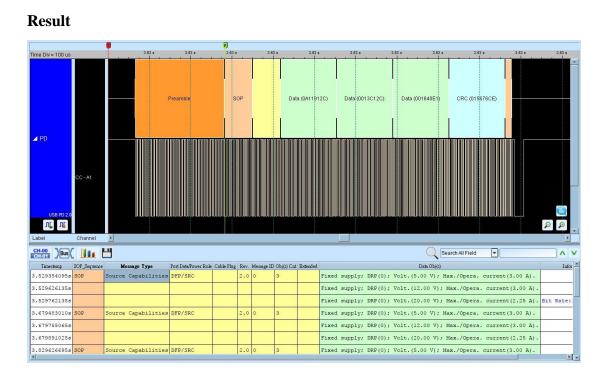
Settings

USB Power Delivery 3.0 Settings	×
Channel Configuration Channel (CC)	Color Preamble SOP / EOP Header Extended Header
Show 5b value in waveform window	Data Object(s)
Range Decode Range From Buffer Head V	To Buffer Tail 🗸
Def	ault OK Cancel

Channel: Set Configuration Channel (CC).

Show 5b value in waveform window: Show 4b or 5b value in the waveform.







Wiegand

It is commonly used to connect a card swipe mechanism to the rest of an electronic

entry system..

Settings

Wiegand S	ettings	×
Channel	Channel	
	Data 0 🛛 A0 🗸 🗸	Data 📃 🗸
	Data 1 🛛 A1 🗸 🗸	Parity 📃 🗸
Range	Decode Range From	
	Buffer Head 🛛 🗸 🗸	
	То	
	Buffer Tail 🛛 🗸	
		Default OK Cancel

Channel: Show the selected channels (Data 0 and Data 1).

Result

Click **OK** to run the wiegand decode and see the result on the Waveform Window.



WG Data 0-A0 448 ms 448 ms 3.31 ms 3.34 ms 3.31 ms 5.62 ms 2.17 m 2.17 m Wegens Data 1-A1 3.33 ms 2.17 m 2.37 m 4.46 ms 2.17 m 2.17 m 2.17 m 2.17 m Wegens Channel	WG Data 0 - A0 Ja		-6 ms	0 ps	6 ms 10	ms 16 ms	20 ms	25 ms	30 ms	35 ms	40 ms	46 ms
Vergend 3.53 ms 2.17 m 2.17 m 2.17 m 2.17 m 4.45 ms 3.31 ms Wegend Image: Channel	Wegene 3,33 ms 2,17 m 2,17 m 4,45 ms 2,17 m 4,45 ms 3,31 ms Wegene Image: Channel Image: Ch	me UN = 5 ms										
Wregard Image: Channel Image: Chann	Wregene R, R, R sabel Channel Search All Field Search All Field Search All Field Sample D0 D1 D2 D3 D4 D5 D6 D7 Even parity Old parity Information	✔ WG Data 0 - A0		4.4	6 ms 4.48 ms	3.31 ms	.3.34 ms 3.31 ms	5 5.62 ms	2.17 m	2:17 m		
CH.00 Cel.00 Cel.00 </td <td>CH.00 CH.01 CH.02 Search All Field Search All Field A Sample D0 D1 D2 D3 D4 D5 D6 D7 Even pairly Odd pairly Information</td> <td></td> <td></td> <td>3,33 ms</td> <td>2.17 m 2.</td> <td>17 m 4.45 ms</td> <td>2.17 m 2</td> <td>2.17 m</td> <td>4.45 ms 3.3</td> <td>ri ms</td> <td></td> <td></td>	CH.00 CH.01 CH.02 Search All Field Search All Field A Sample D0 D1 D2 D3 D4 D5 D6 D7 Even pairly Odd pairly Information			3,33 ms	2.17 m 2.	17 m 4.45 ms	2.17 m 2	2.17 m	4.45 ms 3.3	ri ms		
Sample D0 D1 D2 D3 D4 D5 D6 D7 Even parity Odd parity Information	Sample D0 D1 D2 D3 D4 D5 D6 D7 Even pairly Odd parity Information	NL IN										
		Label Channel										Þ
UDB BB B7 B9 D <thd< th=""> D <thd< th=""> D</thd<></thd<>	JODE 379 87 87 89 1: OK 0: OK Image:	Label Channel Channel Channel							Q	Search All Field		
		AL A		D5 D6			Information		Q	Search All Field		Ě
		AL AL Channel Channel Channel Channel Semple D0 D1 I		D5 D6			Information		Q	Search All Field		Ě
		Label Channel « CH400 DBus D0 D1 I		D5 D6			Information		Q	Search All Field		ŀ
		Label Channel « CH400 DBus D0 D1 I		D5 D6			Information		Q	Search All Field		ŀ
		Label Channel « CH400 DBus D0 D1 I		D5 D6			Information		Q	Search All Field		<u>•</u>



Chapter 2 Bus Trigger



Bus Trigger

Bus Trigger	TravelLogic B+	TravelLogic B	TravelLogic E	TravelLogic
CAN	O	Ô		0
eSPI	Ô			
I2C	Ô	Ô		\odot
128	Ô	Ô	Ô	\bigcirc
LIN	Ô	Ô		
LPC	Ô	Ô		
MIPI SPMI	Ô			
NAND Flash	Ô			
SD/eMMC	Ô			
Serial Flash	Ô			
SMBus/PMBus	Ô	\bigcirc		
SPI	Ô	\bigcirc		\odot
SVI2	Ô	Ô		
SVID	Ô	Ô		0
UART	Ô	\bigcirc		\odot
USB 1.1	Ô	Ô		

The bus trigger are only available for the TravelLogic Series.



Clause Trigger

LPC Trigger 🔨 ng	2		<u>o</u> 4 💌
Channel LFRAME# CH 0 • LCLK CH 1 •	Run State 1 T1 T2	→ True → False	State 1 Logic Condition OR AND Event 1 × Event 2 × + OR Image: AND Timer 1 >= v 0.000 ns Cycle Type Memory Read Image: AND Timer 2 >= v 0.000 ns
	State 2	> Trigger	Clk #
LAD[1] CH 3 +			Three Topological CT/DIR 1 010Xb Image: Reset Counter 2
LAD[3] CH 5			ADDR = 8 7654XXXXh
Clock Edge		→ ▼ Trigger ×	TAR 2 XXh SYNC 1 Xh
Error Trigger Option			DATA 2 ABh XXh XXh XXh
CT/DIR Error		+ State x 4	
Address Error (Bus Master)		+Counter x 2	Data Offset
(DMA)			Fix Offset 1+
Size Error		Timer 1 Timer 2	<< Advanced Setting
Sync Error			載入 存檔
Undo Redo	Pre-Trigger Pass Co	ount 0 🛨	

The Clause trigger settings dialog box is as below.

1. Channel and bus trigger settings:

Please refer to the descriptions in each bus trigger settings section.

2. Flow chart

$ \begin{array}{c} Run \\ \hline \\ State 1 \\ \hline \\ \\ \hline \\ State 2 \\ \hline \\ \\ \hline \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\$	$ \begin{array}{c} Run \\ \hline \\ State 1 \\ \hline \\ \end{array} \end{array} False \\ \hline \\ Trigger \\ \hline \\ \hline \\ Trigger \\ \hline \\ \end{array} $	Run State 1 State 1 State 2 State 2 State 2 Trigger Trigger Trigger
State 1 next State 2	State 1 then State 2	State 1 next State 2 then State 3 next State 4



$ \begin{array}{c} & \underset{\text{State 1}}{\overset{\text{WIN}}{\longrightarrow}} & \underset{\text{False}}{\overset{\text{Trigger}}{\longrightarrow}} \\ & \underset{\text{State 2}}{\overset{\text{Trigger}}{\longrightarrow}} \\ & & \underset{\text{Trigger}}{\overset{\text{WIN}}{\longrightarrow}} \end{array} $	$ \begin{array}{c} \text{Run} & \longrightarrow & \text{True} \\ \text{State 1} & \longrightarrow & \text{False} \\ \text{State 2} & \longrightarrow & \text{Trigger} \\ \end{array} $	
State 1 (Active T1)	State 1 (Active T1)	
next State 2 (Time >= T1)	next State 2 (Time < T1)	

A state button represents a trigger state. The true state condition will only lead the branch to the next state, on the other hand, the false state condition could lead the branch to any state as below:

Click state 1 and state 2, then state 1 will branch to state 2 while state 1 is false.

Double click any state, the state will branch to itself if it is false.

Click the state button and trigger button (**Trigger**): triggere when the state

conditions is satisfied.

Delete any state by clicking the cross sign on the state.

Clear the links to the trigger button by clicking on the trigger button (♥ Trigger |[×])

Click + State x 4 and + Counter x 2 to add a new state.

Timer 1 : The timer ranges from 5 ns to 8 days.



3. State settings

	Clk #	
START	1	0000b
CT/DIR	1	010Xb
ADDR =	8	7654XXXXh
TAR	2	XXh
SYNC	1	Xh
DATA	2	ABh XXh XXh XXh
		4

The trigger conditions of the state:

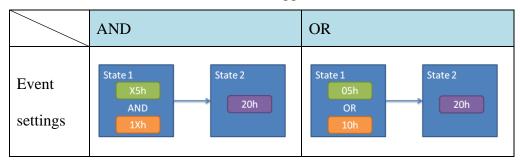
- 1. The current state index
- 2. Logic condition between every event in the state.
- 3. Switch between the tab windows to edit the trigger events . Click + OR / /

|+AND] to add new events (up to 8 events). All inputs are supported binary(e.g.

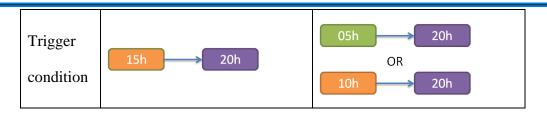
01000001b)/decimal(e.g. 65)/ hexadecimal(e.g. 41h)

4. The bus trigger settings.

The relations between events and the trigger condition:

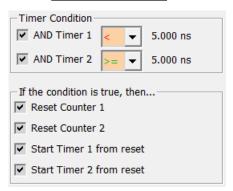






4. Timer and Counter settings

Press Advanced Setting >> button to edit the timer/counter reset settings of the state.



The following table describes the state button icons:

	Run State 1	State 1	State 1	State 1 T1 T2 C1 C2 T1 T2
	State 1		State 1	State 1
Conditions	State 1	And	And	And
			timer < T1	T2 < timer <t1< td=""></t1<>
satisfied	Stort T1	X	Start T2	Start T1 and T2
condition	Start T1	Δ	Reset C2	Reset C1 and C2



CAN Trigger

Supported Models : TB1016B. TB1016B+. TL3134B. TL3234B+. LA3068B.

LA3136B

CAN Trigger Settings

Click CAN Trigger in the toolbar and will show the dialog as the following $\,^\circ$

M CAN Trigger Setti	ngs				×
Channel	Clause Trigger				
Channel Channel CAN Port LA Port CAN L CAN	Clause Trigger Run State 1	→ True → False → Trigger → Trigger * → State x 7 → Counter x 2	Byte 3 Byte 5	11 Bits ID XXh Byte 2 XXh Byte 4 XXh Byte 6 XXh Byte 8	OR OR XXh XXh XXh XXh XXh XXh
 Default 				✓ OK	× Cancel

- 1. Channel: Select CAN_H or CAN_L as the trigger channel.
- 2. Data Rate: CAN data rate. Users could type the data rate if no data rate is available.
- 3. Simple Trigger: Specific trigger function of CAN.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side; there are



11 Bits ID, 29 Bits ID, Data, 11 Bits ID + Data and 29 Bits ID + Data selections in the Trigger On; selecting one of them and typing the trigger values in the ID or Data fields, default value is XX means "don't care".

Note: Only TB1016B. TB1016B+ provide CAN port channel



DALI Trigger

Supported Models : TB1016E, TB1016B, TB1016B+, TL3134B, TL3234B+,

LA3068B, LA3136B

DALITrigger Settings

Click DALI Trigger in the toolbar and will show the dialog as the following.

∭ DALI Trigger Settings		Х
Channel	Clause Trigger	
DALI 0	Run State 1	
Data Rate 1200 bps Simple Trigger Start of frame End of frame	$False$ $False$ $False$ $Trigger$ $Address byte$ $Short Address = 0$ $Data byte$ O_OFF $Data (8 bits)$ $Address byte$ 01	
O Default		✓ OK X Cancel

- 1. Channel: Select channels.
- 2. Simple Trigger: Trigger specific of DALI.
- 3. Clause Trigger: Please reference Clause Trigger chapter.
- 4. State: Show the details of trigger condition in every state as left side; selecting the trigger type of DALI (102, 103), command type (short address, group address, broadcast, response, special command), or custom cmd.



eSPI Trigger

Supported Models : TL3234B+. LA3068B. LA3136B

eSPI Trigger Settings

Click eSPI Trigger in the toolbar and will show the dialog as the following.

∭ eSPI Trig	ger Settings						?	×
Channel		Clause Trigger						
CS#	0	Run		State 1				
SCLK	1	× 5	> True			Logic OR	l O Logi	AND
I/O 0	2 🗘	State 1		Event 1				OR
I/O 1	3 🌲		→ False	Command	Any Comman	d (00h)		-
I/O 2	4		→ Trigger	Response	Any Response	· · /		F
I/O 3	5 🗘			Data Dir	 Command 	O Res	ponse	
Alert	6 🗘			Data Offset	🖌 Any Ofs 🔲		·	-0+
Start up sett	ings		→ ▼ Trigger [×]		mmand	· · · ·	onse	
Single Mod	le 🔻				PCode XXh		oonse Xh	
Alert From	1/0[1]		+ State x 7		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		<u>^</u> 11	
	k Enable		- -					
			🕂 Counter x 2					
Trigger on								
Format	Error							
OPCod	e Error							
	ise Error				,			
Status I								
CRC E	rror							
tCLQV 15ns	5							
 Default 						✔ ОК	×C	ancel

- 5. Channel: Select channels.
- 6. Startup settings: Set the initial parameters of eSPI.
- 7. Trigger on: Trigger specific error of eSPI.
- 8. Clause Trigger: Please reference Clause Trigger chapter.
- 9. State: Show the details of trigger condition in every state as left side; selecting

the trigger values in the Command, Response fields, default value is 00h.

Data Dir: Trigger the data in the Command or Response.



Timestamp	OpCode/Response	CycType	Tag	LEN	Address	DO	D1	D2	D3	D4	D5	D6	D7	ASCII	Status	CRC	Memo
-0.00000245 S	GET CONFIGURATION(21)			_	0010									_		5.5	
0.00000086 5	ACCEPT (08)					13	11	00	00						0305	95	
0.000003 S	SET_CONFIGURATION (22)			_	0010	01	11	00	00							25	
0.000005935 S	ACCEPT (08)														030F	98	
0.000008455 5	GET_STATUS (25)															FB	
0.000009365 5	ACCEPT (08)														030F	98	
0.001601195 5	GET_CONFIGURATION(21)				0010											58	
0.001602795 S	ACCEPT(08)					13	11	00	00						0302	95	
0.001606635 5	SET_CONFIGURATION (22)				0010	01	11	00	00							75	
0.001609575 S	ACCEPT(08)														030F	98	

Data Offset: **Trigger the data from start of data frame without any offset. For example, setting D0 13h will check the first byte of data frame. With any offset, the siganl would be triggered by the byte pattern. For instance, setting D0+ XXh D1+ 11h, and the byte pattern of XXh and 11h will be triggered regardless of the position of the data.**



HIDoverI2C Trigger

Supported Models : TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+.

LA3068B. LA3136B

HIDoverI2C Trigger Settings

Click HIDoverI2C Trigger in the toolbar and will show the dialog as the following.

M HIDoverI2C Trigge	er Settings				×
Channel	Clause Trigger				
 I2C Port LA Port SCL 0 ‡ SDA 1 ‡ Simple Trigger Start of frame Repeat Start Stop of frame ACK NACK 	Run State 1	 True False Trigger Trigger State x 7 Counter x 2 	State 1 Event 1 Address Mode [7-Bit Addr Value XXh Data XXh WHIDDescLength Report Descrip USAGE_PAGE (05 USAGE_PAGE (05 USAGE_PAGE (05 USAGE_PAGE (05 USAGE_MINIMUM USAGE_MINIMUM DESIGNATOR_INI DESIGNATOR_INI	R/W A	+ OR CK
 Default 				✓ OK	× Cancel

- 1. Channel: Select I2C / LA port.
- 2. Simple Trigger: Specific trigger function of I2C.
- 3. Clause Trigger: Please reference Clause Trigger chapter.
- 4. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the R/W, ACK and Data(HID Descriptor) fields, default value is XX means "don't care". When trigger the descriptor, R/W field



will be selected Read state automatically.

Note: Only TravelBus series provide I2C port channel



I²C Trigger

Supported Models : TravelBus series. TravelLogic series. Logic Analyzer series

I2C Trigger Settings

Click I2C Trigger in the toolbar and will show the dialog as the following.

∭ I2C Trigger Settin	igs			×
Channel	Clause Trigger			
		 True False Trigger Trigger * State x 7 Counter x 2 	2/W A(▼ [
 Default 			✓ ОК	× Cancel

- 1. Channel: Select I2C / LA port.
- 2. Simple Trigger: Specific trigger function of I2C.
- 3. Clause Trigger: Please reference Clause Trigger chapter.
- 4. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the R/W, ACK and Data fields, default value is XX means "don't care". Data field only provided 4 bytes data to trigger, checking the Fixed offset and selecting the offset value when want to trigger at the specific



position.

Note: Only TravelBus series provide I2C port channel



I²S Trigger

Supported Models : TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+.

LA3068B. LA3136B

I2S Trigger Settings

Click I2S Trigger in the toolbar and will show the dialog as the following.

👖 I2S Trig	ger Setting	s		×
Channel				
SCК р	۵ ۱	WS 1 🗘	SD 2	\$
Data Bits (8		•	Bits
Method	Data Match]
Data Trigge	er			
Channel	I 🔍 Both	○ Left	 Right 	
Pattern	Unit 🔍 Value	e O Volta	age ○ dB	
Pattern	=			•
(00h			
Duration	(# of frames	s) [1		
 Defau 	ult	✓ OK	× Can	cel

- 1. Channel: Select Serial clock (SCK), word select (WS) and serial data (SD).
- **2. Data Bits:** 1-32 bits, normally it is 8, 12, 16, 24 or 32.
- 3. Method:

Data Match : Trigger when the conditions matched.Rising Edge : Trigger when it is a rising edge between two patterns.Falling Edge : Trigger when it is a falling edge between two patterns.Glitch : Trigger when there is a glitch.

Mute : When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of -P < X < +P.



- Clip : When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of -P < X ∪ +P > X.
 Timing Violation : Provide 6 trigger conditions and this function will be enabled at 200 MHz sampling rate.
- 4. Data Trigger: Select Both, Left, Right channel and pattern unit.



LIN Trigger

Supported Models : TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+.

LA3068B. LA3136B

LIN Trigger Settings

Click LIN Trigger in the toolbar and will show the dialog as the following.

∭ LIN Trigger Settings	;				×
Channel	Clause Trigger				
CH 0 🗢	Run		State 1		
Data Rate	State 1	> True	Event 1		🛉 OR
9600 🔽 bps		→ False			
LIN 1.3		> Trigger			
Simple Trigger			ID XXh	Parity	Xh
Start of frame			Data Length	4	•
End of frame	l I	→ 🛡 Trigger *	Data		
Data frame			Byte 1 X	(Xh Byte 2	XXh
Wake up frame		🛉 State x 7	Byte 3 🛛 🗙	(Xh Byte 4	XXh
Sync frame		🕂 Counter x 2	Byte 5 🛛 💙	(Xh Byte 6	XXh
Error Trigger			Byte 7 🛛 🗙	(Xh Byte 8	XXh
Sync error					
Parity error					
Stop bit error					
Checksum error Checksum mode					
Classic					
 Enhanced 					
 Default 				✓ OK	× Cancel

- 1. Channel: Select channels.
- 2. Simple Trigger: Specific trigger function of LIN.
- 3. Error Trigger: Trigger specific error of LIN.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the ID, Parity, Data Length and Data fields, default value is XX means "don't care". When select the LIN 2.2, Data Length field will



be enabled.

LPC Trigger

Supported Models : TL3134B. TL3234B+

LPC Trigger Settings

∭ LPC Trigger Setti	tings	×
Channel	Clause Trigger	
Channel LCLK 0 + LFRAME# 1 + LAD[0] 2 + LAD[1] 3 + LAD[2] 4 + LAD[3] 5 + AUX 6 + Clock Edge Rising Edge + Error Trigger	Clause Trigger Run State 1 True False Trigger Trigger Trigger State 1 Event 1 Cycle Type Start of Frame Clk# START 1 XXXXb	+ OR
START Error CT/DIR Error (Bus Master) Channel Error (DMA) Size Error MSize Error Sync Error		
 Default 	✓ OK	X Cancel

Click LPC Trigger in the toolbar and will show the dialog as the following.

- **1.** Channel: Select LPC channels.
- 2. Clock Edge: Select Rising/Falling clock edge.
- **3.** Error Trigger: Trigger specific error of LPC.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Cycle Type and its parameters, default value is

XX means "don't care". Switch $=/\neq/>/\leq$ by click = button.



	Data Offset
	Fix Offset 0+
Data offset setting:	



MDIO Trigger

Supported Models : TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+.

LA3068B. LA3136B

MDIO Trigger Settings

CHCK WIDIO TH	lgger in the tooldar		lie ulalog	as the following	ig.
∭ MDIO Trigger Sett	tings				×
Channel	Clause Trigger				
MDC 0	Run	S	State 1		
MDIO 1 🗘	State 1	> True	Event 1		🛉 OR
		→ False	ST	Any	_
Clock Latch on		> Trigger	OP	Any	
Rising Edge				=	-
Preamble			PHYADR (P	P)	Xh
32 🗘 bit(s)		→ ▼ Trigger *		F- 20	
Simple Trigger			REGADR (I	R) =	-
		+ State x 7		R = XXh	
Start of frame		+ Counter x 2	DATA	XXXXh	
Stop of frame					
IA EITOI					
O Default				✓ OK	× Cancel

Click MDIO Trigger in the toolbar and will show the dialog as the following

- 1. Channel: Select MDC / MDIO channels.
- 2. **Preamble:** Select the length of preamble.
- Simple Trigger: Specific trigger function of MDIO. 3.
- Clause Trigger: Please reference Clause Trigger chapter. 4.
- 5. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the ST, OP, PHYADR, REGADR and DATA fields, default value is XX means "don't care".

PHYADR(P) / REGADR(R) fields provided the range function:



=	-
=	
!=	
>=	
<=	
In Range	
Not In Range	



ModBus Logic Trigger

TL3K/LA3K Settings

∭ ModBus Trigger Se	ettings				×
Channel	Clause Trigger		State 1		
Idle High Tx 0 Rx 1 Baud Rate	State 1 *	→ True → False → Trigger → Trigger *	Event 1 Rx Bypass 0 Data (ASCII)	Tx Data(s	+ OR
9600 v bps Option Parity None v Mode ASCII v Simple Trigger Start of frame End of frame Parity Error Break/Idle frame		 State x 3 Counter x 2 			
 Default 				♥ ОК	× Cancel

TBA Settings

∭ ModBus Trigger Se	ettings				×
ModBus Trigger Se Channel UART Port LA Port Idle High Tx 0 + Rx 1 + Baud Rate 9600 + bps Option	ttings Clause Trigger Run State 1	→ True → False → Trigger → Trigger * → Trigger *	State 1 Event 1 O Rx Bypass 0 Data (ASCII)	● Tx → Data(s	CR CR C) after Break
Parity None Parity None ASCII Simple Trigger Start of frame End of frame Parity Error Break/Idle frame		 State x 3 Counter x 2 			
 Default 				✓ OK	X Cancel

Channel

UART Port / LA PortSelect ModBus channels.



Baud Rate

Select the baud rate and providing the manual input if no appropriate selection.

Option

Parity Provide None/Odd/Even selections, none parity defaulted.

Mode Provide ASCII/RTU mode, ASCII mode defaulted.

Support the 8-N-1 protocol under RTU mode, 8-N-2 protocol defaulted.

Option	
ParityNone	•
Mode RTU	•
N-8-1	

Simple Trigger Provide Start of frame, End of frame, Parity Error, Break/Idle frame

triggers •

State Provide ASCII/HEX input mode by ASCII/RTU mode.

A	SCII	
	bCII	

RTU

State 1	State 1	
Event 1	R Event 1 + C	R
○ Rx ● Tx Bypass 0 Data(s) after Break Data (ASCII) :1103]



NAND Flash Trigger

Supported Models : TL3234B+. LA3136B. BusFinder (NAND Flash solution)

NAND Flash Trigger Settings

Click NAND Flash Trigger in the toolbar and will show the dialog as the following.

MAND Flash T	rigger Settings					×
Channel	8	Clause Trigger				
CLE	B12 🗘	Run		State 1		
ALE	B13 🗘	State 1	→ True	Event 1		🕂 OR
RE# (W/R#)	B14 🗘		→ False	(Command	
WE# (CLK)	B15 \$		> Trigger	XXh		
CE#	B16 \$				Address	
✓ R/B# ✓ DQS	B17 B18 \$			3-Byte Row Addr.	O 4-Byte Row	v Addr.
Reverse RE#			Trigger *	Condition	Address =	-
Reverse DQS	S		• mggo	Row	XXXXXXh	
DATA			🛨 State x 7	Column/Feature	XXXXh	
 x8 Quick Setup 	○ x16		Counter x 2		Data	
User Defined			- Obunter A 2		Data Offse	t
DQ0 (LSB)	B4 ♦					
Startup Mode				1st 2nd		4th
	T DDR Mode			XXh XXh	XXh	XXh
tREA >= 0ps	tDQSQ >= 0ps		Timer 1			
					Advance	ed Setting >>
Cmds. accept	during busy 🛛 💐	k	Timer 2			
Busy time che	eck 🖏	F				
Default					✓ OK	× Cancel

- 1. Channel: Select CLE, ALE, RE, WE, CE, R/B, DQS channels.
- 2. DATA: Select x8 or x16 bits
 - I. Quick Setup: Only set DQ0(LSB), others will be set automatically.

(e.g. LSB = B4, MSB = B11; LSB = B7, MSB = B14)

II. User Defined:



∭ I/O Channel Settings ×							
1/00	B4 🗘	J/08	}	B12	•		
I/O1	B5 🗘	1/09)	B13	\$		
I/O2	B6 🗘	I/O1	0	B14	•		
I/O3	B7 ‡	/01	1	B15	•		
I/O4	B8 ‡	/01	2	B16	•		
I/O5	B9 🗘	I/O1	3	B17	•		
I/O6	B10 🗘	I/O1	4	B18	•		
1/07	B11 🗘	I/O1	5	B19	•		
 Default 			OK	🗙 Can	cel		

- 6. Startup Mode: Set DDR mode.
- 7. **tREA / tDQSQ:** Set tREA at SDR mode and tDQSQ at DDR mode.

Cime/Div: 7.5	5 ns				A								
Acquired: 11:			-105 ns	97.5 ns -9	0 ns -	82.5 ns	-75 ns	-67.5 ns	-60 ns	-52.5 ns	-45 ns -	37.5 ns	-3
		Idle		DO: 00					00				ρ́ο
	5 I/OO												
	6 I/O1												
	7 I/O2						-						
	8 I/O3		-										
	9 I/O4												
	10 I/O5												
NAND Flash	11 I/O6												
	12 I/O7												
	0 CLE												
	3 ALE												
	4 RE		10n	2	2 2.5 n		7.5n		22.5n		12.5	n	
	2 WE												
	1 CE1												
NandFl	🙀 13 R/B1												
Data Bus	125				00				Į48	<u> </u>	49		
							1			γ			

tREA:

tDQSQ:



Time/Div: 7.5						P		Ą					
Acquired: 12:0	7:49.63	-112.5 ns	-105 ns	-97.5 ns	-90 ns	-82.5	ns -7!	Sins -	67.5 ns	-60 ns	-52.5 ns	-45 ns	-37.5 ns
		Idle	Į	DO: 0E	I	DO: 4	8	D	0: E5	I	DO: C3	I	DO: C2
	O DQO						i.		30n			15n	
	1 DQ1		17.5	n _		27.	5n				32.5	า	
	2 DQ2		17.5	n	12.5	n 🗌	1	7.5n			27.5	า	
	3 DQ3			32.5n	1						57.5	<u>1</u>	
	4 DQ4												
	5 DQ5						1	.7.5n			27.5	า	
NAND Flash	6 DQ6										92.5	า	
	7 DQ7						1			47.5	īn		
	8 CLE												
	9 ALE												
	13 W/R			12.5n		17.5n		12	2.5n		17.5n		12.5n
	12 CLK						i.						
	14 CE1												
	10 R/B1						i.						
Nand Flark	15 DQS		15n		15n		1	5n		15n		15n	
Data Bus	70	00	OE		48	E		E5		C3		C2	

8. Commands accepted during busy: Set NAND commands still could be

triggered during busy state, default is 70h/FFh/78h/7Bh.

Ⅲ Busy Command Settings ×								
Commands								
1 70h	5 XXh							
2 FFh	6 XXh							
3 78h	7 XXh							
4 7Bh	8 XXh							
O Default	✓ OK X Cancel							

Trigger 70h during busy state:

cquired. 10.	35:22.352	1.1.1.1		. 🀳	100 ns	1.1.20	" <u>"</u> "	1.1.1	 1.1.	1.1.1	- 1 - L	 1.1.1.1
		Busy	R	AD STAT	. REG.(70)							Bus
	7 I/O0											
	8 I/O1											
	9 I/O2											
	10 I/O3											
	11 I/O4											
	12 I/O5											
NAND Flash	13 I/O6											
	14 I/O7											
	0 CLE								 			
	1 ALE				_				 	_		
	5 RE							_				
	2 WE											
	6 CE1				_				 			
NandFl	🔸 4 R/B1		_							_		
Data Bus	147										70	

9. Busy time check: Triggers when timing >= tBusy, providing 6 tBusy to check.



🎵 Busy Tir	me Settings	i				×
tBusy1	tBusy2	tBusy3	tBusy4	tBusy5	tBusy6	
tBusy (Ra	ange: 0.1us-	250ms)				
>= 2	50000					us
Comman	d					
		1 XXh				
		2 XXh				
		3 XXh				
		4 XXh				
 Default 					√ок 🗴	Cancel

Trigger the tBusy >= 25 us after NAND command (10h)

7 1/0	Idle	PAGE PROG. #2(10)					Busy
8 1/0							
9 I/C							
9 I/C 10 I/							
10 I) 11 I)							
12 I)							
NAND Flash 13 I,							
14 I,							
0 CL							
1 AL							
5 RE							
2 W							
6 CE							
Nand Flark 4 R/	31		>=25 us	\rightarrow			
Data Bus 14						10	

- **10.** Clause Trigger: Please reference Clause Trigger chapter.
- 11. State: Show the details of trigger condition in every state as left side; selecting the trigger values in the Command, Address and Data fields, default value is XX means "don't care".



PMBus Trigger

Supported Models : TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+.

LA3068B. LA3136B

PMBus Trigger Settings

Click PMBus Trigger in the toolbar and will show the dialog as the following.

MBus Trigger Settin	ngs				×
Channel	Clause Trigger				
PMBCLK 0 ¢ PMBDAT 1 ¢	Run State 1	$ \longrightarrow True \\ \longrightarrow False \\ \longrightarrow Trigger $	State 1	▼ XXh	+ OR
Simple Trigger		Trigger *	Extended	XXh	(Xh
Repeat Start Stop of frame		→ ♥ Trigger *	Any Offe	set O Fixe	ed Offset
ACK		+ Counter x 2	XXh		/
Check PEC			XXh XXh		•
None Group CMD					
 Default 				✓ OK	× Cancel

- 1. Channel: Select I2C / LA port.
- 2. Simple Trigger: Specific trigger function of I2C.
- 3. Check PEC: Trigger PEC.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Address, Command and Data fields, default value is XX means "don't care".

Data field only provided 4 bytes data to trigger, checking the Fixed offset and



selecting the offset value when want to trigger at the specific position. Note: Only TravelBus series provide I2C port channel

ProfiBus Trigger

Supported Models : TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+.

LA3068B. LA3136B

ProfiBus Trigger Settings

Click ProfiBus Trigger in the toolbar and will show the dialog as the following.

M ProfiBus Trigger S	Settings				×
Channel	Clause Trigger				
		→ True → False → Trigger → Trigger * → State x 7 → Counter x 2	State 1 Event 1 Start Delimiter (S DA XX FC XX EDH 16	ih SA ih FCS	OR XXh XXh XXh
Even					
O Default				✓ OK	× Cancel

- 1. Channel: Select channels.
- 2. Simple Trigger: Specific trigger function of ProfiBus.
- 3. Clause Trigger: Please reference Clause Trigger chapter.
- 4. State: Show the details of trigger condition in every state as left side; typing or



selecting the trigger values in the SD packet and its fields, default value is XX means "don't care".

SD/eMMC Trigger

Supported Models : TL3234B+. LA3068B. LA3136B. BusFinder (SD/eMMC

solution)

SD/eMMC Trigger Settings

Click SD/eMMC Trigger in the toolbar and will show the dialog as the following •

👖 SD/eMMC Trigger Sett	ings				×
Channel	Clause Trigger				
CLK A0 🗢	Run		State 1		
CMD A1 AUX A10	State 1	True	Event 1		🛉 OR
Protocol Setting		→ False	Command	O Resp	onse
Protocol		> Trigger	Any Command DATA0 =)	X 0 1	User Defined
SD O eMMC			ST Comm		
CMD Only			XXX XXh		
O CMD + RESP		→ ▼ Trigger *	Stuff Bits[31: XXh	24]	
			Stuff Bits[23:	16]	
		State x 7	XXh Stuff Bits[15	:8]	
✓ CMD Gap Time		🕂 Counter x 2	XXh		
10 ms			Stuff Bits[7: XXh	0	
tODLY Settings			CRC	E	
Host -> Device 0ps			XXh	1	
Device -> Host 5ns					
 DATA Settings 					
Error Check Settings					
Default				♥ ОК	× Cancel

1. Channel: select CLK, CMD as the trigger channel

AUX can be used for checking power state before running CRC error check, disabled by default.

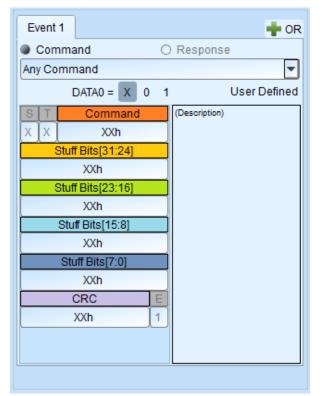
- 2. Protocol: select SD or eMMC trigger
- 3. CMD Gap time: delay trigger between the two CMDs.
- 4. **tODLY Settings:** set the phase delay time such that the device can latch valid



command and response.

5. Clause trigger settings: Please reference Clause Trigger chapter

6. Trigger settings



Parameter :

DATA0 = X 0 1 : use Data0 to judge the R1 and R1b.

Input trigger value, input 'X' means don't care.

Append 'h' for HEX, 'b' for binary, no append for DEC.

When cursor on the input table, the information showed in the right side field.

User Defined add the command reserved:



Command	Description	
Cmd 1	Click To Edit	
Cmd 5	Click To Edit	
Cmd 14	Click To Edit	
Cmd 21	Click To Edit	
Cmd 22	Click To Edit	
Cmd 26	Click To Edit	
Cmd 31	Click To Edit	
Cmd 34	Click To Edit	•



SD/eMMC Data Trigger

Supported Models : TL3234B+. LA3068B. LA3136B. BusFinder (SD/eMMC

solution)

SD/eMMC Data Trigger Settings

Click SD/eMMC Data Trigger in the toolbar and will show the dialog as the

following °

∭ SD/eMMC Data Trigger Setti	ings	×
Protocol Select	Data Trigger Error Trigger	
SD O eMMC	✓ Start Data Trigger after READ command (CMD17/18)	
	Data Address XXh XXh XXh XXh	
Probe Select	✓ Start Data Trigger after WRITE command (CMD24/25)	
LA Probe	Data Address XXh XXh XXh XXh	
	Start Data Trigger after CMD 0 - GO_IDLE_STATE 🌞 as Read 💌 command	
DATA Settings	CMD Command Response	
O 8-bit Data	DAT	
4-bit Data	Pattern P P P P	
O 1-bit Data		
DDR Mode		
HS 400 (MMC)	Data Trigger Pattern	
Data Length (Byte)	Trigger when pattern(s) match	
512 💌	Pattern Size 8 bytes	
	BYTE 00 - 03 XXh XXh XXh XXh XXh	
	BYTE 04 - 07 XXh XXh XXh XXh XXh	
tODLY Settings	BYTE 08 - 11 XXh XXh XXh XXh XXh	
Host -> Device 0ps	BYTE 12 - 15 XXh XXh XXh	
Device -> Host 500ps		
 Default 	V OK X Cancel	

- 1. Protocol: select SD or eMMC trigger
- 2. **Probe Select:** select CLK, CMD and AUX as the trigger channel.
- 3. Data Settings: select current bus width, byte, SDR, DDR of the test object
- 4. **tODLY Settings:** set the phase delay time such that the device can latch valid command and response.
- 5. Data Trigger: set the patterns of data trigger.



∭ SD/eMMC Data Trigger Setti	ings	×
Protocol Select	Data Trigger Error Trigger	
SD O eMMC		
Probe Select LA Probe	CMD	
	DAT Data CRC Status	
DATA Settings	Trigger when IDLE time > 5 ms 💌	
 8-bit Data 4-bit Data 1-bit Data DDR Mode HS 400 (MMC) Data Length (Byte) 512 	Trigger on Data IDLE timeout after CMD CMD Host Command Card Response DAT Data CMD Lists	
tODLY Settings	Cmd 17 Cmd 18 Cmd 24 Cmd 25	
Host -> Device Ops	Trigger when IDLE time > 5 ms v	
Device -> Host 500ps		
O Default	✓ OK X Cancel	

6. Error Trigger: set the condition of idle time to trigger.



Serial Flash / SPI NAND Trigger

Supported Models : TL3234B+. LA3136B. BusFinder series

Serial Flash / SPI NAND Flash Trigger Settings

Click Serial Flash Trigger in the toolbar and will show the dialog as the following.

∭ Serial Fla	sh / SPI N	NAND Flash Trigger Setting	gs			? ×
Channel		Clause Trigger				
CS# SCLK SI/SIO0 SO/SIO1 WP#/SIO2 Hold#/SIO3		Run V State 1	→ True → False → Trigger	State 1 Event 1 Single Mode Single Mode 8 cycles		OR C Logic AND
SIO4 SIO5 SIO6 SIO7 DQS CS# Glitch T None Width <	•		Trigger * State x 7 Counter x 2	 16b 24b 32 O In Out	2b XXXX Dun 0 0	Dummy cycles
✓ tSHSL >= tCLQV >= 8.			Timer 1 Timer 2		Adv	vanced Setting >>
 Default 					✓ OK	× Cancel

- **1.** Channel: Select channels.
- 2. CS# Glitch Trigger: Trigger the glitch on CS# channel.
- 3. tSHSL / tCLQV: Set tSHSL / tCLQV.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Command, Address and Data fields, default value is XX means "don't care".

Provided the Single / Dual / Quad / Octal mode.



Single Mode	-
Single Mode	
Dual Mode	
Quad Mode	
Octal Mode	

SMBus Trigger

Supported Models : TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+.

LA3068B. LA3136B

SMBus Trigger Settings

Click SMBus Trigger in the toolbar and will show the dialog as the following.

∬ SMBus Trigger Setti	ngs				\times
Channel	Clause Trigger Run		State 1		
SMBCLK 0 SMBDAT 1 Protocols Select SMBus Simple Trigger Start of frame Repeat Start Stop of frame ACK NACK Check PEC	State 1	 True False Trigger Trigger State x 7 Counter x 2 	Event 1 Address Command Data Data Any Offs 0 XXh XXh XXh XXh	XXh set O Fixe Byte(s	ed Offset
 Default 				✓ OK	× Cancel

- 1. Channel: Select I2C / LA port.
- 2. Protocols Select: Select SMBus / SBS / SPD protocol.
- **3. Simple Trigger:** Specific trigger function of SMBus.
- 4. Clause Trigger: Please reference Clause Trigger chapter.



5. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Address, Command and Data fields, default value is XX means "don't care".

Data field only provided 4 bytes data to trigger, checking the Fixed offset and selecting the offset value when want to trigger at the specific position.

Note: Only TravelBus series provide I2C port channel

SPI Trigger

Supported Models : TravelBus series. TL3134E. TL3134B. TL3234B+.

Logic Analyzer series. BusFinder series

SPI Trigger Settings

Click SPI Trigger in the toolbar and will show the dialog as the following.

M SPI Trigger Setting	gs				×
Channel	Clause Trigger				
Channel ✓ CS 0 ↔ Clock 1 ↔ MOSI 2 ↔ MISO 3 ↔ Frame guard time ✓ Clock latch data on Rising Edge ♥ Chip select Active Low ♥ Data output delay ● 0 ns Word size 8 ♥ bit(s)	Clause Trigger	→ True → False → Trigger → Trigger * → State x 7 → Counter x 2	Data 2 X Data 3 X	_	Offset XXh XXh XXh XXh XXh XXh
O Default				♥ ОК	× Cancel

1. Channel: Select SPI channels.



- 2. Frame guard time: Only for unchecked CS state.
- **3. Option:** Set SPI parameters.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Data fields, default value is XX means "don't care".

Data field provided 8 bytes data to trigger, checking the Fixed offset and selecting the offset value when want to trigger at the specific position.



SVI2 Trigger

Supported Models : TL3134B. TL3234B+

SVI2 Trigger Settings

Click SVI2 Trigger in the toolbar and will show the dialog as the following.

∭ SVI2 Trigge	r Settings					×
Channel SVC SVD V SVT	r Settings 0 \$ 1 \$ 2 \$ 3 \$	Clause Trigger Run State 1	→ True → False → Trigger	State 1 Event 1 SVD Packet VDD E Xh PSI1 L Xh Load Line Slo		PSIO L V XhV
Error Trigger	ket Error		Trigger *	xh SVID SVT Packet = Xh VDD Vo = XXh	XXh XXh VIO Xh	
SVT Pack	et Error				₩ OK	* Cancel
Default					✓ OK	🗙 Cancel

- 1. Channel: Select channels.
- 2. Error Trigger: Trigger specific error of SVI2.
- 3. Clause Trigger: Please reference Clause Trigger chapter.
- 4. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the SVD and SVT packet, default value is XX means "don't care".

When check the AUX, the trigger function will refer to the state of AUX (High/Low).



SVID Trigger (Upon Request)

Supported Models : TL3134B. TL3234B+. LA3068B. LA3136B

If you have any issues with SVID protocol features, please contact your Intel Field Representative.

SVID Trigger Settings

SVID Trigger Settings × Channel Clause Trigger State 1 Run SCLK 0 🌲 J. > True Event 1 OR State 1 SDATA 1 ‡ → False Address XXh Don't care • ✓ Alert 2 \$ Trigger Command XXh Don't care • = AUX 3 🌲 Master Payload 🔳 XXh • When Alert X Don't care Trigger ACK X Don't care -XXh Slave Payload 🛉 State x 7 🛉 Counter x 2 Error Trigger Parity Error Default ✓ OK X Cancel

Click SVID Trigger in the toolbar and will show the dialog as the following.

- **1.** Channel: Select channels.
- 2. Error Trigger: Set SVID Parity Error trigger.
- 3. Clause Trigger: Please reference Clause Trigger chapter.
- 4. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Address, Command, Master Payload, ACK and Slave Payload fields, default value is XX means "don't care".
 When check the AUX, the trigger function will refer to the state of AUX (High/Low).



UART Trigger

Supported Models : TravelBus series. TL3134E. TL3134B. TL3234B+. Logic

Analyzer series

UART Trigger Settings

Click UART Trigger in the toolbar and will show the dialog as the following.

∭ UART Trigger Settings ×					
Channel UART Port LA Port Idle High Tx 0 Rx 1 Baud Rate	Clause Trigger Run State 1	→ True → False → Trigger → Trigger	State 1 Event 1 Rx Tx Hex Value ASCII Bypass 0 Data(s) after Break Data (Hex) Data Size 8		
9600 ♥ bps Option Data Bits 8 bits ♥ Stop Bits 1 ♥ Parity None ♥ Simple Trigger Start of frame End of frame Break/Idle frame Break/Idle frame Parity Error Parity Error		 State x 3 Counter x 2 	0-3 XXh XXh XXh XXh 4-7 XXh XXh XXh XXh		
 Default 			✓ OK X Cancel		

- 1. Baud Rate: Select UART baud rate.
- 2. Simple Trigger: Specific trigger function of UART.
- 3. Clause Trigger: Please reference Clause Trigger chapter.
- 4. State: Show the details of trigger condition in every state as left side; typing the trigger values in the Data fields, default value is XX means "don't care".



Data field provided 16 bytes data to trigger, checking the Bypass and selecting

the offset value when want to trigger at the specific position.

Note: Only TB1016B. TB1016B+ provide UART port channel



USB 1.1 Trigger

Supported Models : TB1016E. TB1016B. TB1016B+. TL3134B. TL3234B+.

LA3068B. LA3136B

USB 1.1 Trigger Settings

Click USB 1.1 Trigger in the toolbar and will show the dialog as the following.

- 1. Channel: Select channels.
- 2. Simple Trigger: Specific trigger function of USB 1.1.
- 3. Error Trigger: Trigger specific error of USB 1.1.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the PID, Frame Number, Address and Data Field, default value is XX means "don't care".

Data field provided 4 bytes data to trigger, checking the Fixed Offset and selecting the offset value when want to trigger at the specific position.



USB PD 3.0 Trigger

Supported Models : TB1016E. TB1016B. TB1016B+. TL3134E. TL3134B.

TL3234B+. Logic Analyzer Series

USB PD 3.0 Trigger Settings

Click USB PD 3.0 Trigger in the toolbar and will show the dialog as the following.

∭ USB PD 3.0 Trigger Settings ×						
Channel	Clause Trigger					
CC 0 ¢ Data Rate 300 Kbps Simple Trigger Start of frame End of frame	Run State 1	True $ False $ $ Trigger $ $ Trigger $ $ State x 7 $ $ Counter x 2$	State 1 Event 1 SOP Sequences Message Heade XXXXh	Any	+ OR	
Error Trigger SOP error EOP error Chunked bit error CRC32 error			Offset	XXXXh		
Oefault				✓ OK	× Cancel	

- 1. Channel: Select channels.
- 2. Simple Trigger: Specific trigger function of USB PD 3.0.
- 3. Error Trigger: Trigger specific error of USB PD 3.0.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the SOP Sequences, Message Header and Data Obj(s), default value is XX means "don't care".

Provide $0 \sim 7$ offset value for Data Obj(s) field.